

Advanced Synchronization Scheme for Wideband Mobile Communications

Yumi Takizawa, Saki Yatano, and Atushi Fukasawa

Abstract— This paper describes a high performance synchronization scheme based on analog matched filters. Synchronization is the toughest problem for wideband urban mobile communications. A simplified configuration for wideband radio system was designed with advanced synchronization by matched filter technologies.

A set of parallel matched filters has been composed of CMOS semiconductor technologies. New scheme has been proved to realize radio systems with simplified configurations and high performances.

Keywords—synchronization, analog matched filter, mobile communications, parallel matched filter, simplified configurations.

I. INTRODUCTION

Personal communications services (PCS) exploited user-oriented services with still and moving pictures. Demand on wideband data has been grown up according with internet access capability in mobile communications.

A wideband spread spectrum (SS) modulation scheme had first been proposed for radio air interface of personal communications services (PCS) by the authors [1].

When a radio bandwidth is spread wider, effective transmission data rate is not increased proportionally. This phenomena is assumed mainly by the effect of multipath radio propagation and Doppler effect of radio channels.

This study is done high-resolution timing of synchronization which is assumed critical for analysis. The target is focused on a configuration of parallel matched filters to be a solution for this question.

Effective data rate and transmission characteristics are made lower under constrained radio bandwidth and worse propagation condition. Wideband SS modulation, coherent demodulation, and multipath combining technologies are

essential to realize reliable and high quality wideband radio channel. Advanced way of synchronization is developed based on a parallel matched filter for enhancement of the W-CDMA for the next generation.

A prototype hardware was implemented for validation of utility, complexity, and available data rate.

II. THEORY OF WIDEBAND SS MODULATION & DEMODULATION

The system is composed of wideband SS modulation. Combined codes of Pseudo Noise (PN) and Hadamard sequence (Walsh function) are used for SS modulation. Quadrature Phase Shift Keying (QPSK) modulation is followed with SS modulation. Transmission data is divided into two streams of in-phase and orthogonal phase components a , b respectively. Transmitter output $x(t)$ is written as,

$$x(t) = (a + jb)\phi(t)\psi(t) + \phi(t) \quad (1)$$

where, $\phi(t)$, $\psi(t)$ are PN and Walsh codes. Receiver input $y(t)$ is written as,

$$y(t) = \{(a + jb)\phi(t)\psi(t) + \phi(t)\} \gamma \exp(j\theta), \quad (2)$$

where, γ , θ are the amplitude and phase parameters of radio propagation. The following processing is done.

$$\begin{aligned} u &= \frac{1}{T} \sum \phi(t)\psi(t)y(t) \\ &= \frac{1}{T} \sum \phi(t)\psi(t)\{(a + jb)\phi(t)\psi(t) + \phi(t)\} \cdot \gamma \exp(j\theta) \\ &= \left\{ (a + jb) + \frac{1}{T} \sum \psi(t) \right\} \gamma \exp(j\theta) \\ &= (a + jb)\gamma \exp(j\theta) \end{aligned} \quad (3)$$

where, the following relationship is used,

$$\frac{1}{T} \sum \phi^2(t) = 1, \quad \frac{1}{T} \sum \psi^2(t) = 1, \quad \frac{1}{T} \sum \psi(t) = 0$$

and

$$\begin{aligned} v &= \frac{1}{T} \sum \phi(t)y(t) \\ &= \frac{1}{T} \sum \phi(t)\{(a + jb)\phi(t)\psi(t) + \phi(t)\} \cdot \gamma \exp(j\theta) \end{aligned}$$

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$$= \left\{ (a + jb) \frac{1}{T} \sum \psi(t) + 1 \right\} \gamma \exp(j\theta)$$

$$= \gamma \exp(j\theta) \tag{4}$$

Demodulated signal \hat{d} following result is obtained as,

$$\hat{d} = u * v$$

$$= (a + jb) \gamma \exp(j\theta) \gamma \exp(-j\theta)$$

$$= \gamma^2 (a + jb) . \tag{5}$$

Eq. (4) includes the information of phase rotation caused by radio propagation. Compensation of phase rotation is achieved by Eq. (5). Finally transmission data can be demodulated without distortion.

III. PRACTICAL CONFIGURATION OF WIDEBAND SS MODULATION & DEMODULATION

An oversight link of radio channels is featured by multipath radio propagation (multiple times of diffraction), which degrades the characteristics of radio channels[2].

A pilot signal is transmitted for system synchronization of target base station and path synchronization of received multipath components. Unreliable synchronization causes serious deterioration of coherent demodulation and transmission characteristics of high data rate. Accurate path timing enables fine discrimination and fine combining of each multipath component. It is assumed as an essential factor to enhance capabilities of wideband SS modulation for higher data rate transmission.

Basic configuration of new W-CDMA is shown in Fig.1 composed by the Eqs. (1) – (5). This study correspond to receiver under painted in Fig.1.

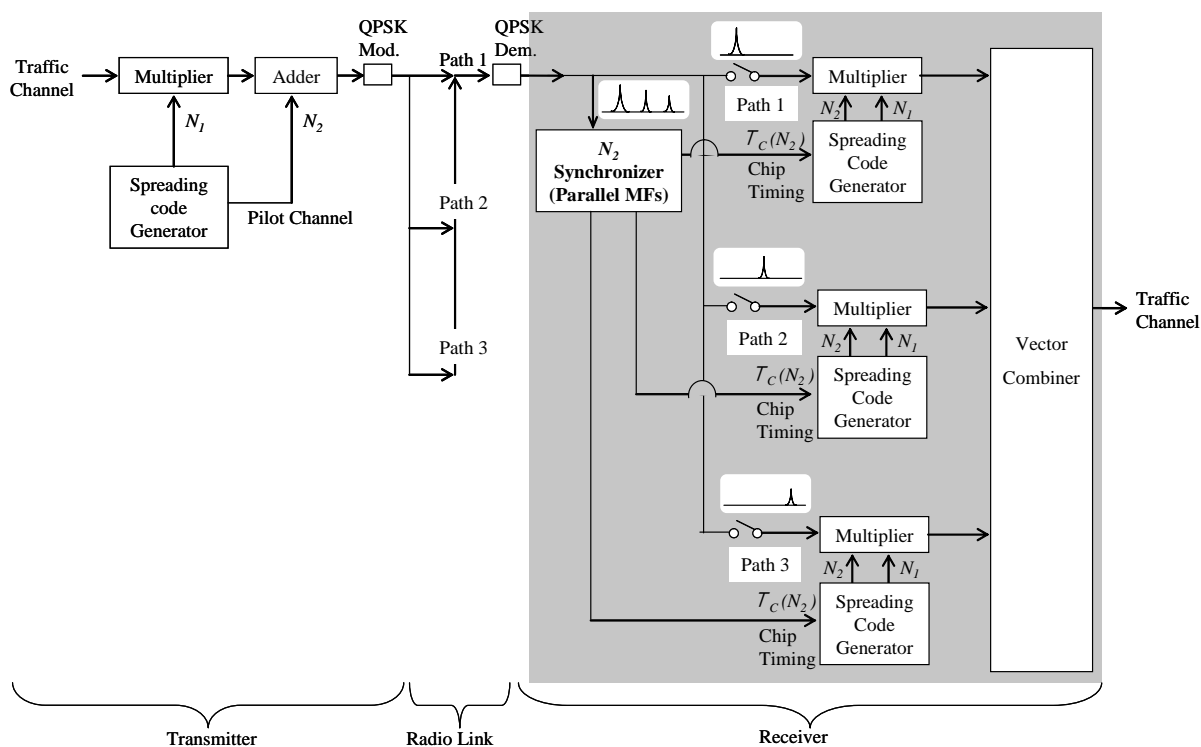


Fig.1 Basic Configuration of new W-CDMA.

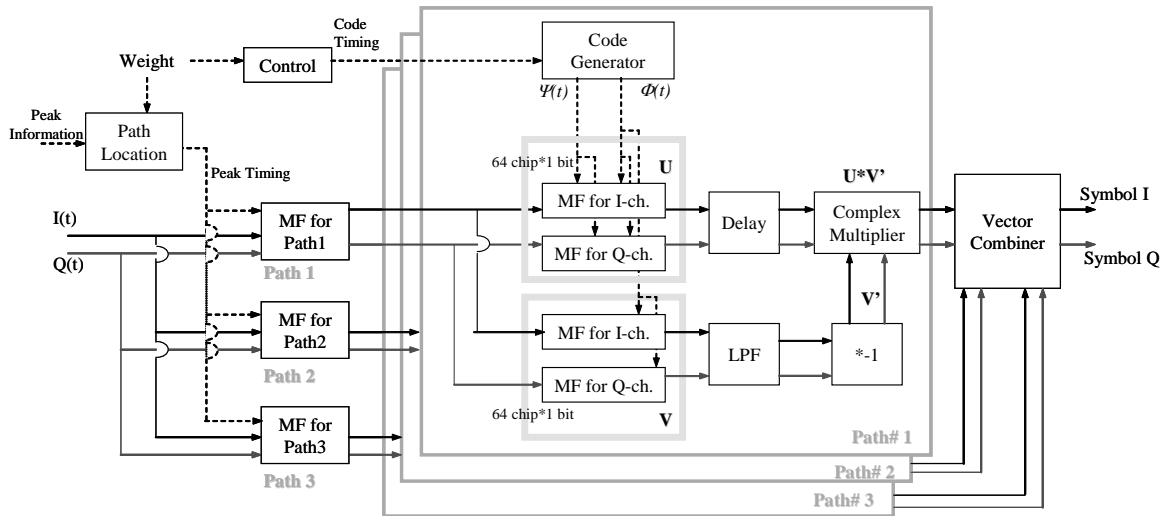


Fig.2 Practical UV calculation using path information from path synchronizer

The number of UV calculator depends on number of paths. In Fig.2, 3 UV calculators are provided due to consideration of 3 paths. A practical configuration is shown in Fig.2 describing detail of UV calculation operation.

The most essential requirement in UV calculation are:

- (1) I,Q signal calculation in synchronized time must be conducted to be time adjusted by path information, and
- (2) generation of Walsh and PN codes in synchronization must be mutually adjusted with the data itself.

IV. SYNCHRONIZATION WITH A PARALLEL MATCHED FILTER CONFIGURATION

Configuration of a set of parallel matched filters is shown in Fig.3 for synchronization. Over sampling and long timeframe are needed to extract correlation peaks with fine resolution and precise point of timing. An useful strategy was given for common designing of cell synchronization (between cell site and mobile) and path synchronization (among radio propagate paths between a cell site and a mobile).

One sampling per chip is taken, 1024 chips are required for cell synchronization. Four samplings per chip are taken, 256 chips are required at least for path synchronization.

Timing of path synchronization must be designed with high resolution toward vector combining of multiple paths.

Extremely short data processing time is required especially for synchronization and coherent demodulation compared to other processing and operations in a radio system.

Synchronization is done by acquisition firstly and holding secondly. Timing of synchronization is defined as timing of acquisition. Acquisition is performed to fined peak of correlation value C . Holding is to keep the obtained timing in spite of jitter caused by noise.

A. Configuration of a parallel matched filters

Correlation value C is given for signals X and Y , n is a flame length,

$$C = \sum_{i=1}^n (X_i \cdot Y_i). \tag{6}$$

When X is a time sequence, $X = X(k, i)$, and k is the flame time, i is the time in a flame,

$$C_k = \sum_{i=1}^n (X_{k,i} \cdot Y_i). \tag{7}$$

When X is a signal time sequence S , and Y is a PN code sequence PN ,

$$C_k = \sum_{i=0}^n (S_{k-i} \cdot PN_i^+) - \sum_{i=0}^n (S_{k-i} \cdot PN_i^-). \tag{8}$$

where the notations of right shoulder of PN code are defined corresponding to signs of chip value of PN code (+1, -1).

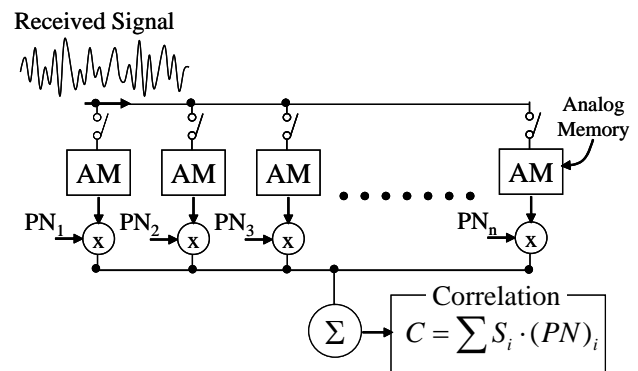


Fig. 3 Parallel Analog Matched Filters for Advanced Synchronization. Notations in the figure are ;
Received Signal: S , Spreading Code: PN ,
Correlation Value: C , and Analog Memory: AM .

V. SYNCHRONIZATION BASED ON ANALOG OPERATION

Analog operation is introduced for processing of huge and high-speed data analysis of correlation operation. A parallel matched filter configuration is studied and applied to realize this scheme[4][5]. Current mode is adopted to compose a synchronization system. The block diagram is shown in Fig.4.

Received analog voltage is converted to analog current S . Each sampled data S_j is stored in each analog current memory CM_j sequentially included in each matching cell. When all the memories are written fully and correlation calculation is executed, old data are overwritten with new data. For correlation operation, stored data are not shifted, but PN code sequence is shifted chip by chip. PN code sequence and "Activation Flag" are both shifted by shift-registers (REGs). Activation flag locates the target cell storing the signal. Correlation operation is achieved by current summation/subtraction operation. The output current representing values of correlation is directly converted to a digital format by the low-power A/D converter also developed with low power consumption in this work.

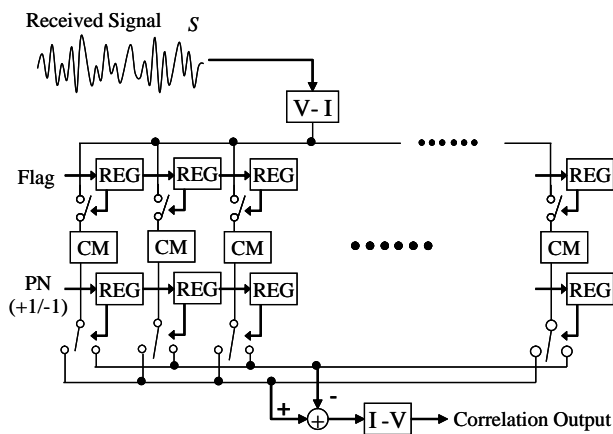


Fig. 4. Block diagram of analog matched filter.

A prototype chip has been composed of 8 parts as shown in Fig. 5. A part is composed of 256 taps as a filter.

A set of 4 parts is connected in serial as a 1024 taps filter used for cell synchronization of I- or Q- components of QPSK signal. A set of 4 parts is connected in parallel as a 256 taps filter. Each filter operates with a quarter phase shift of a chip time for path synchronization.

The chip designed by a 0.35- μm rule CMOS occupies a very small space of 0.49mm². The chip includes an output A/D converter and dissipates 1.65mW at 11Mchip/s operation under 2V power supply[5]. The power consumption and dimension of the LSI are reduced into 1/16 ~ 1/32 of power consumption and size designed by digital LSI.

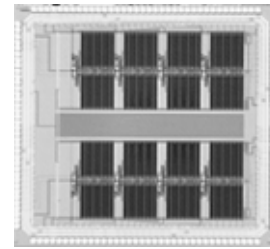


Fig.5. An analog LSI chip for parallel matched filters.

VI. VALIDATION BY A PROTOTYPE HARDWARE

Complex and large quantity of processing steps are validated by field programmable gate array (FPGA), and flexible management of data and process are done by micro processor unit (MPU).

A prototype model is designed for 40 MHz and 5 MHz band width for the forward and reverse links at 3.5 GHz radio frequency band. Variable data rate is adopted at multiple times of 64 Kbit/sec. The data rate of 64 Kbit/sec ~ 32 Mbit/sec is designed to the forward link for download of broad band data of high quality video data.

Prototype hardware was designed and implemented. This hardware was developed by the aid of automatic characteristic monitoring system with registers fabricated in FPGA board and read and write access software fabricated in a personal computer[3][4][5].

VII. SIMULATION ON CHARACTERISTICS OF SYNCHRONIZATION

The characteristics of synchronization have been evaluated by computer simulation.

The configuration is written in Fig.1. The specification is follows. Base stations are all synchronized to GPS satellite.

Acquisition success rate and calculation times are shown in Fig.6 For example, 2 path (3dB) denotes acquired number of path are two and E_b over $N_o = 3\text{dB}$.

Synchronization has been established approximately 20, 40, 80 ms for the case of 1,2,3 successful number of paths under condition of $N_o/E_b = 6\text{ dB}$. It is found that the newly proposed scheme of synchronization has been confirmed to enhance the W-CDMA effectively.

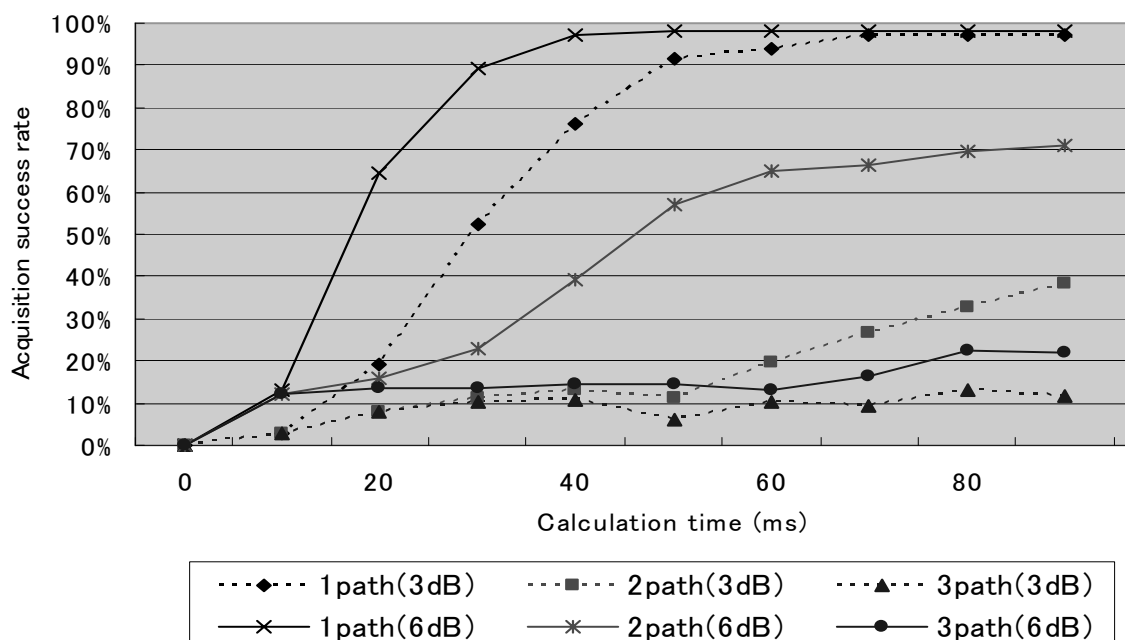


Fig.6 Acquisition Success Rate and Calculation Time.

VIII. CONCLUSION

The result of this study will contribute to enhance the quality of mobile communications and to reduce communication cost compared to existing network and services.

It is found that fast and reliable synchronization have been proved practical and this result is effective and useful to design practical system for wideband mobile radio system applied to RF channel composed of oversight link, which is radio path of reflection and diffraction.

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