

Fig. 2. Wave of THmn

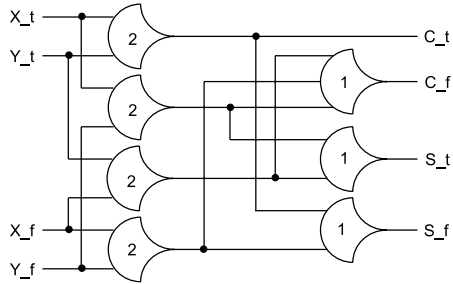


Fig. 3. NCL Half Adder

TH gate has two parameters, one is the number of inputs and the other is a threshold value. A hysterisial threshold gate which has n-inputs and threshold n is described as THmn hence force. Fig.2 is wave of THmn. Note that the threshold m means that the gate output is activated to ON when m inputs or more are activated. Afterward output retains ON while all of input deactivated to OFF. In other words, TH gate is a special gate such as threshold of activating and deactivating are different. Note that a THmn has activating threshold m and deactivating threshold 1, thus the output has hysteresis.

NCL circuit which has TH gate can synthesize. Fig.3 is NCL half adder. It can synthesize register and control circuit as well as combinational circuit [9].

Fig.4 shows a TH gate synthesis using MOS transistors. It is called *block type* TH gate because it has four MOS network blocks. For instance, Fig.5 is a block type TH23 gate. Block type requires a number of MOS transistors.

III. DESIGN OF TH GATE USING ν MOS

A. Basis of ν MOS

ν MOS (neuron MOS) is one of the floating gate which has some inputs and an output. Fig.6 is the structure of ν MOS and fig.7 is the equivalent circuit. The behavior of ν MOS is as follows. Suppose $V_0=0$ as in fig.7 and the V_F in the floating gate is stated as follows.

$$V_F = \frac{\sum_{i=1}^n C_i V_i}{\sum_{i=0}^n C_i} \tag{1}$$

That is, V_F increases depending on the number of asserted inputs m' . When threshold voltage is V_{th} and $C = C_1 = C_2 = \dots = C_n$, the ON condition of ν MOS is stated as follows.

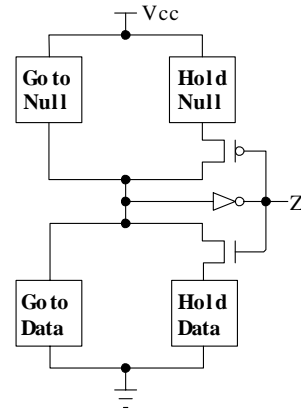


Fig. 4. Block type TH gate

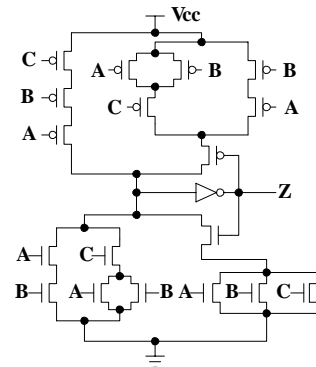


Fig. 5. Block type TH23

$$V_F = m' \cdot \frac{C}{nC + C_0} V_d > v_{th} \tag{2}$$

where C_0 is the capacitive coupling coefficient between the floating gate and the substrate. Therefore, when the number of activated inputs m' exceeds threshold m , the ν MOS activate to ON.

Fig.8 is a ν MOS threshold gate having three inputs. The output of the gate is activated when two or more inputs are activated.

In the following we propose two kinds of techniques to implement TH gates. The one is a technique exploiting ν MOS at blocks in Fig.4, and the other is ν MOS with feedback to synthesis TH gate. Both techniques reduce the number of MOS transistors then higher speed operation is expected.

B. ν MOS TH gate

The proposed TH gate (hysterisial threshold gate) with feedbacked ν MOS is shown in Fig.10. In case of THmn, the number of feedback inputs $|I_f|$ is

$$|I_f| = (m - 1). \tag{3}$$

And the number of unit capacitance $|C_u|$ is

$$|C_u| = n + (m - 1). \tag{4}$$

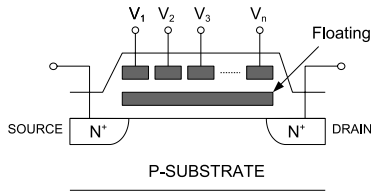


Fig. 6. Structure of νMOS

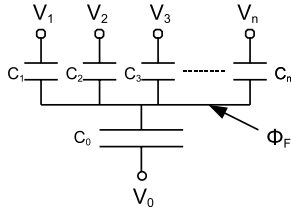


Fig. 7. Equivalent circuit

Thus initially an $n + m - 1$ inputs νMOS has to be prepared to fabricate THmn.

Instead of the above, a feedback with capacitance;

$$C_f = (m - 1) \cdot C_u \quad (5)$$

in a νMOS can fabricate the same THmn gate.

Let's consider the case $|C_u| = n + (m - 1)$ for simplicity. In Fig.10, when activated inputs are m or more, the output V_{out} goes up HIGH (ON), and the feedback input also activated to ON. In the sequel, V_F goes up by bias voltage $(m - 1) \cdot C_u$. Then until all the activated inputs goes down to LOW, V_{out} retains ON because the V_F stays $m \cdot C_u$ or more.

Fig.11 indicates TH23 with νMOS. The TH23 SPICE simulation results as Fig.12. The result shows when two or more inputs are activated to HIGH, the output goes to HIGH and a feedback input is also activated. Then floating gate voltage V_F is biased by C_u and the output remains HIGH until all input goes down to LOW.

C. Block type TH gate with νMOS

The second technique is block type TH gate with νMOS. Block type TH gate has four MOS network blocks. Each block can be defined simple threshold function. Define threshold function $Th(x)$ as;

$$Th(x) = \begin{cases} ON & m' \geq x \\ OFF & otherwise \end{cases} \quad (6)$$

where m' is the number of activated inputs. Then the four blocks in Fig.4 can be synthesized with $Th(x)$. The activating conditions of each block is stated as follows;

- GOTO NULL : Th(m)
- GOTO DATA : Th(m)
- HOLD NULL : Th(1)
- HOLD DATA : Th(1)

Therefore, each block can be synthesized only one νMOS.

Fig.14 is the block type TH23 with four νMOS's. Clearly Fig.14 is simpler construction than traditional block type th23

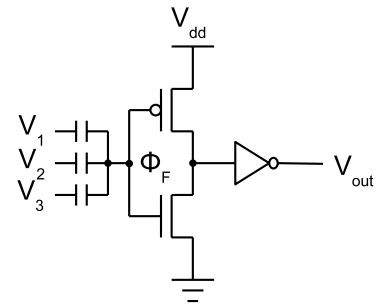


Fig. 8. Three inputs threshold νMOS gate

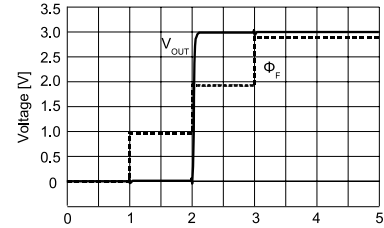


Fig. 9. Characteristic wave form of νMOS

in Fig.5. Especially, delay of block type TH gate is depend on GOTO NULL block, then the delay is reduced because GOTO NULL block in Fig.13 has only one transistor. Note that connecting PMOS transistors makes longer delay.

IV. DESIGN AND EVALUATION

We designed THmn gates made from νMOS with feedback and from block type νMOS. Some comparison with the number of MOS transistor and delay are provided here. We prepared MOS FET SPICE model provided by MOSIS [12] for simulations. The process rule is TSMC 0.35[μm] and supplying voltage is 3.3[V].

And We tried to design THmn gates in a layout level. Fig.15 is TH33 with νMOS block-type in a layout level. We used MAGIC layout tool [13] in order to design it and chose Poly1-Poly2 technology. Fig.16 is structure of floating-gate using Poly1-Poly2 technology.

On the basis of these, the value of each parameter in TH33 is Table.II.

Table.III shows the comparison of the number of MOS FETs. Clearly, in Table.III, the number of MOS transistors of the proposed circuits is constant irrespectively of the number

TABLE II
PARAMETERS OF TH33

parameters	value
process rule	0.35 [μm]
V_{DD}	3.3 [v]
C_1, C_2, C_3	36.0 [fF]
C_0	14.1 [fF]
W/L of pMOS	10.75 [μm] / 0.75 [μm]
W/L of nMOS	5.00 [μm] / 0.75 [μm]

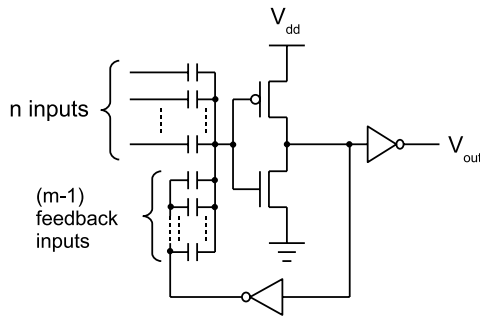


Fig. 10. nuMOS THmn gate

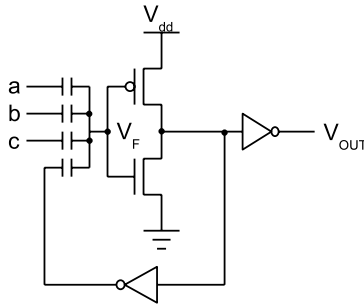


Fig. 11. nuMOS TH23

of inputs or the value of threshold. On the other hand, traditional circuits increase the number of transistors accordance with n and m . Therefore proposed circuit technique is adequate for asynchronous systems.

Table.IV shows that the proposed circuits yields fewer delay than traditional circuits. The delay of traditional circuits depends on number of PMOS in GOTO NULL block. Although nuMOS block type is similar structure to the traditional one, it has only one PMOS in GOTO NULL block. Hence the delay of THmn with blocked nuMOS does not depend on the number of inputs or the value of threshold as shown in table.IV.

Finally, a design of asynchronous full adder consists of THmn gate is shown in Fig.17. Note that the symbols, shaped a ginkgo leaf, indicates a THmn gate where a numeral on a symbol is a threshold value of the gate. The computational wave form is also shown in Fig.???. This simulation provides favorable operations.

TABLE III
THE NUMBER OF MOS TRANSISTORS

	Ordinary	THmn with C-nuMOS	Blocked THmn with nuMOS
TH22	12	6	8
TH23	18	6	8
TH24	18	6	8
TH33	16	6	8
TH44	20	6	8
Full Adder	80	24	31

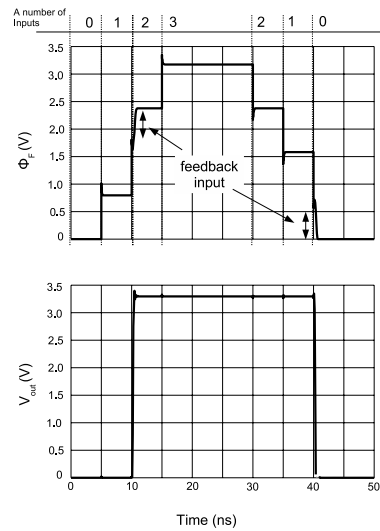


Fig. 12. wave of V_F-V_{OUT}

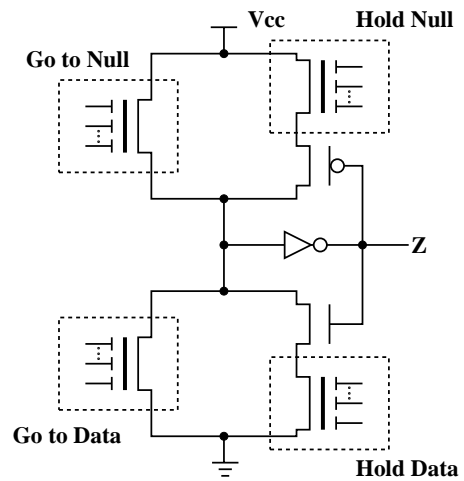


Fig. 13. Block type TH gate with nuMOS

V. CONCLUSION

In this paper, we proposed exploiting nuMOS to hysterisial threshold gates, which is one of the floating gate, for asynchronous systems. Two types nuMOS TH gates are provided and they are compared with traditional constructed NCL TH gates. As a result, we showed nuMOS TH gates are smaller and faster than traditional one. And the number of MOS FETs and average delay time are efficiently reduced to 62% and 49% compared with traditional one, respectively. As a future work, we will try to design larger circuits like a multiplier.

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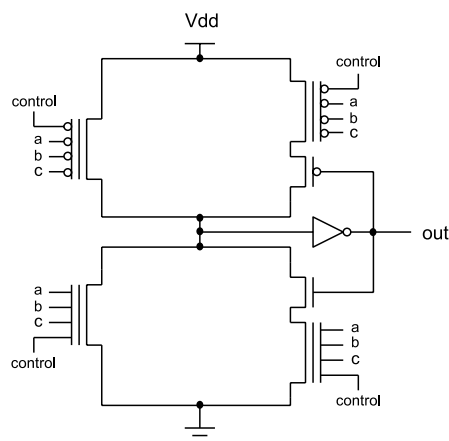


Fig. 14. Block type TH23 with ν MOS

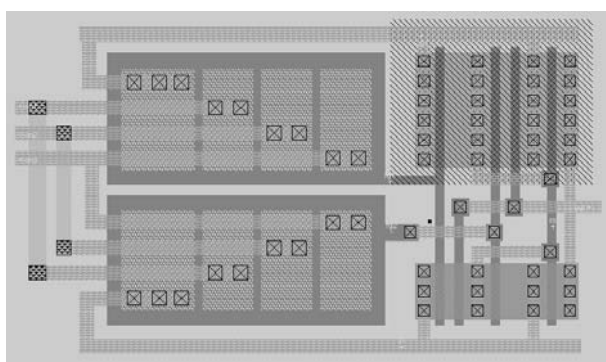


Fig. 15. TH33 layout pattern

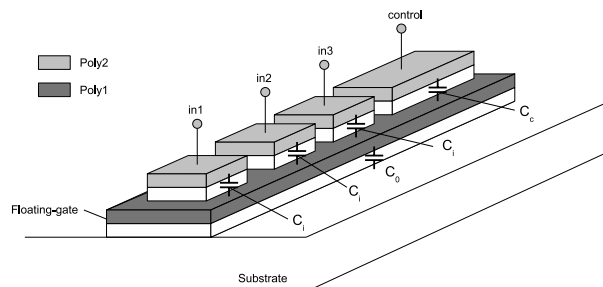


Fig. 16. Structure of Floating-Gate

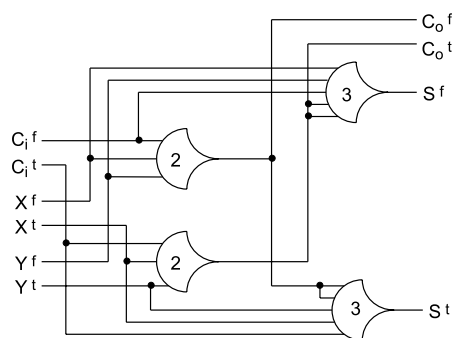


Fig. 17. Full Adder based on ν MOS THmn Gates

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 [13] MAGIC VLSI layout tool, <http://opencircuitdesign.com/magic/>

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TABLE IV

AVARAGE DELAY OF THGATE [PSEC]

	Ordinary	THmn with C- ν MOS	Blocked THmn with ν MOS
TH22	280	160	266
TH23	450	260	271
TH24	890	416	390
TH33	400	197	348
TH44	535	220	423
Full Adder	1041	499	646