An Improved Very-Low Power Pre-amplifier for use with Un-gelled Electrodes in ECG Recording

Cédric Assambo, Martin J. Burke

***Abstract*—**This paper describes the development of an extremely low-power pre-amplifier intended for use in un-jelled electrode recording of the human electrocardiogram. For a lead-II ECG configuration the signal level catered for extends from 100μV to 10mV. The amplifier has a gain of 42dB with a 3dB bandwidth of 0.05Hz –1.7kHz and an differential input impedance of 340MΩ. The CMRR exceeds 85dB. Its gain and phase characteristics meet the requirements of the AHA and EU 601 standards. It has a power consumption of 20μW operating from a 3V supply. It is intended for use in light, portable electrocardiographic and heart-rate monitoring instrumentation.

***Keywords*—** Dry-electrodes, ECG, Skin-Electrode Interface, Ultra-low power amplifier.

I. Introduction

MEASUREMENT of the human electrocardiogram (ECG) is one of the most valuable diagnostic tools in clinical medicine. In recent years, there has been increasing interest in the recording of the human electrocardiogram (ECG) using dry or un-jelled electrodes. Monitoring of the ECG has also extended outside of the conventional clinical scenario into other areas such as cardiac rehabilitation, neonatal infant monitoring, sports medicine and athletics. In conventional recording of the ECG, a coupling gel is used with the electrodes which must be placed correctly on the subject's body. However, in many non-clinical situations where the ECG is monitored, it is more convenient to incorporate re-useable dry electrodes which do not require a coupling gel into an elasticated belt or vest worn by the subject. In these scenarios the demands placed on the recording amplifier are more stringent than in conventional recording. This article reports the design of an improved low-cost preamplifier based on an earlier design [1], having extremely low power consumption which meets the requirements of dry-electrode recording and allows a signal of adequate quality for clinical diagnostic purposes to be obtained.

Manuscript received March 1, 2007. This work was supported by Grant POC 102/2005 received from Enterprise Ireland on behalf of the Government of the Rep. of Ireland. Revised version received June 19, 2007

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II. Design Requirements

In clinical diagnosis involving the ECG signal, it is of the utmost importance that the profile of the signal be as faithfully preserved as possible en route from the electrodes to the recorder output. The principal factors influencing the input stage amplifier design, which affect the quality of the recorded ECG signal are: the skin-electrode-amplifier interface and its frequency dependence [2, 3]; interference rejection and the amplifier common-mode rejection ratio (CMRR); amplifier offset voltage and bias currents; and semiconductor noise generated in the amplifier.

A. The Skin-Electrode-Amplifier Interface

A physical model of the skin-electrode interface and its equivalent electrical model are shown in Fig.1. The electrical equivalent circuit has six passive elements, as simpler models prove to be inaccurate in determining the frequency dependence of the interface with the amplifier [4]. It can be seen that there is one resistor-capacitor network associated with the skin-electrode contact and one associated with the epidermal layer of the skin itself. There are also associated polarisation potentials which are treated as dc voltage sources.

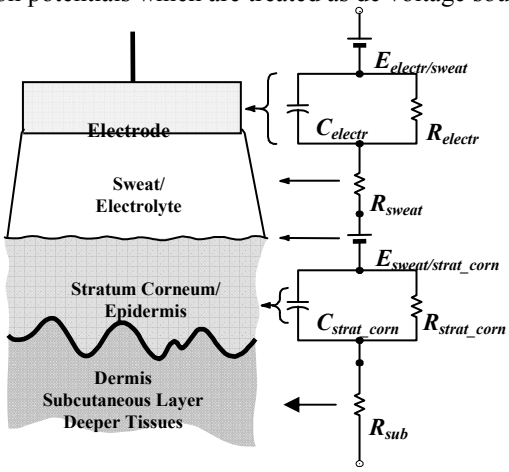

Fig. 1 Skin-electrode interface and its electrical equivalent circuit [5].

A set-up, showing the detection of an ECG signal from the body using two electrodes and an amplifier having a differential input impedance of R_{in}, is illustrated in Fig. 2. The input impedance of the amplifier is taken as purely resistive as the capacitance is extremely small.

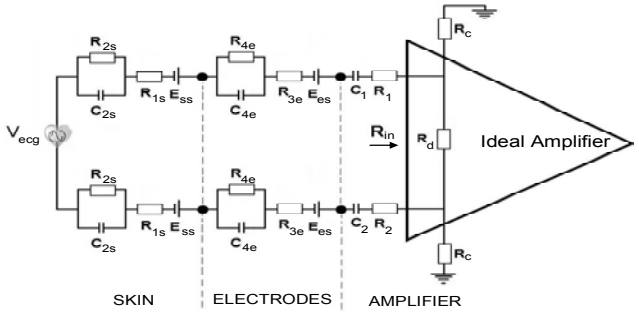

Fig. 2 Measurement of the ECG using two identical Electrodes and a differential amplifier.

The transfer function of the combined skin-electrode-amplifier network as measured at the amplifier input is given as:

$$H_0(s) = \frac{R_{in}}{R_{in} + 2\left(Z_i + R_l + \frac{1}{sC_l}\right)} \qquad (1)$$

where:

$$R_{in} = R_d // (2R_c) \qquad (2)$$

and

$$Z_i = R_{1s} + R_{3s} + \frac{R_{2S}}{1 + sR_{2s}C_{2s}} + \frac{R_{4e}}{1 + sR_{4e}C_{4e}} \qquad (3)$$

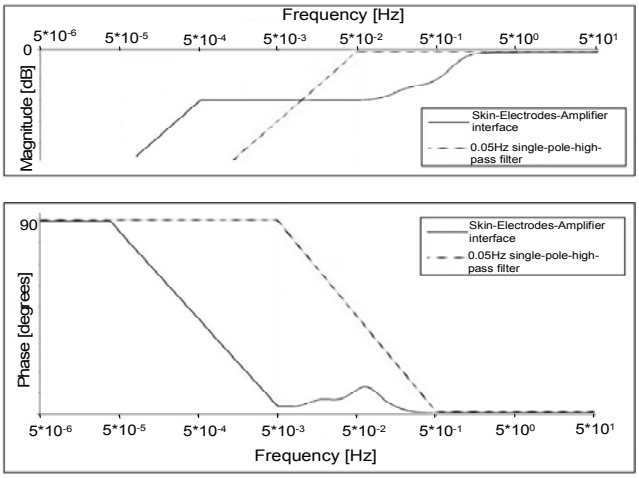

Fig. 3 A Bode plot of the magnitude and phase.

The dc polarisation potential of dry electrodes can be much higher than is the case with conventional electrodes and is best eliminated by using dc blocking capacitors, C_1 and C_2, in series with the electrodes as shown. This can give rise to phase distortion of the ECG signal if the input impedance of the amplifier is not high enough. The recommendations of the American Heart Association on the performance of ECG recording equipment [6] require that the amplifier should introduce no more phase shift into the signal than that which would be introduced by a single-pole high-pass filter having a cut-off frequency of 0.05Hz, as indicated in Fig. 3. It can be shown that in order to meet this requirement the input resistance of the amplifier must meet the requirement:

$$R_{in} > \frac{20}{\pi}\left(\frac{R_{2s}}{R_{4e}C_{4e}} + \frac{R_{4e}}{R_{2s}C_{2s}} + \frac{1}{C_1}\right) \qquad (4)$$

B. Sources of Interference

Movement of the subject during exercise induces pressure variations at the skin-electrode interface, which generate artefact in the signal present at the amplifier input. Much of this occupies the very low frequency range and is suppressed by the use of ac coupling as described above. However, other sources of electrical interference exist which generate interference that occupies the spectrum of the signal and cannot be removed by filtering.

Unwanted in-band signals can be superimposed on the wanted ECG signal at the amplifier input by means of electrical interference, particularly that caused by the mains power supply. Mains hum can be introduced into the ECG by two means, namely electromagnetic induction and electrostatic induction. In the case of electromagnetic induction, the magnetic field associated with mains supply current flowing in nearby electrical equipment cuts the loop enclosed by the subject, the electrode leads and the amplifier and induces an emf in the leads. This emf is directly proportional to the area of the loop but, in the case of electrodes and a preamplifier mounted in a belt or vest worn by the subject, there is little or no loop area present and hence this type of interference is not prevalent.

In the case of electrostatic induction, the electric field associated with the mains supply is capacitively coupled to the subject who is also coupled to ground via their body capacitance. With battery-operated instruments, when the common supply line of the amplifier is not at true earth potential, there is also an isolation capacitance present. A displacement current then flows through the subject to ground, developing an interfering signal at the input to the recording amplifier. When the electrodes are mounted close together on the subject, the interference is predominantly common-mode. Displacement currents of the order of 0.5μA have been measured by the authors generating a typical interfering signal level of 40mV. The common-mode rejection ratio (CMRR) of the amplifier must be relied upon to suppress this interference.

C. Amplifier Common Mode Rejection Ratio

A schematic diagram of a standard simple 3 op-amp instrumentation amplifier is shown in Fig .4. Practically all ECG amplifier input-stages can be shown to have an equivalent structure of this form. There are three primary factors which limit the CMRR obtainable, namely: common-mode impedance mismatch at the amplifier input, ΔZ; manufacturing tolerances in the gain-determining resistors, ΔR and the finite $CMRR_{op}$ of the op-amps used to implement the amplifier. The overall CMRR of the amplifier is determined by the combination of these effects as:

$$\frac{1}{CMRR} = \frac{1}{CMRR_{\Delta Z}} + \frac{1}{CMRR_{\Delta R}} + \frac{1}{CMRR_{op}} \qquad (5)$$

For a minimum input ECG signal level of 100μV and a maximum error of 1% at the amplifier output due to the interference, a CMRR of 92dB is required.

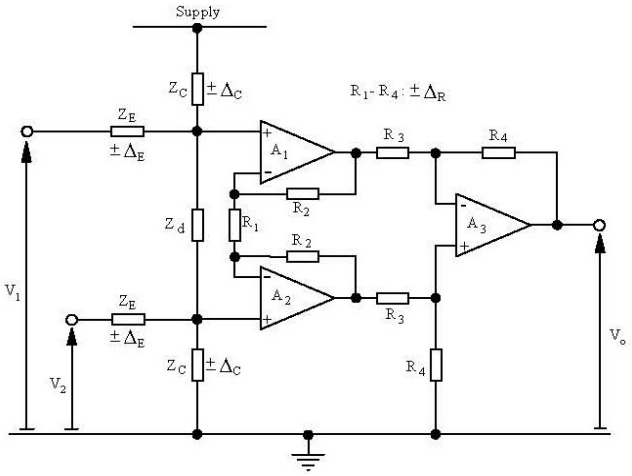

Fig. 4 A standard instrumentation amplifier.

A common-mode signal present at the input to the electrodes gives rise to a differential component at the amplifier input, due to mismatch in the common-mode impedances on either side of the amplifier. The CMRR due to the impedance mismatch is:

$$CMRR_{\Delta Z} = 20\log_{10}\left[\frac{Z_C}{Z_E}\right] + 20\log_{10}\left[\frac{1-\Delta_C^2}{2(\Delta_C+\Delta_E)}\right] \quad (6)$$

where Z_C is the common-mode input impedance of the amplifier, Z_E is the electrode impedance and Δ_C and Δ_E are the variations in these impedances, respectively. The dominant variation is that of the electrodes which, if considered to be mismatched by a factor of 2:1 gives $\Delta_E = 0.33$ and with $\Delta_C = 0.03$, makes the right hand term of the above expression equal to 3.6dB.

The CMRR due to a manufacturing tolerance, $\pm\Delta_R$ in the gain-determining resistors, when these are assigned to give the highest degree of imbalance between the inverting and non-inverting sides of the amplifier, can be shown to be:

$$CMRR_{\Delta R} = 20\log_{10}\left(1+2\frac{R_2}{R_1}\right)\left(\frac{1+\frac{R_4}{R_3}}{4\Delta_R}\right) dB \quad (7)$$

This shows that the effect of the resistor mismatch in the differential-to-single-ended second stage of the amplifier is reduced by the gain of the preceding differential input stage. It is also the case that the mismatch of the resistors in the differential stage does not influence the CMRR because of the cross-symmetrical nature of this stage. This favours the use of as high a gain as possible in both stages of the amplifier as well as the use of low-tolerance resistors.

The final component of the overall CMRR is determined by the $CMRR_{op}$ of the individual op-amps used to implement the amplifier. This is given as:

$$\frac{1}{CMRR_{op}} = \frac{1}{CMRR_{op1}} + \frac{1}{CMRR_{op2}} + \frac{1}{\left(1+2\frac{R_2}{R_1}\right)\left(CMRR_{op3}\right)} \quad (8)$$

It can be seen that the CMRR of the op-amp used in the differential-to-single-ended stage is less significant than that of the other op-amps by a factor equal to the gain of the differential-input stage. If the latter is high and if all op-amps are identical, then $CMRR_{op} = 1/2(CMRR_{op1})$, or 6dB lower than that of a single op-amp.

D. Semiconductor Noise

In its passage through the amplifier, the signal quality is degraded by any added noise. The total rms output noise voltage of a standard non-inverting single op-amp structure is given by:

$$v_{no} = \sqrt{\left(1+\frac{R_2}{R_1}\right)^2 v_{na}^2 + i_{na}^2 R_2^2 + \left(1+\frac{R_2}{R_1}\right)^2 i_{na}^2 R_i^2 + \left(1+\frac{R_2}{R_1}\right)^2 v_{nR_i}^2} \quad (9)$$

where v_{na} and i_{na} are the noise voltage and current respectively of the op-amp, referred to its input and v_{nRs} is the noise voltage generated by the equivalent source resistance, R_S. The noise generated by the resistors R_1 and R_2 can be included as part of the source resistance. The output noise voltage can be scaled by a factor of $\sqrt{2}$ when considering a two op-amp instrumentation amplifier input stage. The profiles of the noise voltage and noise current as functions of frequency are shown for a typical operational amplifier in Fig. 5.

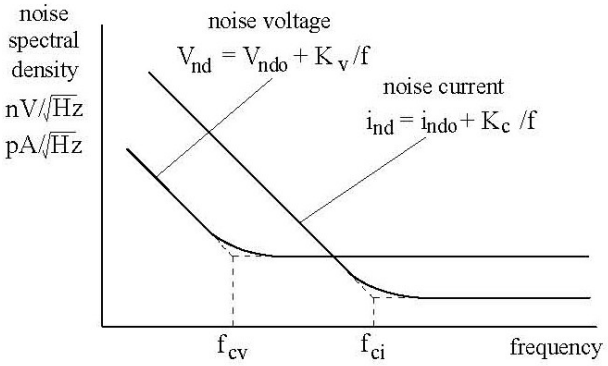

Fig. 5 Typical op-amp noise spectral densities.

The corner frequencies, f_{cv} and f_{ci}, usually lie within the ECG signal spectrum and a knowledge of these is required as well as the white noise values, v_{ndo} and i_{ndo}, to allow an accurate estimation of the output noise voltage. Integrating these profiles over the frequency range f_L to f_H gives:

$$v_{na}^2 = v_{ndo}^2\left[(f_H - f_L) + 2f_{cv}\ln\left(\frac{f_H}{f_L}\right) + f_{cv}^2\left(\frac{f_H - f_L}{f_H f_L}\right)\right] \quad (10)$$

and

$$i_{na}^2 = i_{ndo}^2\left[(f_H - f_L) + 2f_{ci}\ln\left(\frac{f_H}{f_L}\right) + f_{ci}^2\left(\frac{f_H - f_L}{f_H f_L}\right)\right] \quad (11)$$

These expressions can be evaluated and the results substituted into eq.9 to determine the output noise voltage, which can then be referred to the amplifier input by dividing by the gain. If the rms noise level is to remain at least 20dB below the minimum signal level of 100μV, then the input referred noise voltage must be less than 10μVrms.

E. Parasitic capacitance and stability considerations

Stray capacitances are present at the op-amp input terminals due to structural parasitics. They cause poles and zeros to occur in the amplifier frequency response which, if not neutralised, can affect the performance of the system by reducing stability or causing peaking in the response [7]. The effect of parasitic capacitance must be considered in the design of each stage of an instrumentation amplifier.

Stray capacitances appear at the non-inverting inputs of the pre-amplifier front-end in parallel with the common-mode input impedances, Z_{c1} and Z_{c2} , as illustrated in Fig. 6.

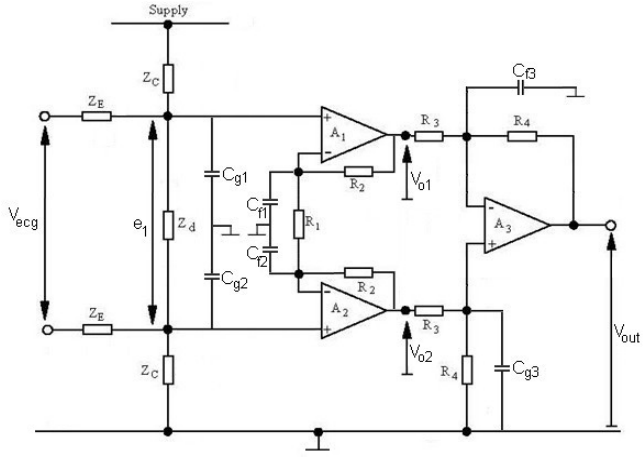

Fig. 6: A standard instrumentation amplifier including op-amp input stray capacitances.

Stray capacitances at the non-inverting inputs add a pole in the frequency response as described by eq.12 and eq.13.

$$\frac{e_1}{V_{ecg}} = H_0\left(\frac{1}{1+s\tau_0}\right) \tag{12}$$

with

$$\tau_0 = Z_E C_g H_0 \tag{13}$$

If the value the amplifier input impedance satisfies the condition specified by eq.4, then H_0 as defined in eq.1 can be closely approximated as unity.

In addition, it is the case that stray capacitances at the inverting inputs of op-amps A_1 and A_2 introduce a zero in the loop gain of the differential stage depending on the value of the feedback resistor, R_2 and the differential gain, A_{d1}:

$$\frac{V_{o1}-V_{o2}}{e_1} = A_{d1}(1+j\omega\tau_1) \tag{14}$$

with

$$\tau_1 = \frac{2R_2C_f}{A_d} \tag{15}$$

In the differential-to-single-ended stage it can be seen that input stray capacitances and their mismatch alter the final closed-loop gain. The output voltage can be expressed as follows:

$$V_{out} = \left[\frac{R_3+\frac{R_4}{1+sR_4C_{f3}}}{R_3+\frac{R_4}{1+sR_4C_{g3}}}\frac{R_4}{R_3(1+sR_4C_{g3})}\right]V_{o1} - \left[\frac{R_4}{R_3(1+sR_4C_{f3})}\right]V_{o2} \tag{16}$$

The capacitances C_{g3} and C_{g4} must be matched and limited to relatively small values to keep the poles outside of the amplifier's operating bandwidth. Consequently, the final output of a non-compensated instrumentation amplifier with N differential gain stages can be expressed as:

$$V_{out} = \frac{R_4}{R_3}\frac{\prod_{i=1}^{N} A_{di}(1+j\omega\tau_i)}{(1+s\tau_0)(1+j\omega R_4C_{g3})}V_{ecg} \tag{17}$$

with

At each stage of the instrumentation amplifier, it is important to asses whether the frequency locations of the poles and zeros affect the stability and phase margin of the system. Usually, values of phase margin lower than 45 degrees may produce peaking in the frequency response. Stability can be preserved if the poles and zeros generated by parasitic capacitances are maintained at least a decade above the amplifier closed-loop bandwidth. If this condition is not guaranteed, instability may be experienced.

III. CIRCUIT OUTLINE

A schematic diagram of the preamplifier designed by the authors is shown in Fig.6. It is a very low-power circuit operating from a single 3V supply. The specified input signal level ranges from 100μV-10mV. The amplifier consists of two differential-input-differential-output stages followed by a differential-to-single-ended stage. The operational amplifiers used were selected from the MAX400 series (Maxim Inc.), chosen for its extremely low power consumption, the quiescent current being typically 1μA per op-amp.

The front-end differential stage of the amplifier is ac coupled via capacitors C_1 and C_2, which provide a low-frequency response which does not cause phase distortion of the ECG signal. Resistors R_1 and R_2 limit transient current spikes or the current due to fault conditions which may reach the subject. The dc bias voltages required for single-supply operation are provided by resistors R_5, R_6 and R_7. The bias voltages are fed to both inverting and non-inverting sides of the op-amps A_1 and A_2 so that the output dc voltages are the same as those at the input of each op-amp. The resistors R_3 and R_4 are used to define the input impedance on each side of the amplifier. The lower ends of these resistors are connected to either side of resistor R_6 which receives positive feedback from the outputs of op-amps A_1 and A_2 via resistors R_8, R_9, R_{10} and R_{11}. This has the effect of making the magnitude of resistors R_3 and R_4 appear much higher at the amplifier inputs, which allows the requirement of very high input impedance to be met without the use of unduly large values of resistors. The transfer function of this first stage for a differential input signal, $V_{id} = V_1 - V_2$ is given as:

$$\frac{V_{o1}(s)}{V_{id}(s)} = \left[1+\frac{R_{10}}{R_8+\left(\frac{R_5R_6}{2R_5+R_6}\right)}\right]\left[\frac{sC_1\left(\frac{R_cR_d}{2R_c+R_d}\right)}{1+sC_1\left(\frac{R_cR_d}{2R_c+R_d}\right)}\right] \tag{18}$$

where R_c and R_d are the common-mode and differential-mode input impedances, respectively given by:

$$R_c = R_3\left[\frac{R_8 + \frac{R_5(R_6+R_8)}{R_5+R_6+R_8}}{R_8}\right]\left[1+\frac{R_5}{R_6+R_8}\right] \qquad (19)$$

and

$$R_d = R_3\left(1+\frac{R_8}{R_5}\right)\left[2+\frac{R_6(R_8+R_5)}{R_5R_8}\right] \qquad (20)$$

The mid-band gain of the first stage is 2dB. The second term of eq.19 describes the frequency dependence of this stage and the value of C_1 is chosen to give a pole at a frequency of 0.002Hz, which counteracts the effect of a zero in the transfer function of the second stage.

The only drawback of this stage is the fact that the input offset voltages of the op-amps appear augmented at their outputs by a factor which is much higher than the mid-band gain of the stage.

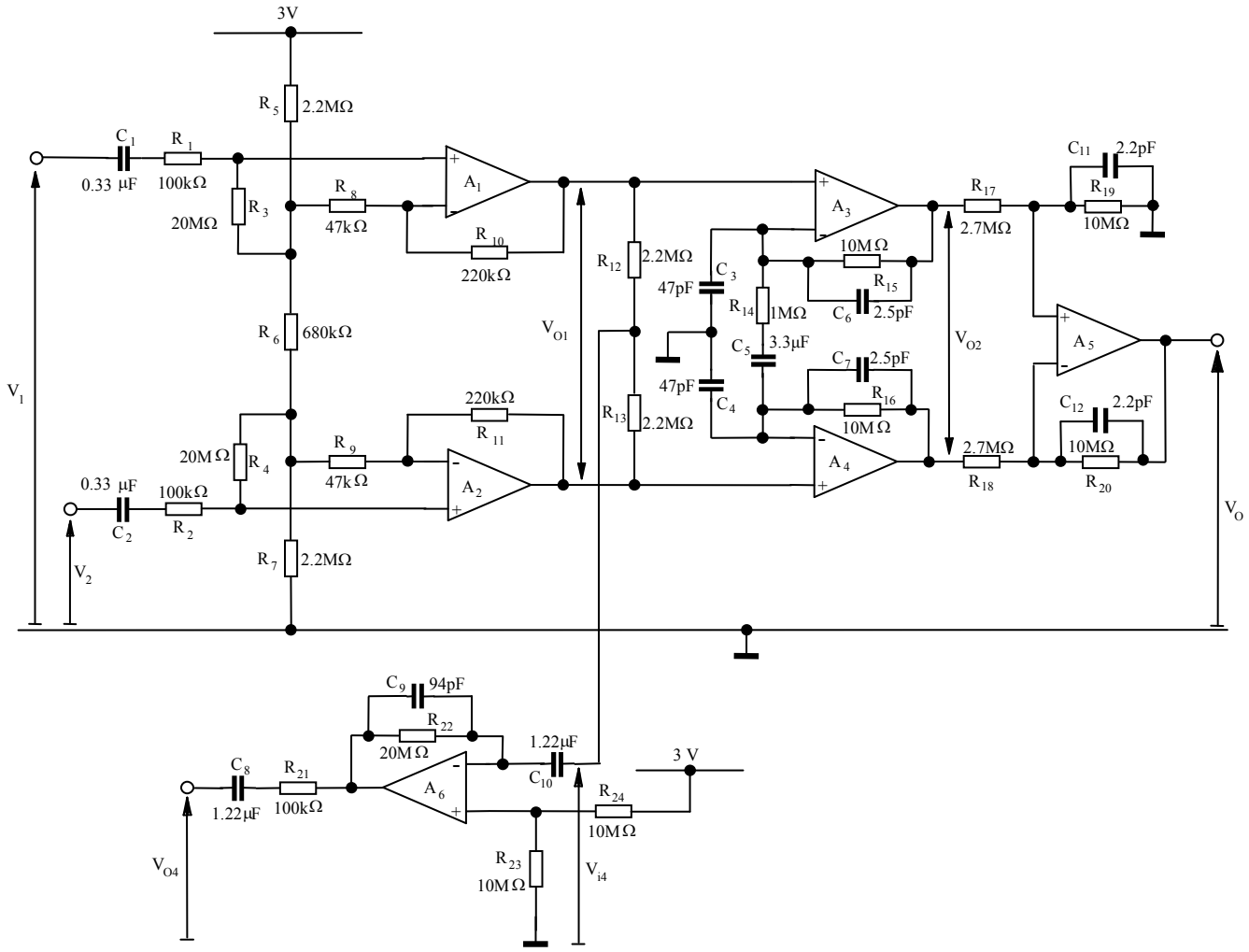

Fig. 6 Schematic diagram of the preamplifier.

If the input offset voltages of op-amps A_1 and A_2 are of equal magnitude and opposite polarity, $\pm V_{osi}$, and the mismatch in bias currents is i_b, it can be shown that the magnitude of the differential output offset voltage of the first stage is quantified as:

$$V_{oso1} = \left(1 + \frac{R_5 + R_{10}}{R_8}\right) V_{osi} + i_b R_3 \left[1 + \frac{R_{10}}{R_8} + \frac{R_5 R_6}{R_8 (2R_5 + R_6)}\right] \quad (21)$$

This offset essentially receives unity gain in the second stage and a limited gain in the final stage. Consequently, the op-amps used as A_1 and A_2 must have low-input offset voltages and the bias currents should also be as low as possible.

The second stage of the amplifier is also a differential-input stage. This stage is dc coupled at the input, but the resistor-capacitor combination R_{14} and C_5 limits the dc gain to unity. The appropriate choice of component values allows the combined low-frequency response of the first and second stages to be that of a single pole at 0.05Hz, thus avoiding phase distortion of the signal. The differential gain of the second stage is given as:

$$\frac{V_{o2}(s)}{V_{o1}(s)} = 1 + \frac{2sC_5R_{15}\left(1 + s\frac{1}{2}C_3R_{14}\right)}{(1 + sC_6R_{15})(1 + sC_5R_{14})} \quad (22)$$

It was discovered during the design process that the input capacitances of the op-amps A_3 and A_4 introduce a zero into the high frequency response of this stage, giving rise to an unwanted peak in the response. In order to overcome this, capacitors C_3 and C_4 were added at the op-amp inputs to define the zero more reliably. The capacitors C_6 and C_7 are therefore included across resistors R_{15} and R_{16} to introduce a pole which cancels this zero by making $2C_6R_{15}=2C_7R_{16}=C_3R_{14}=C_4R_{14}$. This eliminates the peak in the high frequency response of the second stage. The mid-band gain of the second stage is $1+2(R_{15}/R_{14}) = 25.6$dB. The final output stage of the amplifier is a differential-to-single-ended stage which is dc coupled, with a gain given by $R_{19}/R_{17}=3.5$dB.

The overall CMRR of the amplifier is increased by the use of a driven common electrode, previously suggested by Winter and Webster [8]. Resistors R_{12} and R_{13} sense the common-mode output signal from the first stage of the amplifier. This is then inverted and amplified in the stage built around op-amp, A_6 and is then fed back to the common electrode via resistor, R_{21} and capacitor, C_8. This signal is therefore effectively subtracted from the common-mode interfering signal present at the amplifier input and has the effect of increasing the rejection of common mode input signals by a factor equal to the gain of the inverting stage. The transfer function of this stage is given as:

$$\frac{V_{o4}(s)}{V_{i4}(s)} = -\frac{\dfrac{s}{\left(\frac{1}{2}C_9R_{12}\right)}}{\left(s + 1/C_9R_{22}\right)\left(s + 1/\frac{1}{2}C_{10}R_{12}\right)} \quad (23)$$

with a mid-band value of 30dB. The lower cut-off frequency was 0.2Hz while the higher cut-off frequency was limited to 85Hz to maintain stability.

IV. Performance

A. Frequency Response

Simulations of the circuit were carried out using PSpice during design of the amplifier whilst actual measurements were performed using a signal analyser (Agilent 35670A). Plots of the simulated and measured gain and phase of the amplifier are shown in Fig. 7 and Fig. 8. Variations between simulations and measurements can be explained by differences in the value of the gain-bandwidth product between the modelled parts and the actual MAX406 op-amps.

The measured 3dB bandwidth of the amplifier extends from 0.05Hz to 1.7kHz, with a mid-band gain of 42dB. The high frequency response of the amplifier is limited by the properties of the op-amps and any further bandlimiting may be implemented in a subsequent amplifier.

The CMRR obtainable is in excess of 85dB in the frequency range 0.5Hz to 85Hz and it is reduced outside of this range. The estimated current drawn from a 3V supply is 6.8μA, giving a power consumption of 20 μW.

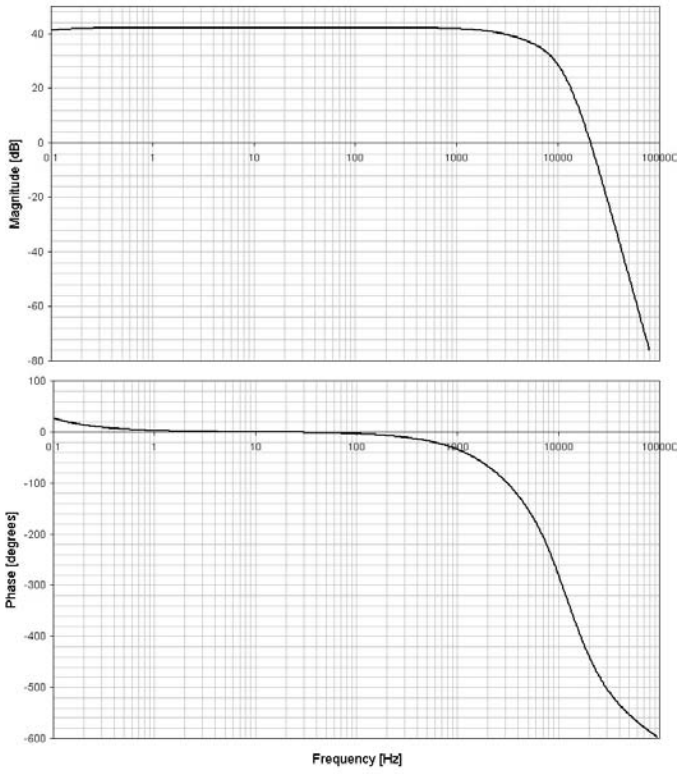

Fig. 7 A plot of the simulated magnitude and phase response of the preamplifier.

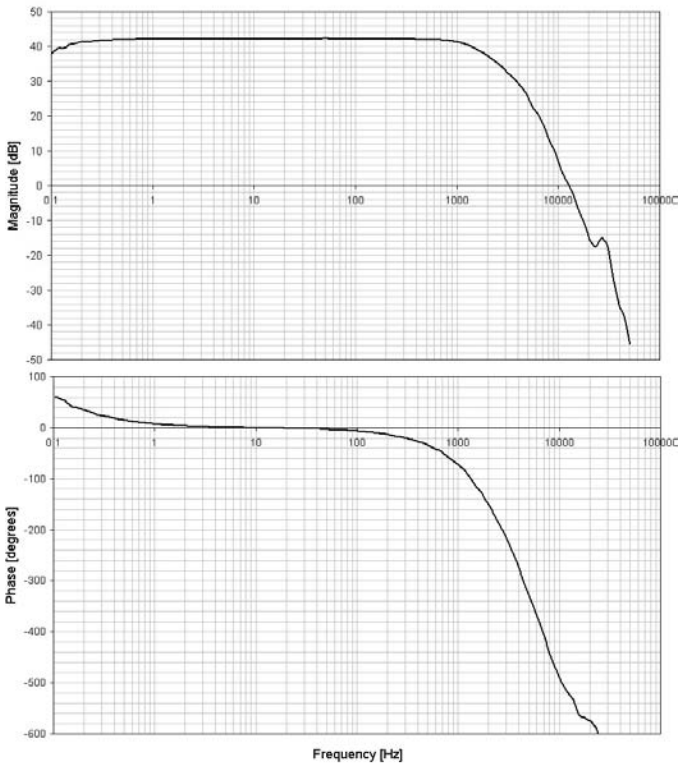

Fig. 8 A plot of the measured magnitude and phase response of the preamplifier.

B. ECG Measurement

A plot of an ECG signal recorded from an individual using pasteless electrodes mounted in an elasticated vest is shown in Fig. 9. The signal quality is considered reasonable for diagnostic purposes

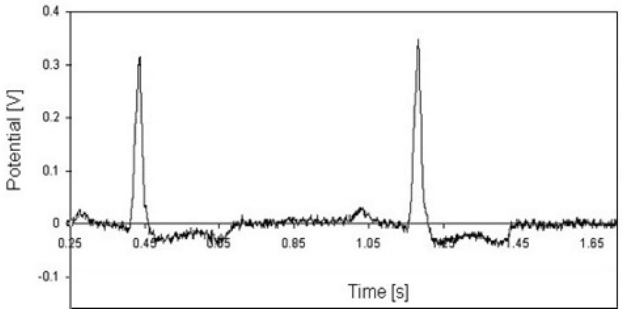

Fig. 9 A plot of a recorded ECG signal

V. CONCLUSION

The pre-amplifier presented meets the requirements of the American Heart Association for electrocardiographic equipment. The amplifier has very low power consumption and can easily be constructed using surface mounted components and powered from a small button cell battery so that the entire amplifier may be mounted on an elasticated belt or vest worn by the user.

This makes it ideally suitable for use with portable electrocardiographic equipment and heart rate monitoring instrumentation.

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