Hardware Implementation of BLDC Motor and Control System Diagnosis

Robert I. Lorincz, Mihai E. Basch, Ivan Bogdanov, Virgil Tiponut, Adrian Beschieru

Abstract: - In today's automotive applications the usage of BLDC (Brushless DC) motors is becoming very popular because of its advantages over the DC motors. For automotive applications the permanent fault diagnosis and protection of the BLDC motor and control system is mandatory. This paper presents several concepts for extensive diagnosis implementation for different fault conditions that may appear in the BLDC motor or its control electronics (the three phased bridge inverter and control ASIC). The detectable failure conditions by the methods described in this paper are: short circuit conditions at the motor terminals (short to battery, GND or even short between the phase terminals); internal, external power supply voltages and over-temperature failure conditions; position, hall signals failure conditions. The implementation is done using hardware circuits which can be easily integrated in the BLDC motor control ASIC (Application Specific Integrated Circuit).

Keywords— Automotive applications, BLDC, Diagnosis, Three phased inverter;

I. Introduction

In automotive applications the use of DC or BLDC motors for fan, pump or actuator applications is very common with the trend of replacing the conventional DC with BLDC motors.

The BLDC motors are controlled using three phased power inverter circuits as presented in Fig.1. In this example the power inverter switches are implemented using MOSFET's (Metal Oxide Semiconductor Field Effect Transistor) controlled by a motor driver ASIC circuit. This motor driver ASIC communicates with the system microcontroller via a serial interface (e.g. SPI Serial Peripheral Interface).

A large number of papers have been published regarding the motor construction, driving methods, initial rotor position sensing and the control electronics [26][28]. A comprehensive overview of these methods is presented in [1]. A few of them treats the diagnosis of the BLDC motor and the electronic control system. In a typical application the extensive diagnosis of the BLDC motor or the electronic control circuit is not needed, most of the cases only a simple short circuit protection circuit is implemented [2][3][27].

In almost all automotive application detection of fault conditions of the BLDC motor and the control electronics is mandatory. The control electronics must identify any fault condition and then apply counter measures to protect the system. The detected fault condition is reported to the system microcontroller and it is accessible via the diagnosis interface of the automobile for further service investigations [3].

For an advanced automotive application the following diagnoses of the BLDC motor and control system are required:

- Short circuit to GND (SCG) at U, V or W;
- Short circuit to battery (SCB) at U, V or W;
- Short of the load (SCL);
- Open Load (OL);
- Weak short circuit (WSC);
- Supply voltages monitoring (battery supply, logic supply, ASIC internal charge pump over and under voltage failure condition detection);
- ASIC internal logic clock;
- HALL sensors (pattern and sequence errors);
- Power inverter MOSFET's over temperature;
- BLDC controller ASIC over temperature;

In most of the BLDC motor driver ASIC's the short circuit conditions are detected using VDS monitoring of the bridge MOSFET and overcurrent detection sensed in the motor current measurement circuit. These measures protects the driver circuit against most of the above mentioned failures (SCB, SCG, SCL and OL) however not all of them are covered with 100% detectability coverage and in most of the cases the system stops, indicating a failure on a single error output line/bit, without clearly indicating the failure root cause to the system microcontroller.

The next sections of this paper present the state of the art of the existing failure detection methods and propose an implementation concept for an advanced diagnosis system for BLDC motor control electronics implemented in an ASIC, based on existing and new methods introduced with this paper.

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II. BLDC MOTOR CONTROL ASIC

This section describes the main parts of an advanced BLDC motor controller ASIC. The diagnosis block is a subpart of this ASIC dealing with the fault condition detection only. Fig. 1 presents the block diagram of an advanced BLDC motor control ASIC [5]-[13], [23]-[25]. This ASIC contain several sub-circuits each dealing with a specific functionality implemented in the chip. There are three identical driver blocks which drives the gates of the half bridge MOSFET's using constant current sources obtaining a very precisely controlled switching time. The high gate voltage necessary to open the high side power MOSFET's is provided by a charge pump unit supplied from the main battery supply ($+V_{BATT}$). The current through the BLDC motor is sensed by amplifying the drop voltage on the external shunt resistor RS. The waveform of the voltage across the shunt is identical to the BLDC motor current shape during the ON phase of the control PWM. The current measurement block uses a Sample & Hold stage which is synchronized with the middle of the ON phase of the PWM drive signal thus sampling the average value of the BLDC motor current [4]. This current measurement path is also used to detect overcurrent and short circuit conditions. The evaluation of the voltage at the current measurement output (CS_OUT) can be used by the software as primary failure detection. The driving of the BLDC motor is done via the direction and phase control unit containing the block commutation look-up table and having as inputs the three hall signals (HALL1, HALL2 and HALL3), the direction input control signal and PWM used to control the motor speed and torque. This block has as output signals the actual rotation direction of the BLDC motor and the CCS (Cycle Count Signal, each hallx signal transition generates a transition on this line). The control interface of the ASIC is composed by the SPI interface and a disable block. Via the SPI interface the ASIC operational mode can be configured by the system microcontroller (e.g. bridge enable, gate charge current strength, dead time, diagnosis configuration etc.) and the diagnosis bits can be read (like faults, forced disabled state etc.). The disable unit controls the bridge state in case of failure detection or in case of external emergency interruptions. The ASIC contain several diagnosis functions/blocks (from Fig. 1 the yellow units monitors the BLDC motor and the orange units the control ASIC itself), detailed description and implementation concepts of these are presented in the next sections.

III. BLDC MOTOR DIAGNOSIS CONCEPTS

Several diagnosis units are described in this chapter, each of them dealing with the supervising of a particular operating condition of the BLDC motor, ONSM (ON State Monitoring) and OFSM (OFF State Monitoring).

A. BLDC motor ONSM diagnosis unit

During the motor operation, for automotive applications the detection of short conditions is mandatory. There are several

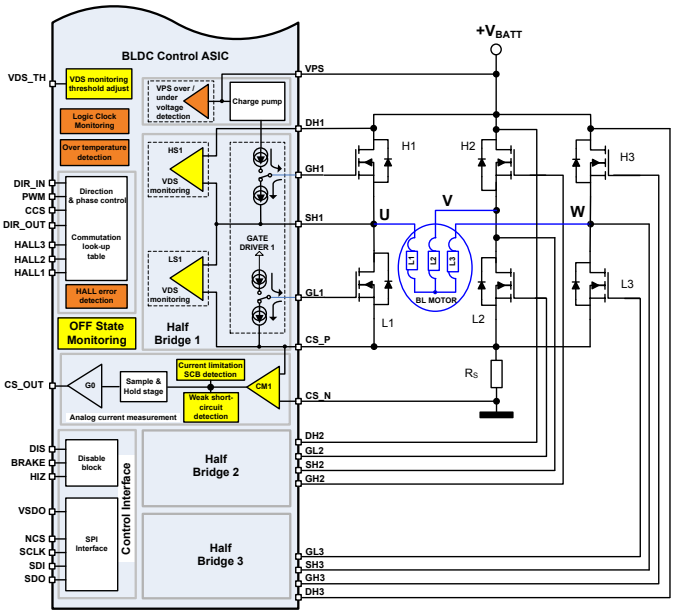

Fig. 1 BLDC motor control ASIC block diagram and external connections

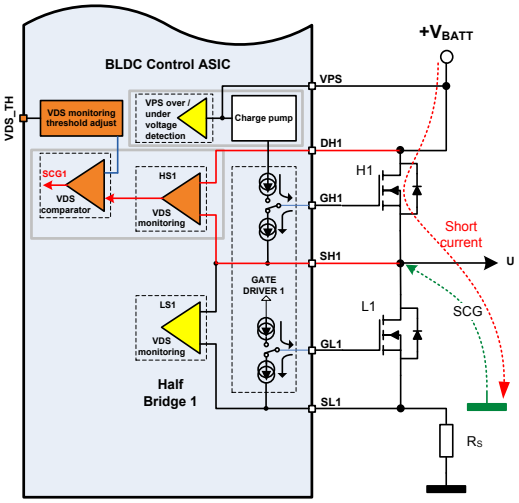

Fig. 2 SCG detection method
*with red color the failure detection circuit blocks are highlighted

short circuit conditions which have to be considered (SCB, SCG, SCL and WSC), each of them being detected using different methods as described in the next sections.

SCG detection mechanism during ONSM

Short circuits to GND are detected monitoring the voltage drop across the high side MOSFET drain to source (the classic VDS monitoring) [10]. Fig. 2 presents the short circuit current path and the detection mechanism. The voltage drop across the high side MOSFET drain to source is applied to a voltage reference shifter, which provides the HS (High Side) VDS drop voltage regarded to GND then this voltage is compared to a threshold voltage (VDSTH) using a comparator circuitry. In case the MOSFET VDS voltage exceeds this threshold the short condition is detected and the default reaction of the ASIC is to shut down the power MOSFET's to avoid further damage to the system due to the high short current. The SCG detection

current threshold can be expressed as follows:

$$I_{SC} \geq \frac{VDS_{TH}}{R_{DS\_ON}} \quad (1)$$

- where with ISC denoting the short detection threshold and RDS_ON the MOSFET drain to source ON resistance.

The disadvantage of this method is that the RDS_ON of a MOSFET have a very large dependency on a various parameters as VGS voltage, drain current, operating temperature etc. Having high enough gate voltage to ensure a full open of the MOSFET the RDS_ON is mainly temperature and initial tolerance dependent. It changes from 0.75 (at -40°C) to 1.8 (at +175°C) normalized value of the RDS_ON referenced to 25°C [14][15]. According to "(1)" the short detection threshold will also change, Fig. 3 presents the normalized short detection threshold over temperature (considering the RD_SON tolerance and 2% tolerance for the detection reference voltage accuracy) where it can be seen that the detection threshold decreases with the increase of the MOSFET die temperature due to the increase of its RDS_ON. To cope with this issue the short detection threshold current should be calculated for RDS_ON of the MOSFET at high temperatures. In case we have a SCG condition combined with low die temperature, we can have the situation that the actual short current does not exceeds the short detection threshold due to the low RDS_ON. However the short current will cause the MOSFET die temperature to increase due to the increased power dissipation, and the RDS_ON and its VDS voltage will exceed the SCG detection threshold and the failure will be detected.

The second and third half bridges are protected with the same concept, therefore the circuit is implemented three times inside the ASIC.

SCB detection mechanism during ON-state

There are two possible ways to detect SCB (Short Circuit to Battery) conditions based on the block schematic presented in Fig .1.

The first method is by using the VDS monitoring of the low side (LS) MOSFET similar to the HS MOSFET VDS monitoring for SCG condition detection (concept presented in Fig. 4). The LS (Low Side) VDS monitoring suffers the same temperature and tolerance limitation as the HS VDS monitoring. However in case of SCB conditions another more accurate detection method can be applied using the drop voltage on the current measurement shunt resistor. This SCB failure detection concept is presented in Fig. 5. The voltage across the shunt resistor is applied to a repeater amplifier with differential input (to eliminate any internal ASIC GND and external GND shift effect) the output voltage of this is then compared to a threshold voltage (SCB_TH). In case the drop voltage on the shunt exceeds the SCB_TH failure condition is detected and the ASIC default reaction is to disable all the power MOSFET's and signal the error to the system

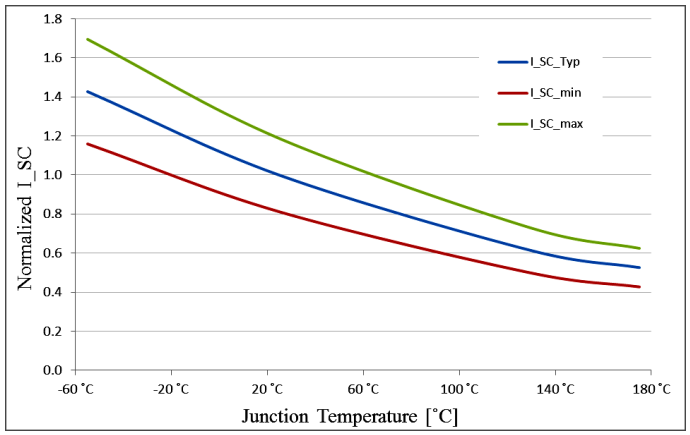

Fig. 3 Normalized VDS monitoring threshold VS MOSFET die temperature

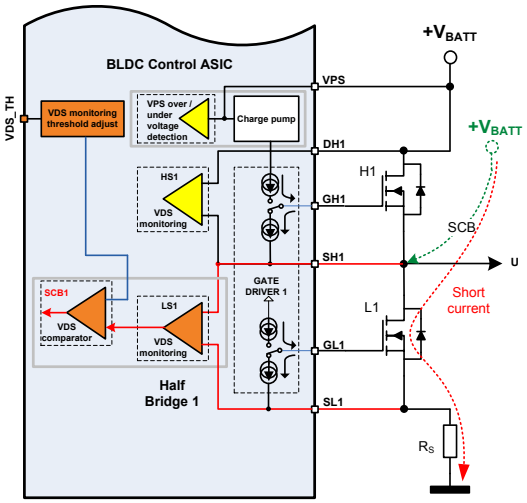

Fig. 4 SCB detection method using V_{DS} monitoring of LS MOSFETs

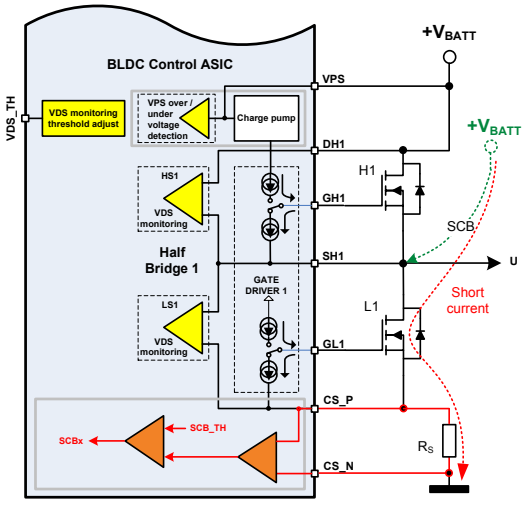

Fig. 5 SCB detection method using the current measurement path

microcontroller. The SCB detection threshold of this concept is much more accurate, it depends only on the tolerance of the shunt resistor, comparator and its threshold voltage, "(2)".

$$I_{SCB} \geq \frac{SCB\_TH}{R_S} \quad (2)$$

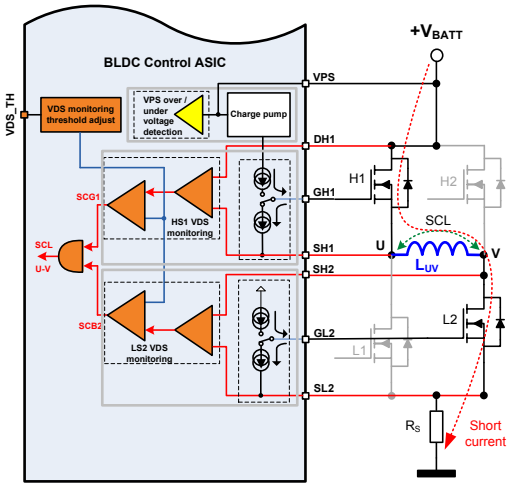

Fig. 6 SCL detection method using V_{DS} monitoring

The advantage of this concept is that this detection circuit needs to be implemented only once. The discrimination between SCB_U, SCG_V or SCB_W is done knowing the active LS MOSFET in the moment of the failure.

An advanced BLDC motor driver ASIC shall contain both SCB detection circuits to increase its versatility. Since not all of the applications require the BLDC current measurement. For those applications the SCB condition detection is done using the less accurate VDS monitoring of the LS MOSFET's. In applications where the BLDC motor current measurement is implemented, the active SCB failure detection mechanism shall be based on the current measurement path, due its better detection threshold accuracy.

SCL detection mechanism during ONSM

In SCL current flow among one HS and one LS MOSFET from different half bridges. Fig. 6 presents an example SCL between U and V phases and the implied detection circuits block schematic. The short circuit causes high drop voltage on both H1 and L2 MOSFETS triggering the short detection by their VDS, resulting SCG_U and SCB_V to be detected in the same time. The error signals are feed into an AND logic circuit which indicates the SCL condition. In the same manner shorts between V-W and U-W phases are detected. The default reaction of the ASIC would be to disable all the output MOSFETS and report the error via SPI.

The main drawback of this classic method is the fact that the actual short circuit current detection is very dependent on the MOSFET die temperature as shown in Fig. 3. It has been demonstrated that the bridge MOSFET's has no equal power dissipation, resulting a different die temperature of the MOSFET's [16]. In a real application the thermal resistance to the cooling area may not be equal for all six MOSFET's, contributing to the die temperature differences. So there are short conditions in which only a SCB or SCG is detected because the other MOSFET die temperature is lower and its VDS monitoring needs a higher current to detect it.

In the next subchapters a combined ON and OFF state monitoring solution for the SCL detection method is proposed, which is overcome these limitations.

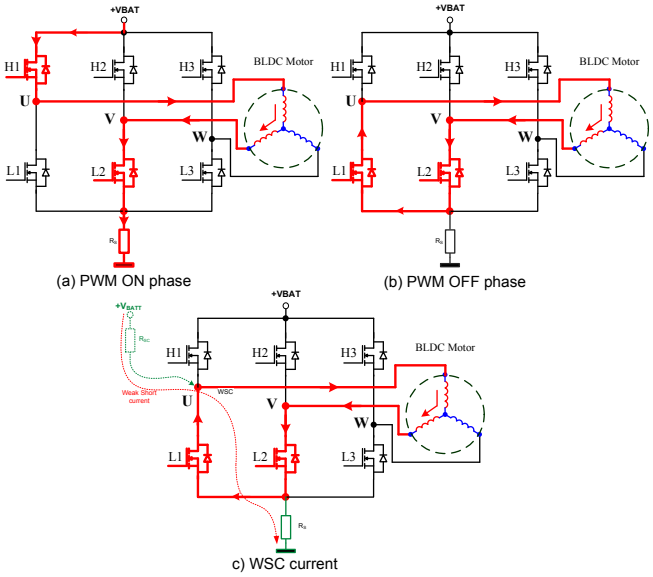

Fig. 7 Weak short circuit current path

WSC detection mechanism during ONSM

For an advanced automotive BLDC motor application it is very important to have weak short circuit detection mechanism. The intention of this WSC detection is the detection of leakage currents which are in the normal operating range of the motor, these are not detectable by the VDS monitoring or current measurement units.

In normal operation having one shunt current measurement in the DC line as presented in Fig. 1, the freewheeling current during OFF phase of the control PWM flows via two LS or via two HS MOSFET's. Fig. 7 c) presents the current path during OFF phase (freewheeling) of the PWM, phase U and V are activated, phase W is in high impedance [16]. During the freewheeling period no current flows via the shunt resistor RS, therefore any current flow must come from a WSC. The detection threshold can be set actually much lower than the maximum nominal load current of the BLDC motor itself. In a practical application the WSC detection threshold is set to around 10% of the maximum nominal motor current.

The failure detection method block circuit is similar with the one presented in Fig. 4 with the different threshold voltage (WSC_TH instead of SCB_TH). Actually this WSC detection circuit can be combined with the SCB detection circuit using the same comparator circuitry with a multiplexed threshold voltage. During ON phase of the PWM the circuit threshold voltage should be SCB_TH, detecting SCB failure conditions and during the OFF phase of the PWM WSC_TH, detecting WSC failure conditions.

Therefore the WSC detection threshold can be expressed as follows:

$$I_{WSC} \geq \frac{WSC\_TH}{R_S} \tag{3}$$

The drawback of this method is that the WSC to GND is not possible to detect and also not possible to identify at which output the failure has occurred.

B. BLDC motor OFF-state diagnosis unit

When the motor is inactive, the bridge outputs has to be monitored in order to avoid the starting of the bridge in case of failure condition, which may lead to malfunction of the system or even permanent damaging it.

With the proposed OFF state monitoring concept SCG, SCB and OL failure conditions are possible to detect.

The OFF-state monitoring mechanism block diagram is presented in Fig. 8. The circuit consists of current source at V phase output, a pull down resistance at V phase and pull down resistances at U and W phases. The resulted voltages at the terminals are compared to two thresholds, one for SCB and SCG condition detection. The circuit shall be active only during OFF phase of the bridge when al MOSFET's are turned OFF, activated by closing sw1, sw2 and sw3 switches. The diodes in the concept schematics are protecting the current sources against shorts to voltages above Vint or below GND.

In normal mode when the BLDC motor (in star connection) is connected to the bridge outputs its internal low resistance shortens all the three terminals together resulting the same voltage at each of the phases set by the current source and pull down resistances. The equivalent circuit is presented in Fig. 9, the resulting voltage at the phase terminals:

$$V_{U\_OSM} = V_{V\_OSM} = V_{W\_OSM} = \frac{R_{OSM} \cdot I_{OSM}}{2} + V_D \quad (4)$$

For a 12V battery voltage automotive application this voltage is set around 3,5V. The SCB threshold voltage (VREF_SCB) has to be over this value (e.g. 4,5V) and the SCG detection threshold (VREF_SCG) has to be below this value (e.g. 2,5V) having around 1V headroom for the short detection. When a SCB at one of the phases occur all the phase voltages will be equal with the battery voltage triggering a SCB_XOFSM to be detected at each output. In case of SCG conditions all the phase terminals will be at GND level triggering a SCG_XOSM to be detected at each of the outputs. In case of open load (OL) condition the motor windings will not shorten all three phases ending up with SCG detection at one phase and SCB at the other phase. Table 1 summarizes the OSM diagnosis result according to the failure indication.

C. OFF state and ON state motor diagnosis combined interpretation

As it can be observed none of the above described monitoring methods (ON and OFF state) can provide a full diagnosis of the BLDC motor. Combining the results from the two monitoring blocks we can have a much complete diagnosis. Fig. 10 presents the flow chart of the diagnosis using the two monitoring concepts. Table 2 summarizes the fault conditions and the final diagnosis combining the results from ONSM and OFSM.

In the final ASIC the failures shall be identified using

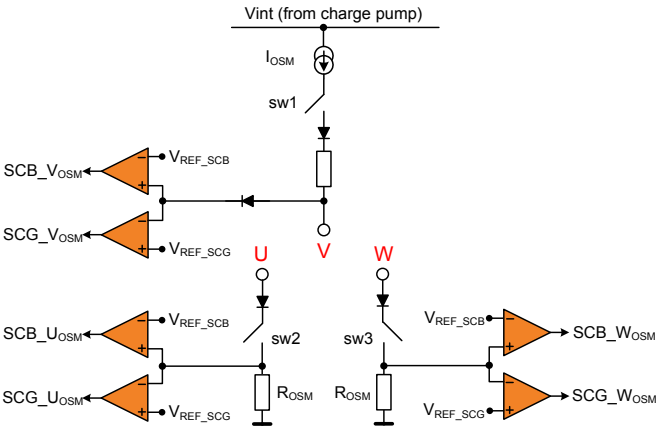

Fig. 8 OFF state monitoring circuit concept

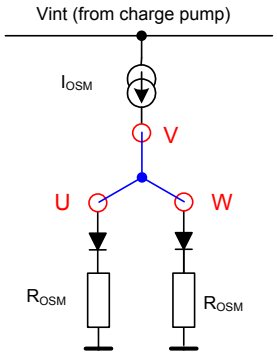

Fig. 9 OFF state monitoring equivalent circuit with BLDC motor connected

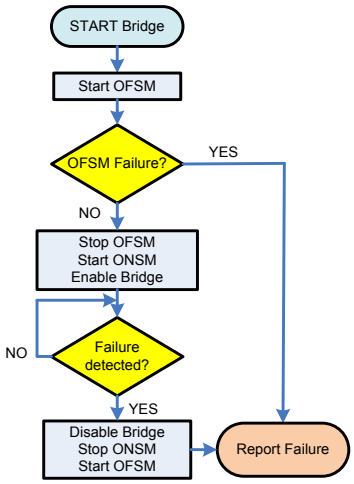

Fig. 10 Diagnosis flow chart

Table 1. OFSM diagnosis interpretation

Nr.	Failure	Final OFSM diagnosis
1	SCB_U_{OFSM} SCB_V_{OFSM} SCB_W_{OFSM}	SCB at one of the phases
2	SCG_U_{OFSM} SCG_V_{OFSM} SCG_W_{OFSM}	SCG at one of the phases
3	SCG_U_{OFSM} SCB_V_{OFSM} SCB_W_{OFSM}	Open Load at U phase
4	SCG_U_{OFSM} SCB_V_{OFSM} SCG_W_{OFSM}	Open Load at V phase
5	SCB_U_{OFSM} SCB_V_{OFSM} SCG_W_{OFSM}	Open Load at W phase

Table3 and the default reaction of the ASIC has to be the disabling of the motor control (by turning OFF all power MOSFETs of the bridge) and reporting of the failure via SPI to the system microcontroller. The SPI failure register shall have 23 latched bits to store the diagnosis result. The re-enabling of the bridge after failure has been removed must be conditioned to an error read and erase command.

IV. BLDC MOTOR DRIVER SYSTEM MONITORING UNITS

A safe and correct operation of a system which employs a BLDC motor cannot ensured only be monitoring the BLDC motor failure modes as presented in the last chapter. The key functions and operating conditions of the BLDC motor controller ASIC must also be monitored.

In this chapter the vital BLDC motor controller ASIC functions and operating conditions monitoring circuit concepts are presented, including:

- Supply voltage monitoring unit;
- Hall sensor failure monitoring unit;
- The ASIC internal clock monitoring concept;
- Overt-temperature condition detection units;

A. Supply voltages monitoring unit

All electronic systems correct operation is directly dependent on its voltage supplies. In case of an automotive application the BLDC motor controller ASIC and bridge has several external and internal supply voltages. In order to ensure the safe and correct operation of the BLDC motor all these voltages most be in their normal limits. Therefore monitoring circuits of these voltages are needed, which can detect voltage limit violations and disables the three phased inverter bridge, disabling the BLDC motor.

These voltages are:

- Battery supply voltage;
- Motor controller ASIC logic supply voltage;
- Charge pump output voltage monitoring unit;
- HALL sensor supply monitoring unit;

Battery voltage monitoring system

The most important voltage in an automotive system is the battery supply voltage. Since this is the supply voltage of the BLDC motor control system it has to be monitored for over and under-voltage conditions. If the battery voltage is too low, the BLDC motor cannot be driven up to its full power, if is below the logic supply voltage the motor controller ASIC is not able to drive the motor, therefore it is necessary to sense battery under-voltage conditions. In case the battery voltage is too high the BLDC motor can be driven over its rated power which can lead to destruction of the BLDC motor, or if the battery voltage exceeds the control circuit components maximum voltage ratings, it can lead to the control electronics destruction. Protection against these failure conditions at the battery line can be provided using two comparators (as shown in Fig. 11), one for under-voltage and second for overvoltage monitoring. The battery voltage is feed into the two comparators via voltage divider circuit realized with R1 and R2. The comparators outputs are feed into the enable logic of the bridge, disabling it in case the battery voltage is out of its limits.

Table 2. ONSM + OFSM diagnosis interpretation

Nr.	ONSM	OFSM	Final diagnosis	Comments
1	SCB_U	SCB_U_{ONSM} SCB_V_{ONSM} SCB_W_{ONSM}	**SCB_U**	short to battery at phase U.
2	SCB_V	SCB_U_{ONSM} SCB_V_{ONSM} SCB_W_{ONSM}	**SCB_V**	short to battery at phase V.
3	SCB_W	SCB_U_{ONSM} SCB_V_{ONSM} SCB_W_{ONSM}	**SCB_W**	short to battery at phase W.
4	SCG_U	SCG_U_{ONSM} SCG_V_{ONSM} SCG_W_{ONSM}	**SCG_U**	short to GND at phase U.
5	SCG_V	SCG_U_{ONSM} SCG_V_{ONSM} SCG_W_{ONSM}	**SCG_V**	short to GND at phase V.
6	SCG_W	SCG_U_{ONSM} SCG_V_{ONSM} SCG_W_{ONSM}	**SCG_W**	short to GND at phase W.
7	WSC	SCB_U_{ONSM} SCB_V_{ONSM} SCB_W_{ONSM}	**WSC**	to battery at one of the phases
8	SCB_U	No failure	**SCL_U**	Load short at U phase
9	SCB_V	No failure	**SCL_V**	Load short at V phase
10	SCB_W	No failure	**SCL_W**	Load short at W phase
11	SCG_U	No failure	**SCL_U**	Load short at U phase
12	SCG_V	No failure	**SCL_V**	Load short at V phase
13	SCG_W	No failure	**SCL_W**	Load short at W phase
14	SCB_U SCG_V	No failure	**SCL_UV**	Load short between phases U and V
15	SCB_V SCG_U			
16	SCB_U SCG_W	No failure	**SCL_UW**	Load short between phases U and W
17	SCB_W SCG_U			
18	SCB_V SCG_W	No failure	**SCL_VW**	Load short between phases V and W
19	SCB_W SCG_V			
20	No failure	SCG_U_{ONSM} SCB_V_{ONSM} SCB_W_{ONSM}	**OL_U**	Open Load at U phase
21	No failure	SCG_U_{ONSM} SCB_V_{ONSM} SCG_W_{ONSM}	**OL_V**	Open Load at V phase
23	No failure	SCB_U_{ONSM} SCB_V_{ONSM} SCG_W_{ONSM}	**OL_W**	Open Load at W phase

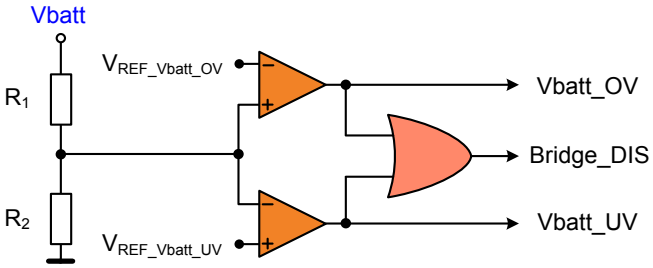

Fig. 11 Battery voltage monitoring circuit concept

Logic supply monitoring system

Almost all BLDC motor control ASIC's has at least two power supplies. One is the battery voltage and second is the

low voltage logic supply. To ensure the correct operation of the BLDC mot or controller ASIC this logic supply voltage must be between its limits. Therefore it is the necessity to supervise this voltage and in the case that is out of limits the control of the BLDC motor shall be inhibited.

The supervising circuit should be realized in the same way as the battery voltage supervisor circuit (Fig. 11) just with different over and under voltage detection thresholds.

Charge pump output voltage monitoring system

An advanced three phased inverted is built using only N channel MOSFET's for both HS and LS switches. Therefore a high voltage internal supply is needed to charge the HS MOSFETs gates to voltages above the battery voltage. In a typical automotive applications the MOSFET types used has a gate threshold voltage around 3-4V and the recommended VGS_ON voltage is around 10V, this ensures very low RDS_ON of the MOSFET when is activated [15].

There are two common implementation of this high voltage generation in the motor controller electronics. The most commonly implemented is using a bootstrap circuit which is charged during the LS MOSFET conduction and its energy used for the HS gate drive circuit [6][8]. The disadvantage of this method is that switching of the LS MOSFET must occur to generate the high voltage which limits the max PWM which can be used to drive the BLDC motor.

Another way to generate the internal high voltage is using a low power charge pump. This has a separate oscillator and generates the high voltage regardless of the bridge operation. Another advantage of such a system is that in low battery voltage conditions the full charge of the LS MOSFETs gate is still possible reducing its power consumption.

This internal voltage as described above is very important for a proper functioning of the bridge inverter, therefore any failure of it under and over voltages must be sensed and the bridge shall be disabled to prevent further damages. The fault detection circuit is again very simple, it is similar with the battery voltage supervising circuit presented in Fig. 11 just with different threshold voltages.

B. HALL sensor monitoring unit

To drive BLDC motors, using three phased inverter rotor position information is needed. This can be achieved using rotor position sensors, so called sensored drive and sensorless estimating the rotor position evaluating the phase voltages and currents.

In sensored drive mode in most of the applications hall sensors are used. The most common BLDC drive implementation is the six step, or 120° electrical commutation method which requires three hall sensor units. The displacement of these hall sensors is presented in Fig. 12. The three hall cells generate digital signal which represents the rotor electrical position with a 60° electrical resolution. The position is encoded using grey code as presented in Fig.13.

Without correct hall signals the BLDC motor cannot be driven correctly. Therefore it is a necessity to detect failure

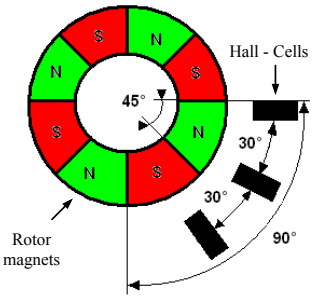

Fig. 12 Hall cells angular displacement for a four magnet poles rotor configuration

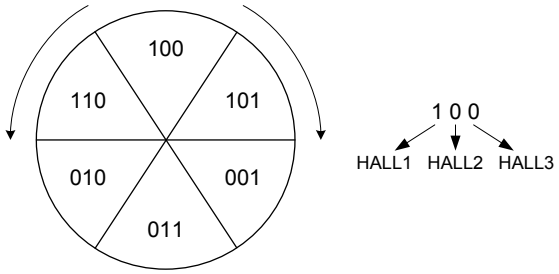

Fig. 13 Six commutation steps

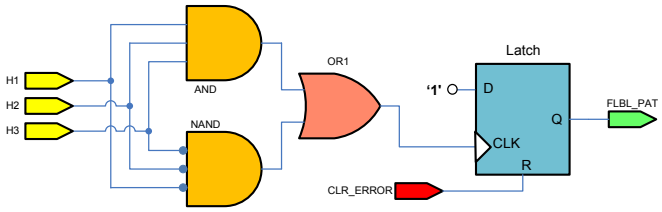

Fig. 14 Hall pattern error detection concept

Table 3. Six step block commutation encoding

HALL1	HALL2	HALL3	
0	0	0	**Invalid!**
1	0	0	Sequence 1
1	0	1	Sequence 2
0	0	1	Sequence 3
0	1	1	Sequence 4
0	1	0	Sequence 5
1	1	0	Sequence 6
1	1	1	**Invalid!**

conditions of these hall signals.

There are several failure conditions which can be detected using very simple principles:

- Hall level error;
- Hall sequence error;

HALL pattern error detection method

The encoding of the six steps of the 120° electrical commutation method is done using grey code as shown in Table 3. Having three halls sensors eight position combination can be encoded, two of these combinations '000' and '111' are not used for position encoding, these are invalid combinations. In case the control electronics detects that all hall sensors are stuck to '111' or '000' it considers it as hall pattern error.

This failure is frequently caused by the missing power supply of the hall cells or if the hall cells are damaged. For example if one hall cell is damaged and is stuck at one level (0 or 1 logic) there are combinations of the hall pattern when the

other two hall cells are at the same level as the damaged hall cell causing a hall pattern error to be detected.

The detection procedure is very simple, Fig. 14 presents the basic implementation circuit for the hall pattern error detection. It uses two logic gates, AND and NAND with three inputs. The outputs of these are feed into an OR circuit which output is connected to a latching circuit. This latching circuit provides then the hall level failure signal "FLBL_PAT". The error flag is maintained until the D Latch circuit is cleared via the "Clear error" signal. This mechanism ensures that the application software can detect not permanent level failures of the hall signals.

HALL sequence error detection method

When the hall sequence pattern is not consistent with the previous step hall sequence the failure must be detected in the control system. The grey code method ensures that from one hall sequence (pattern) to the next or previous only one hall signal changes its level, therefore when two hall signals levels are changing in the same time or with a very short time difference between them sequence error is detected.

The hall sequence error detection concept is presented in Fig. 15. It uses three transition detection units (TD1, TD2 and TD3) for each hall signals. These transition detector units generate a short pulse for each transitions of their input hall signal. The generated pulse width establishes the time interval to which two hall sensor changes is considered as sequence error. The outputs of these are feed into three AND circuits which will detect the combinations of hall transitions in the same time, the outputs of these are feed into and OR circuit which provides the hall sequence error signal, which is maintained by the lath circuit. The output of this latch provides the "FLBL_SEQ". If sequence failures occur, this latch maintains the error flag (FLBL_SEQ) until cleared by the "Clear error" signal.

Fig. 16 presents a signal flow diagram of the hall sequence error detection circuit. During time interval *t1* we have a transition at H1 hall signal, the TD1 transition detector generate a pulse with a predefined length *tp* (see TD1_OUT). During time interval *t2* we see that the second hall signal H2 also have a transition, the TD2 transition detector generates the pulse (see TD2_OUT), the two pulses does not overlap therefore no error is been detected. Now during time interval *t3* there is a transition at both hall signals H1 and H2 with a very short time difference between, which leads that the transition detectors pulses to overlap causing sequence error detection (FLBL_SEQ signal). During *t4* time interval the system microcontroller can read the error and the drive of the BLDC motor is disabled. The error is maintained by the output latch (from Fig. 15) till is cleared via CLR_ERROR signal, which happens in the Fig. 16 at the end of *t4* time interval.

The hall sequence error mainly happens in case of short circuits between two hall signals mostly caused by damage in the wiring harness of the BLDC motor or damage of the hall sensors itself.

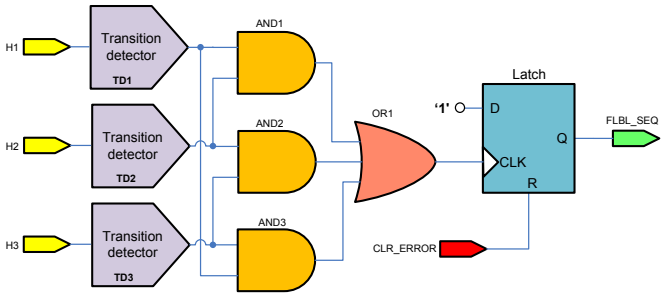

Fig. 15 Hall sequence error detection concept

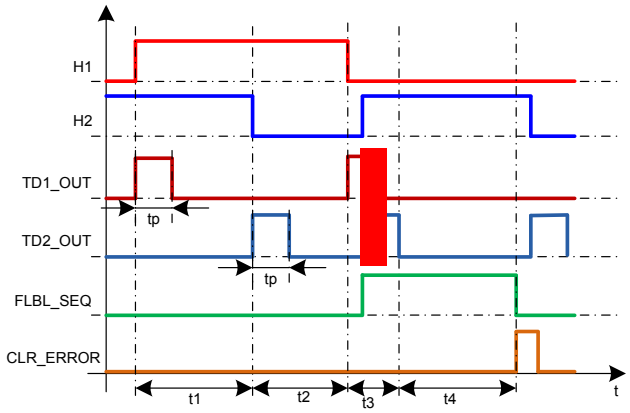

Fig. 16 Hall sequence error detection flow diagram

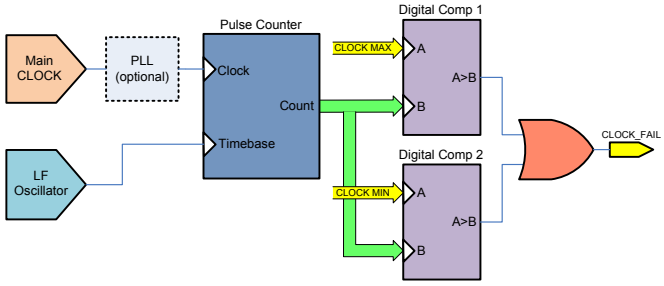

Fig. 17 Clock monitoring concept

C. Logic clock monitoring unit

All internal processes (e.g. dead time generator, SPI communication, failure detection filter time etc.) of an advanced BLDC motor driver ASIC are controlled via the internal clock and PLL (Phase Locked Loop) module. In case this clock module time base fail all internal process timing are compromised, therefore the BLDC motor cannot be controlled correctly. It even can cause damage to external components, as example if the internal clock goes to higher frequency, the dead time between HS and LS MOSFET switch will be shorted, causing their switching period to overlap which leads to high cross currents damaging the power inverter. Therefore it is very important to make sure that this clock is in its limits. In case there is a PLL unit in the ASIC it has to be guaranteed that the ASIC does not start up until the PLL is locked, in case if fails to lock than the ASIC shall remain OFF.

The detection of such failure methods is very easy to implement using a separate low frequency oscillator [19]. Than the main clock of the ASIC is then compared to this low frequency oscillator clock. The comparison can be made using

a simple frequency meter with the measurement period defined by the low frequency oscillator. In case one of the oscillators gets out of its limits, the measured frequency will also be out of limits and the failure can be detected by a simple digital comparator.

The block schematic of such a clock monitoring system is presented in Fig.17. The two clock sources generated by the Main CLOCK and the low frequency LF Oscillator outputs are feed into a counter circuit with the time base set by the low frequency oscillator. The resulted count number is then compared with two thresholds, CLOCK_MAX and CLOCK_MIN. The outputs of these are set to one logic in case the number feed into the 'A' input is higher than the number feed into the 'B' input. The two outputs of the comparators are combined together using an OR circuit at which output the CLOCK_FAIL signal is provided.

D. Over-temperature sensing

Over temperature conditions are damaging for any electronic systems. Therefore is very important to detect and protect the BLDC motor control circuit in these conditions. Basically two temperature sensing is needed in the system. One for the power inverter MOSFET block and second, for the BLDC motor controller ASIC.

Solutions for these circuits are exist in many applications and proposed in several papers. In this paper two example circuits are presented which fulfills the requirements of temperature monitoring of such BLDC motor control unit designed for automotive applications.

Bridge over-temperature sensing

Depending on the application needs the bridge temperature measurement can be done in several ways and is no need to implement it inside the BLDC controller ASIC.

The simplest way is to use a voltage divider circuit composed of a thermistor and a linear resistor as presented in Fig.18. The output voltage will change over temperature. This voltage feed into the system microcontroller ADC (Analog to Digital Converter) input the temperature can be estimated and the microcontroller will shut down the power inverter in case of over-temperature conditions. The disadvantage of this method is that the accuracy of the temperature measurement is quiet poor and may not fit to every application, nevertheless is the cheapest solution.

Another more accurate temperature measurement can be realized using the LM75 integrated digital temperature sensor presented in Fig. 19 [20]. The system microcontroller can access this chip via two wire interface. It has also a configurable integrated over-temperature detection comparator, the output of this can be connected to the system microcontroller interrupt input or to the disable logic of the BLDC controller ASIC (the OS pin of the IC).

Control ASIC over-temperature sensing

The BLDC motor controller ASIC die temperature is influencing the correct operation of the ASIC. Therefore it is

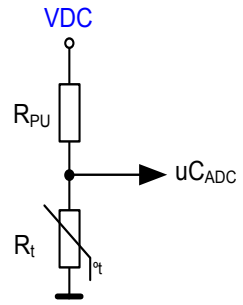

Fig. 18 Bridge temperature measurement using a thermistor

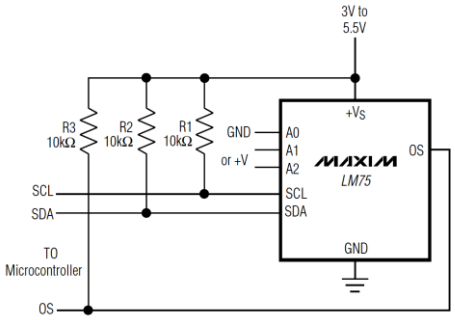

Fig. 19 Bridge temperature watchdog circuit [20]

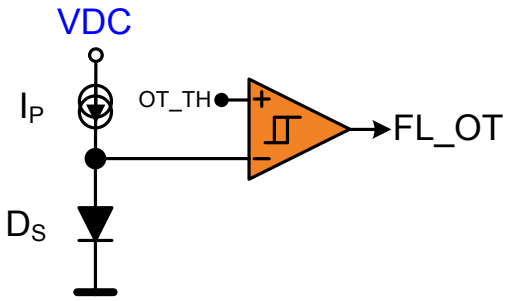

Fig. 20 ASIC over-temperature sensing circuit

necessary for automotive applications that the chip disables itself if over-temperature conditions are sensed. Since there is no need to accurately sense and disable the ASIC at a certain die temperature a very simple circuit proposal can be used, as presented in Fig. 20 [21][22].

The circuit is based the forward voltage change over temperature of a diode DS which is polarized via a constant current source IP. The voltage drop on the diode is then compared to an over-temperature threshold (OT_TH) using a comparator circuit with a small hysteresis. The output of this comparator provides the over-temperature error flag (FL_OT) which disables the ASIC.

V. Experimental Simulation Results

A. Off-state monitoring concept simulation

The evaluation of the VDS monitoring and the SCB detection circuit via the shunt is not presented in this paper, they are implemented and proved in many motor driver applications.

The simulation results (performed using OrCad PSpice v16.0) for the OFSM circuit based on the concept presented in Fig. 7 are shown in Fig. 22, having the circuit parameters:

IOSM = 1mA; ROSM = 7kΩ; Vint = 10V; VREF_SCB = 4.5V; VREF_SCG = 2.5V; Vd = 0.5V. The schematic of the used circuit for the simulations is presented in Fig. 23.

The open load conditions (OL) have been simulated using the circuit presented in Fig. 23 (only for phase U for the other phases the circuit is identical, L1 and R13 simulates the U phase winding connected in star configuration with the other two phase windings). It uses relay switches controlled by pulse generators with different pulse delay times. Fig.24 presents the short to ground and short to battery simulation circuit used in the simulations. The figure presents only for one phase U, for the other two phases the implemented circuit is the same.

The simulation results clearly prove the concept validity. During the time simulation the first three failures are simulating OL conditions at each of the phases followed by a SCG (at phase U) and SCB (at phase V) condition.

B. Supply voltages monitoring concept circuit simulation

This section demonstrates using PSpice simulations the proper operation of the concept circuit proposed for the BLDC motor controller system internal voltage monitoring systems. The simulations are only presented for the battery voltage monitoring circuit the other logic supply and charge pump monitoring units having similar configuration with different failure detection threshold voltages. The circuit used for the simulation is presented in Fig. 25. Fig. 26 presents the time simulations results where the battery voltage has been raised from 0V to 30V. It can be clearly observed that in case of under or over voltage conditions the "Bridge_Dis" signal is at high logic level. The circuit is configures to detect battery under-voltage for battery voltages below 6V and overvoltage over 27V. The circuit is designed to be supplied from a typical 5V supply (the logic supply of the BLDC motor controller ASIC) therefore the battery voltage must be divided with a factor of six, divider realized with R1 and R2 (from Fig. 25). Therefore the resulting voltage references must also be divided with a factor of six to keep the reference and battery voltage ratio to one, resulting battery overvoltage detection threshold (Vref_OV) of 4,5V and under-voltage detection threshold (Vref_UV) of 1V.

C. Hall monitoring circuits simulation results

The hall signal error detection circuits have been implemented using on a Xilinx Cool Runner II CPLD (Complex Programmable Logic Device) circuit XC2C256-TQ144 equipped on a Digilent X-board. The logic circuit design has been developed using Xilinx ISE WebPack v12.4 and simulated using ISim v8.1.

Hall pattern error detection circuit simulations

The hall signals pattern failure detection schematic circuit is presented in Fig. 27. A screenshot of the simulation results of the circuit is presented in Fig. 28.

In the simulation we can observe that in the 2ndµs of the simulation all hall signals (h1, h2 and h3) are at '0' logic level consequently the circuit detects the failure and pulls "lvl_err"

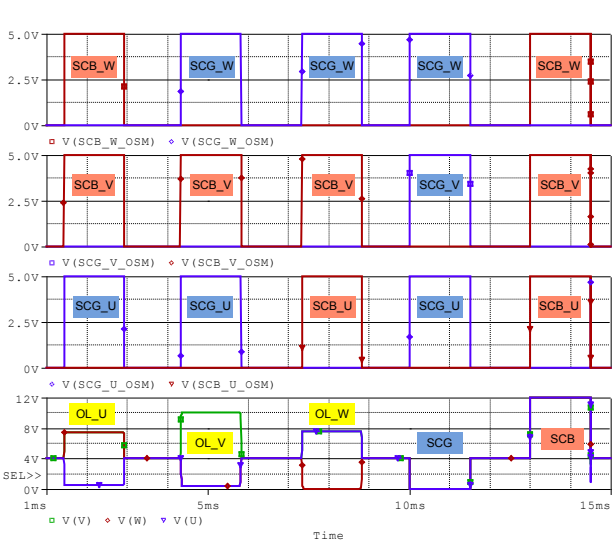

Fig. 21 OFF state monitoring (OFSM) circuit simulation results

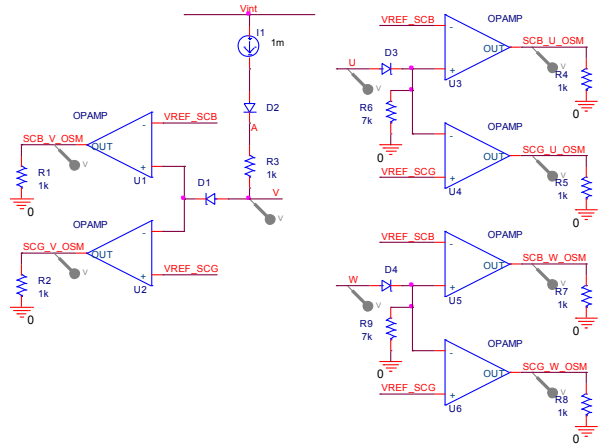

Fig. 22 OFF state monitoring circuit use in simulations

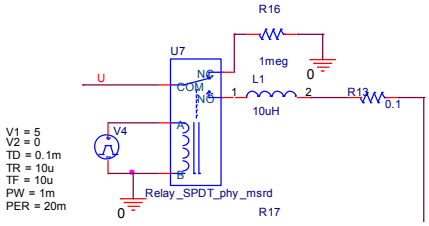

Fig. 23 Open Load (OL) failure simulation circuit

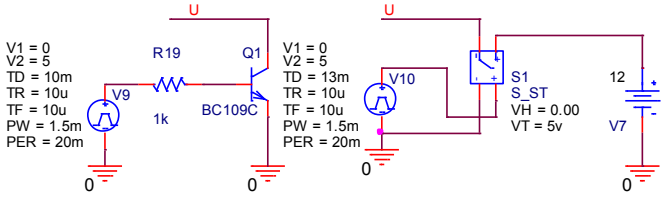

Fig. 24 Short to ground and battery simulation circuits

signal to high logic level. The error is still kept by the output latch circuit until it is cleared by the "clr_err" signal, this mechanism ensures that the system microcontroller is informed by the failure even if is for a very short time. The "clr_err" signal is controlled by the system microcontroller. At the 8thµs time of the simulation all the hall signals are at high logic level ('1'), we can observe that the failure is detected by the circuit

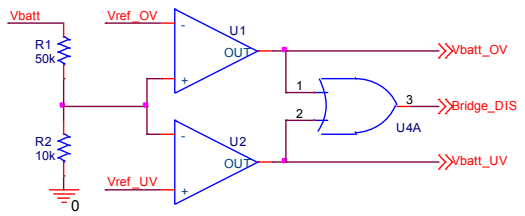

Fig. 25 Battery voltage monitoring circuit

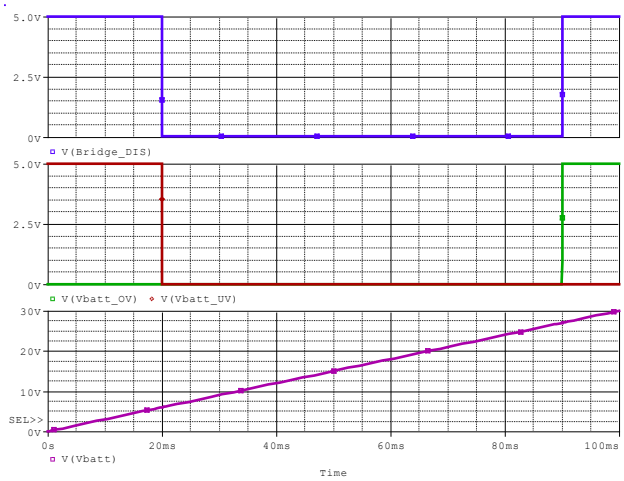

Fig. 26 Battery voltage monitoring circuit simulation results

and is clearable by the "clr_err" signal.

Hall sequence error detection circuit simulations

The hall signals sequence error detection schematic circuit is presented in Fig. 29. A screenshot of the simulation results of the circuit is presented in Fig. 30.

In the simulations we can observe that at every input hall signals transitions (h1, h2 and h3) the corresponding transition detector (td1_out, td2_out and td3_out) generates a predefined pulse equal with four clock cycles ("clk"). In case the two pulses are overlapping as we can observe at time point 9µs the sequence error has been detected, "seq_err" signal goes to high level. The error is been generated because of the too close level change of h1 and h3.

The transition detector circuit is presented in Fig. 31. It is composed by two separate blocks one for rising and second for falling transition detection of the input hall signal. The transition detection is done via the input D latches, and the output pulse is generated using a four bit counter. When the counter reaches five, the counter is cleared and the output signal toggled to '0' logic level. The generated pulse length can be adjusted by the max counter value at which the circuit is cleared.

VI. Conclusions

This paper presents an advanced hardware diagnosis implementation concept for BLDC motors. The diagnosis concept is based on two separate diagnosis systems, one for the BLDC failure conditions detection and second for the control electronics ASIC failure detection.

The diagnosis concept presents high interest for future automotive applications employing advanced BLDC motor

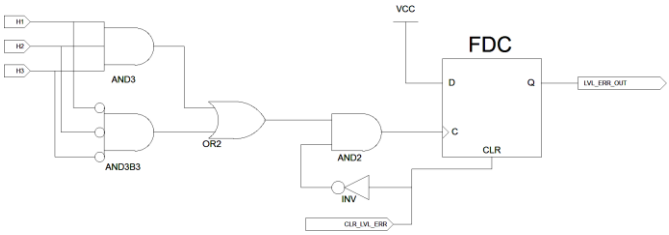

Fig. 27 Hall signals pattern failure detection circuit schematic

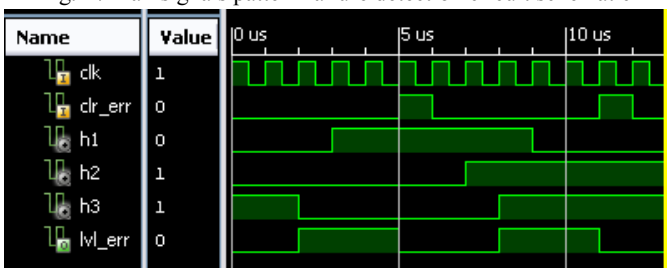

Fig. 28 Hall signals pattern failure detection circuit simulation results

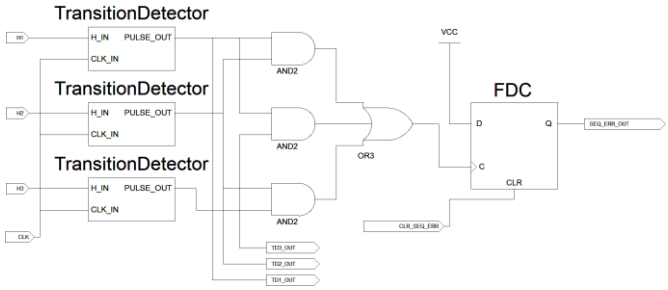

Fig. 29 Hall signals sequence failure detection circuit schematic

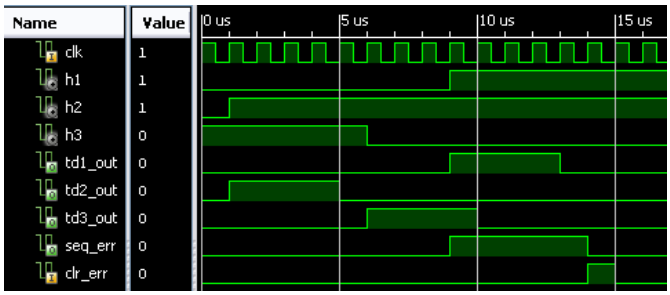

Fig. 30 Hall signals sequence failure detection circuit simulation results

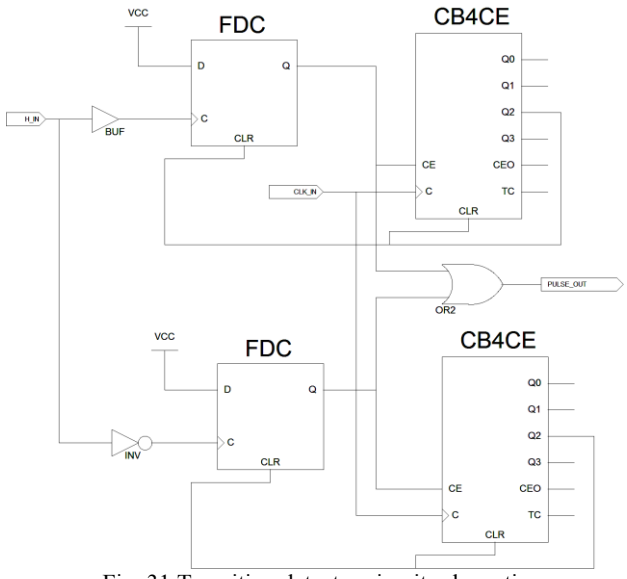

Fig. 31 Transition detector circuit schematic

Table 4 BLDC motor driver ASIC's diagnostics comparison

Diagnose	MCZ33937 [5]	A4935 [6]	TMC603A [8]	MTD6501 [9]	TLE7189 [10]	L6235 [12]	UC3625 [13]	ECN30207 [23]	TB6633FNG [24]	ATA6833 [25]	Proposed -
SCB	Yes	Yes	Yes	Yes	Yes	Yes	Yes	no	Yes	Yes	Yes
SCG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	no	Yes	Yes	Yes
OL	Yes	no	no	no	no	no	no	no	no	no	Yes
SCL	no	Yes	no	no	no	Yes	no	no	no	no	Yes
WSC	no	no	no	no	no	no	no	no	no	no	Yes
Overcurent	Yes	Yes	Yes	Yes	Yes	Yes	no	Yes	Yes	Yes	Yes
Vbatt OV	no	no	no	no	Yes	no	Yes	Yes	no	Yes	Yes
Vbatt UV	Yes	Yes	Yes	no	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Logic OV	no	no	no	no	Yes	no	no	no	no	no	Yes
Logic UV	Yes	Yes	no	no	Yes	no	Yes	no	no	no	Yes
CP OV	no	no	no	no	no	no	no	no	no	Yes	Yes
CP UV	no	Yes	Yes	no	Yes	no	no	no	no	Yes	Yes
OT	Yes	Yes	no	Yes	Yes	Yes	no	no	Yes	Yes	Yes
Hall Pattern	no	no	no	-*	no	no	no	no	-*	no	Yes
Hall Sequence	no	no	no	-*	no	no	no	no	-*	no	Yes
Logic clock	no	no	no	-*	no	no	no	no	-*	no	Yes

*sensorless BLDC motor driver ASIC therefore does not require hall sensors.

diver ASIC's. The simulation results demonstrate the validity of the proposed methods as the OFF state monitoring unit and the hall failure detection circuits.

The combination of the already existing and proposed diagnosis methods delivers a much comprehensive diagnosis report compared to existing solutions and implementations. Table 4 presents a comparison between the most representatives BLDC motor control ASIC's and the proposed one in this paper

VII. References

[1] P. P. Acarnley, J. F. Watson, "Review of Position Sensorless Operation of Brushless Permanent-Magnet Machines", *IEEE. Transactions on Industrial Electronics*, vol. 53, no. 2, April 2006;

[2] William H. Yeadon; Alan W. Yeadon, "*Handbook of Small Electric Motors*", McGraw-Hill; ISBN 0-07-072332-X, 2001;

[3] Bosch "*Automotive Handbook*", Robert Bosch GMBH, 2000;

[4] Richardson, J.; Kukrer, O.T.; "Implementation of a PWM regular sampling strategy for AC drives" *Power Electronics, IEEE Transactions on*, vol.6, no.4, pp.645-655, Oct 1991 doi: 10.1109/63.97764

[5] *Freescale Semiconductor*, "Three Phase Field Effect Transistor Pre-driver", MCZ33937datasheet, 2009;

[6] *Allegro MicroSystems*, "Automotive 3-Phase MOSFET Driver" A4935 component datasheet, 2010;

[7] *International Rectifier*, "3 Phase Controller for DC Brushless Motor", IR3230 datasheet, 2007;

[8] *Trinamic Motion Control*, "TMC603A", component datasheet, Nov. 2009;

[9] *Microchip*, "3-phase BLDC Sinusoidal Sensorless Fan Motor Driver" MTD6501 datasheet, 2010;

[10] *Infineon Technologies*, "3-Phase Bridge Driver IC" TLE7189 component specification, May 2007;

[11] *Atmel*, "Fully Integrated BLDC Motor Control" Application Note 4987A–AUTO–03/07, Mar. 2007;

[12] Vincenzo M. "L6235 Three Phase Brushless DC Motor Driver", *ST Microelectronics application note AN1625*, Oct. 2003;

[13] *Texas Instruments*, "Brushless DC Motor Controller", UC3625 component specification, 2003;

[14] Hasanuzzama, M.; Islam, S.K.; Tolbert, L.M.; Alam, M.T., "Temperature dependency of MOSFET device characteristics in 4H- and 6H-silicon carbide (SiC)," *IEEE Semiconductor Device Research Symposium, International*, Dec. 2003;

[15] *NXP Semiconductors*, "BUK765R2-40B N-channel TrenchMOS Standard Level FET", component datasheet, Jan. 2009;

[16] Lorincz R., Basch M., Tiponut V., "Improved Power Distribution Method for BLDC Motor Driving Power Inverters" Proceedings of the *IEEE 10th – ISSCS conference*, June 2011; ISBN: 978-1-4577-0201-3;

[17] Nandi, S.; Toliyat, H.A.; "Condition monitoring and fault diagnosis of electrical machines-a review," *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting*. Conference Record of the 1999 IEEE, vol.1, no., pp.197-204 vol.1, 1999;

[18] Lorincz R., Basch M., Bogdanov I., Tiponut V. "Hardware Implementation of a BLDC Motor Diagnosis" *Proceedings of the 15th WSEAS International Conference on Circuits*, July 2011; ISBN:978-1-61804-017-6;

[19] Franch, R.; Restle, P.; James, N.; Huott, W.; Friedrich, J.; Dixon, R.; Weitzel, S.; Van Goor, K.; Salem, G.;, "On-chip Timing Uncertainty Measurements on IBM Microprocessors," *Test Conference, 2008. ITC 2008. IEEE International*, Oct. 2008, doi: 10.1109/TEST.2008.4700707;

[20] *Maxim IC*, "Digital Temperature Sensor and Thermal Watchdog with 2-Wire Interface" LM75 component datasheet, Mar. 2009

[21] Ching-Che Chung; Cheng-Ruei Yang; "An Autocalibrated All-Digital Temperature Sensor for On-Chip Thermal Monitoring," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol.58, no.2, pp.105-109, Feb. 2011, doi: 10.1109/TCSII.2010.2104016;

[22] Boyle, S.R.; Herald, R.A.; "A CMOS circuit for real-time chip temperature measurement," *Compcon Spring '94, Digest of Papers*. , vol., no., pp.286-291, 28 Feb-4 Mar. 1994, doi: 10.1109/CMPCON.1994.282911;

[23] *Hitachi*, "3-Phase BLDC Motor Driver IC" ECN30207SP component datasheet, Ref. No. IC-SP-05056 R0;

[24] *Toshiba Semiconductor*, "3-Phase Full-Wave PWM Driver for Sensorless DC Motors" TB6633FNG Component datasheet, may 2010;

[25] *Atmel Corporation*, "BLDC Motor Driver and LIN System Basis Chip" ATA6834 component datasheet, 9122G-AUTO-10/10;

[26] J. Rizik, A. Warson, A. Hellany, M. Nagrial "Brushless DC Motor Control Using a Digital Signal Controller" *Proceedings of the 15th WSEAS International Conference on Circuits*, July 2011; ISBN:978-1-61804-017-6;

[27] Jader A., De Lima, Wallace A. Pimenta, "Overcurent Protection in DC/DC Converters – An Overview" *Proceedings of the 14th WSEAS International Conference on Circuits*, July 2010; ISBN:978-960-474-198-4;

[28] Chun-Fei Hsu, Chia-Yu Hsu, Chih-Min Lin, Chao-Ming Chung; "FPGA-implemented Adaptive RCMAC Design for BLDC Motors" *Proceedings of the 12th WSEAS International Conference on SYSTEMS* July 2008; ISBN: 978-960-6766-83-1