Design of Three-Stage Nested-Miller Compensated Operational Amplifiers Based on Settling Time

Hamed Aminzadeh, Khalil Mafinezhad, and Reza Lotfi,

Abstract—**Settling performance of operational amplifiers (opamps) is of great importance in analog signal-processing applications. Among different architectures, three-stage amplifiers are gaining more attention between analog circuit designers of modern technologies with small supply voltages where few devices can be stacked. Previous attempts to design and optimize a three-stage opamp based on settling time suffer from lack of a comprehensive analysis of the settling behavior and closed-form relationships between settling time/error and other parameters. In this paper, a thorough analysis of the settling response of three-stage nested-Miller-compensated opamps, including linear and non-linear sections, is presented. Based on this analysis, a design methodology is presented which determines the circuit requirements to achieve a desired settling time/error. It allows optimizations in power consumption and area based on settling time.**

Keywords- frequency compensation, nested-Miller, operational amplifier, opamp, optimization, stability, settling time.

I. INTRODUCTION

Design and optimization of multi-stage operational amplifiers (opamps) is becoming increasingly challengeable in modern IC technologies. While submicron transistors benefit from very high transient frequency, their low intrinsic gain significantly affects the linearity and the accuracy of analog circuits. The decrease in intrinsic gain is directly proportional to the scaling rate. Hence, to compensate for the effect of scaling on the accuracy of opamps, DC gain of each stage should be increased.

As the upper limit of voltage supply is continuing to decrease in each coming technology, this is no longer possible. Another solution, compatible with low-voltage environment, is to add more cascaded stages [1-9].

Frequency compensation is mandatory to stabilize a closed-loop three-stage opamp. While several solutions have been proposed [4], nested-Miller Compensation (NMC) is still a popular technique for these amplifiers. To stabilize an amplifier, NMC proposes the use of two negative capacitive feedbacks (Fig. 1a), one via C_{C1} for pole-splitting and the other via C_{C2} for damping factor adjustment of non-dominant poles [1-5]. To place the poles of closed-loop transfer function for the case of unity-feedback, the response of a third-order Butterworth filter has been considered in [1]. Although this approach leads to maximally flat band, but for a particular settling time, the technique does not guarantee minimum power consumption. Indeed, this approach fixes the values of phase margin and open-loop damping factor to 60^o and 0.7, regardless of the value of settling time/error. Phase margin has been included into the equations of [2], stating that phase margin-related equations can be used for optimization based on settling time.

The contribution of damping factor is evident in settling response of a three-stage amplifier. As a result, the relations between phase margin, damping factor and compensation capacitors are obtained in [3]. These relations give the designer the chance to change phase margin and damping factor concurrently. However, as there is no settling time in equations, it is still ambiguous how to optimize settling response.

Although settling time is often reported in the literature, a design methodology completely including this parameter is still missing. In other words, there is

Manuscript received May 30, 2009/ Revised July 24, 2009.

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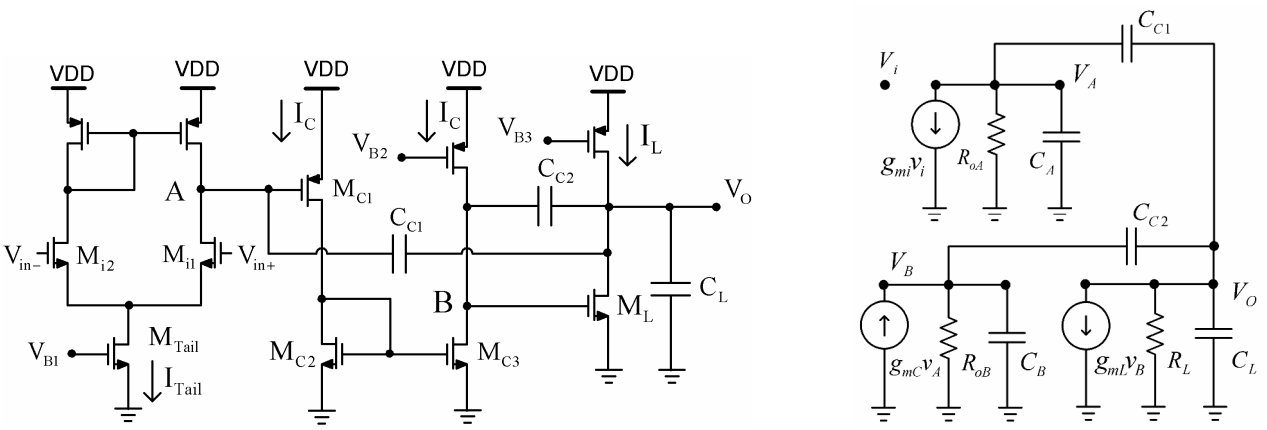


Figure 1: A three-stage single-ended nested-Miller compensated opamp (a) circuit schematics (b) small-signal equivalent

still a difficulty in design and optimization of three-stage opamps based on total settling time/error. In this paper, we will describe a thorough analysis which relates device transconductances into settling time. In addition, all the design procedures presented so far are for three-stage amplifiers in the case of unity-feedback. Although this guarantees the stability for any feedback factor less than unity, the estimations of the required power and area would be overestimated. Furthermore, in certain applications such as low-dropout regulators (LDOs), the circuit can be considered as a three-stage amplifier with feedback factor that is less than unity [15-16]. These issues make the authors to also include feedback factor into the proposed design methodology.

The design approach of this work takes into account both linear and non-linear sections of the step response to obtain accurate equations for settling time. In particular, the direct relation between bandwidth and settling time has been elaborated. Thanks this point of view, it is made possible to estimate the required bandwidth for a particular settling time. This equation plays a key role in including settling time to analysis.

The rest of the paper is organized as follows. In section II, the relationship between settling time and bandwidth, is extracted for the case of single-stage opamps. This analysis plays a fundamental role in extending the analysis into the third-order system of section III, as a more complicated case. Based on these results, a settling-based methodology is then presented in section IV. This is followed by section V and section VI which are devoted to simulation results and conclusions respectively.

II. PROPOSED ANALYSIS: SINGLE-STAGE OPAMPS

The open-loop transfer function of an amplifier with only one dominant pole at the load is as follows (see Fig. 2) [5,17]

$$A_V(s) = \frac{A_0}{1 + s/w_0} \cong \frac{GBW}{s}, \qquad (1)$$

where A_0 and ω_0 are the open-loop DC gain and -3dB angular frequency respectively. GBW represents the gain-bandwidth product where $|A_V(j\omega)|$ becomes equal to unity; i.e. $GBW = A_0\ \omega_0$. Based on the required accuracy, the closed-loop settling error $e_{SS,t}$ comprises of two terms, one originated from finite DC gain ($e_{SS,A}$) and the other from limited gain-bandwidth (e_{SS}). It can be shown that the error caused by finite DC gain is [17]

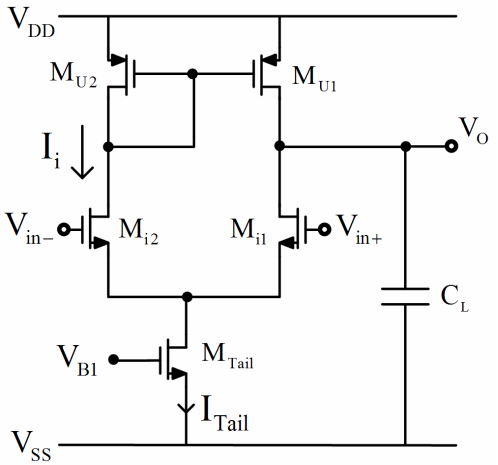


Figure 2: A single-stage telescopic-cascode opamp

$$e_{SS,A} = \frac{1}{1+A_0 b} \cong \frac{1}{A_0 b}, \quad (2)$$

where β is the feedback factor. Slewing effect divides the opamp output settling (t_S) into large-signal (t_{LS}) and small-signal (t_{SS}) regions ($t_S = t_{LS} + t_{SS}$). By taking into account both regions, the relationship between *GBW* and t_S will be [18]

$$GBW = (\frac{n}{b} + \frac{V_{Swing}}{V_{effi}}) \frac{1}{t_S}, \quad (3)$$

where V_{Swing} and V_{effi} are respectively the maximum output voltage swing and the overdrive voltage of input devices (M_{i1} and M_{i2} in Fig. 2). Argument *n*, as the time–constant coefficient, is defined as the number of required time constants in which the error of finite bandwidth becomes less than the required e_{SS}. This parameter can be expressed as follows[17,18]

$$n = \frac{t_{SS}}{1/bGBW} = \ln \frac{1}{e_{SS}} = f(e_{SS}). \quad (4)$$

Equation (3) shows, as predicted, that if the required accuracy and V_{Swing} are decreased, the needed *GBW* for a given settling time reduces.

III. PROPOSED ANALYSIS: THREE-STAGE OPAMPS WITH NESTED-MILLER COMPENSATION

Fig. 1b shows the simplified small-signal equivalent of Fig. 1a [1-4], where the transconductance values of different stages (g_{mi}, g_{mC} and g_{mL}), equivalent output capacitances (C_A, C_B and C_L) and equivalent output resistances (R_{oA}, R_{oB} and R_L) are illustrated. The transfer function of this system is relatively complicated. Nonetheless, some assumptions can be made to simplify the equations. The first assumption treats with values of C_L, C_{C1} and C_{C2} as elements which are much larger than the parasitic capacitances seen at all nodes. The second assumption considers the DC gain of all stages to be much larger than unity. As for the third assumption, g_{mL} is considerably greater than g_{mi} and g_{mC}. Under these circumstances, the open-loop transfer function can be approximated as (5) shown at the bottom of the page [1-3]. This equation can be regarded as in the following form

$$A_V(s) \cong \frac{A_0}{(1+s/w_0)(1+s(2x_0/w_{n0})+s^2/w_{n0}^2)} \cong \frac{1}{(s/GBW)(1+s(2x_0/w_{n0})+s^2/w_{n0}^2)}, \quad (6)$$

where A_0, and ω_0 are DC gain and dominant pole respectively. *GBW* is the amplifier unity gain-bandwidth frequency whose expression is as usual [1-4]

$$GBW = A_0 w_0 = \frac{g_{mi}}{C_{C1}}. \quad (7)$$

Moreover, x_0 and ω_{n0} are respectively the damping factor and the natural frequency of non-dominant poles

$$x_0 = \frac{1}{2}\sqrt{\frac{g_{mL} C_{C2}}{g_{mC} C_L}} \qquad w_{n0} = \sqrt{\frac{g_{mC} g_{mL}}{C_{C2} C_L}}. \quad (8)$$

From (8), C_{C2} role in stabilizing the circuit is revealed. Without C_{C2}, although C_{C1} dominates one pole and moves the rest to higher frequencies, but the value of damping factor might be unacceptable (as $x_0 \propto \sqrt{C_{C2}}$). As a result, the system has the potential of generate a large peak in frequency magnitude response. When this happens, undesirable time-domain transient ringing in step response is inevitable.

Based on the definition of phase margin (*PM*), (6) shows that the relationship between *PM*, *GBW* and damping factor is

$$\tan(PM) = (\frac{1-(bGBW/w_{n0})^2}{2x_0(bGBW/w_{n0})}). \quad (9)$$

As a result

$$GBW = \frac{1}{b} \frac{w_{n0}}{x_0 \tan(PM) + \sqrt{1+x_0^2 \tan^2(PM)}}. \quad (10)$$

$$A_V(s) \cong \frac{g_{mi} g_{mC} g_{mL} R_{oA} R_{oB} R_L}{(1+g_{mC} g_{mL} R_{oA} R_{oB} R_L C_{C1} s).(1+(C_{C2}/g_{mC})s+(C_{C2} C_L / g_{mC} g_{mL})s^2)}. \quad (5)$$

For constant β, ω_{n0} and PM, this equation shows that higher GBW is resulted when damping factor is lowered. However, this may not be useful in improving the speed/stability tradeoff of the amplifier because with unchanged phase margin, the relative distance between ω_{n0} and GBW is also decreased. As a result, an undesirable peak again poses in frequency domain and stability is degraded. Hence, maintaining $x_0 \tan(PM)$ beyond a threshold value is essential for stability and a lower x_0 must be compensated by a higher PM.

To propose a settling-based design methodology for three-stage operational amplifiers, the relationship between GBW and settling time (t_S) is still missing. In Fig. 1a, if the slew-rate of first stage is dominant, similar analysis as in the case of single-stage amplifiers shows that such relation is similar to (3). However, it is essential to determine the modified formula of time-constant coefficient (n) with the same definition of (4). The equivalent definition in third-order systems, however, is non-linear function of small-signal settling error, phase margin and damping factor; namely

$$n = \frac{t_{SS}}{1/bGBW} = f(x_0, e_{SS}, PM). \qquad (11)$$

For the amplifier shown in Fig. 1a, the error originated from limited gain-bandwidth (e_{SS}) can be evaluated from closed-loop damping factor (x) and natural frequency (ω_n) of non-dominant poles and also small-signal settling time (t_{SS}) [19,20]. Further analysis is required to relate open-loop and closed-loop parameters of a third-order system [6]. Appendix A is dedicated to details of the analysis leading to the exact definition. These equations along with (12) can be used to derive the exact relation of n for the amplifier. The result, represented by (11) is non-linear and can not be expressed with conventional mathematical functions. Consequently, this equation should be numerically solved for pre-assigned values of PM, x_0 and e_{SS}. For e_{SS} =0.05%, the 3D surface shown in Fig. 3 is the result of these equations. As is seen, for this settling error there is a minimum value for time-constant coefficient around $PM = 70^o$ and $x_0 = 0.9$.

Given the value of settling time, the required GBW will be minimized at this point. However, it does not lead to minimum power consumption, because, the designer should perform optimizations based on the power equation. This is related to the amplifier topology.

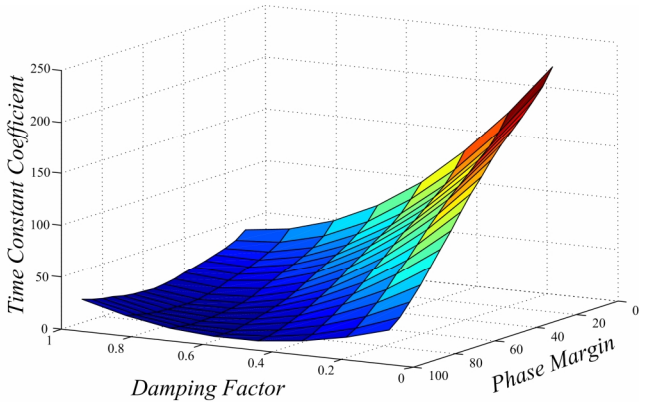


Figure 3: Time constant coefficient (n) against PM and x_0 for e_{SS} = 0.05%

IV. THE PROPOSED DESIGN METHODOLOGY

The performed analysis in previous section makes it possible to present a settling-based design methodology for three-stage nested-Miller compensated opamps. Input parameters that should be determined in this design methodology are load and compensation capacitors (C_L , C_{C1} , C_{C2}), settling time (t_S), overdrive voltage of input transistors (V_{effi}), feedback factor (β), DC gain (A_0), peak-to-peak output voltage swing (V_{Swing}) and finally small-signal settling error (e_{SS}). It is also essential to find the optimized x_0 and PM, along with their corresponding time constant coefficient (n), such that settling time is minimized. As the optimal point corresponding to minimum power consumption equivalent point is typically $PM = 70^o$ and x_0 =0.6 (optimizations based on the equations presented later), the time-constant coefficient values for this point are reported in Table I.

The design procedure starts by deriving the required value for input transistors transconductance. Combining (3) with (7) results

$$g_{mi} = C_{C1}\left(\frac{n}{b} + \frac{V_{Swing}}{V_{effi}}\right)\frac{1}{t_S}. \qquad (12)$$

Substituting (8) into (10), g_{mC} and g_{mL} are eventually found through their relationships with g_{mi}, as follows

TABLE I. TIME-CONSTANT COEFFICIENT AGAINST. SMALL-SIGNAL ERROR FOR PM=70° AND x_0 =0.6

Small-Signal Error (e_{SS})	Time Constant Coefficient (n)
0.005%	6.4792
0.01%	6.3192
0.025%	6.0298
0.05%	5.6927
0.1%	4.2253
0.25%	3.9973
0.5%	3.7963
1%	3.5375

$$g_{mC} = \frac{b}{2x_0}\frac{C_{C2}}{C_{C1}}(x_0 \tan(PM) + \sqrt{1+x_0^2 \tan^2(PM)})g_{mi}, \quad (13)$$

$$g_{mL} = 2b\, x_0 \frac{C_L}{C_{C1}}(x_0 \tan(PM) + \sqrt{1+x_0^2 \tan^2(PM)})g_{mi}. \quad (14)$$

The first-stage tail current can then evaluated from

$$I_{Tail} = 2I_i = g_{mi} V_{effi} = C_{C1} V_{effi} (\frac{n}{b} + \frac{V_{Swing}}{V_{effi}}) \frac{1}{t_S}. \quad (15)$$

In order to improve the slewing performance of the opamp, the slew-rate of all stages can be set equal. Hence,

$$SR_1 = SR_2 = SR_3 \Rightarrow I_C = \frac{1}{2}\frac{C_{C2}}{C_{C1}} I_{Tail}, \quad (16)$$

$$I_L = (1 + \frac{C_{C2}}{C_{C1}} + \frac{C_L}{C_{C1}}) I_{Tail}. \quad (17)$$

V. CASE STUDY

The proposed methodology is validated through simulations in 0.35μm double-poly double-metal process. A three-stage nested-Miller compensated opamp (Fig. 1a) in unity feedback configuration (Fig. 4) was designed to satisfy these specifications: A_0= 105dB, C_L=100pF, C_{C1} = 30pF, C_{C2} = 10pF, 0.1% settling time (t_S) = 1μs, V_{effi} =0.3V and V_{Swing} = 0.5V. Performing power optimization based on these requirements results $PM = 70°$, $x_0 = 0.6$ as the optimized point. The transconductance values, calculated from (12) to (14), are g_{mi} = 277μA/V, g_{mC} = 275μA/V and g_{mL} = 3697μA/V.

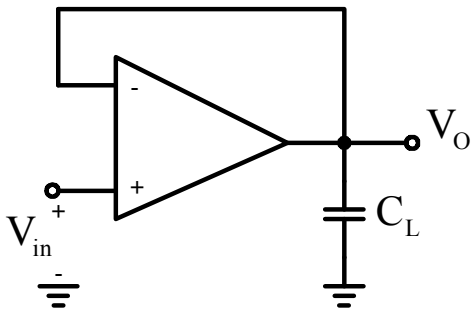


Figure 4: The simulated unity-gain buffer

The circuit dissipates 700μW of power. The loop-gain frequency response of the opamp is shown in Fig. 5. The GBW and PM are equal 1.4MHz and 71° respectively. The damping factor is 0.62.

Table II shows the derived 0.1% settling time of the circuit based on these values. DC gain and slew-rate (SR) are also reported.

To show that the results are optimized for these specifications based on 1μs settling time, compensation capacitors were sized for PM = 60° and x_0 = 0.7 [1] and also PM = 70° and x_0 = 0.7 [2]. These results are also shown in Table II for comparison. As is seen, only the proposed equations can guarantee the 0.1% settling time to be less than 1μs. This is an important result and is due to involving the settling time into the analysis. Fig. 6 compares the step response of the amplifier to a 0.5V input step when capacitances are differently sized.

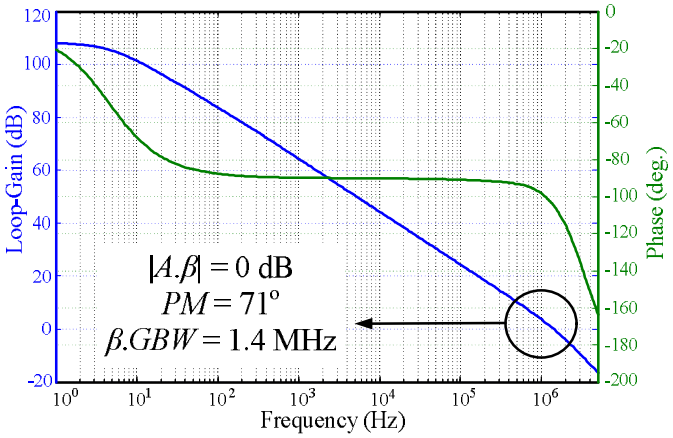


Figure 5: Loop-gain frequency response of the buffer

TABLE II. SIMULATION RESULTS AND COMPARISON

Parameter	As in [1]	As in [2]	This work
Load Capacitor (pF)	100		
Power (μW)	700		
DC Gain (dB)	108		
C_{C1},C_{C2} (pF)	27,13.6	40,13.6	30,10
GBW (MHz)	1.41	1.10	1.40
SR+ (V/ µs) SR- (V/ µs)	1.20, 0.90	0.82, 0.70	1.16, 1.24
Damping Factor	0.73	0.68	0.62
Phase margin (deg.)	58	70	71
Expected t_S (μs) +0.1% t_S (μs) -0.1% t_S (μs)	--- 1.05 1.24	--- 1.26 1.27	1 0.94 0.93

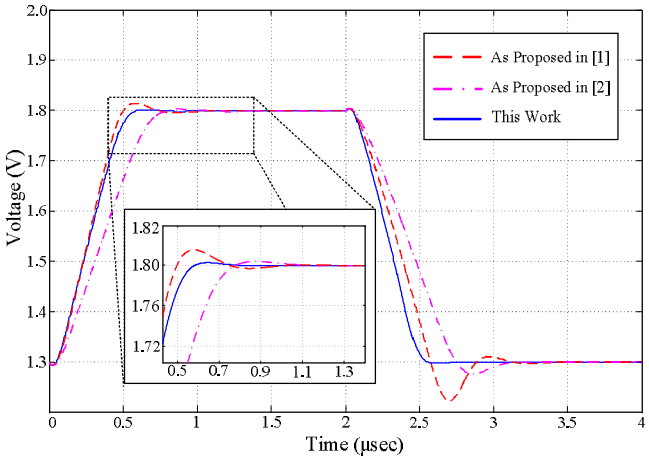
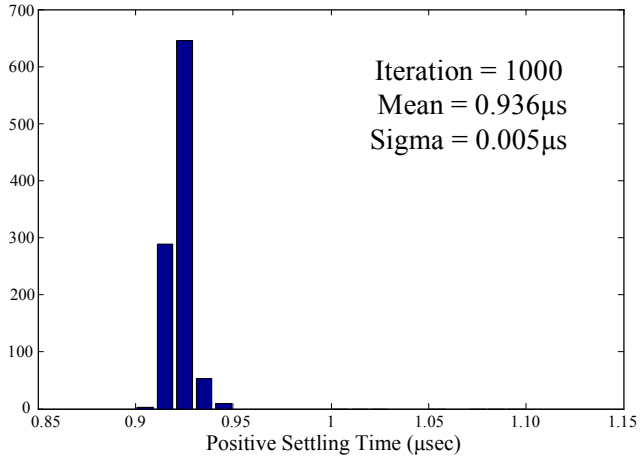


Figure 6: Comparison between different methodologies



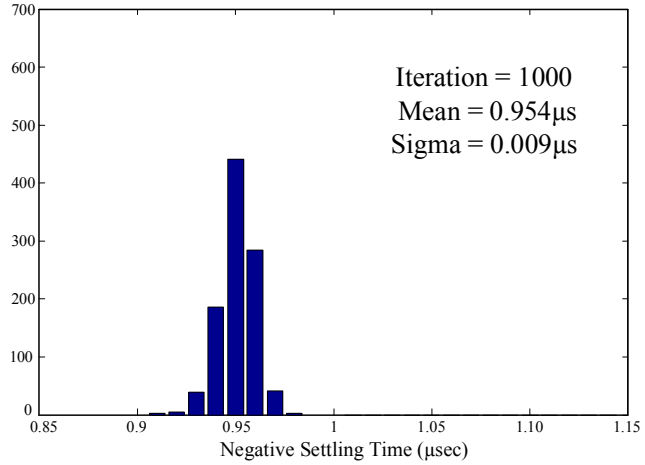


Figure 7: Statistical distribution of 0.1% settling time resulting from 1000 Monte Carlo simulations due to local mismatches

Fig. 7 illustrates the 0.1% settling time distribution for 1000 iterations, with 5σ = 1% (σ is the standard deviation) capacitor mismatch and available models device mismatches. For the optimized point, the mean values of positive and negative settling times are 0.94μs and 0.96μs with standard deviations of 0.005μs and 0.009μs, respectively. The total harmonic distortion (THD) for a 100 kHz sinusoidal input is -92dB, -72dB, and -66dB for 0.2Vp-p, 0.6Vp-p and 1Vp-p amplitude respectively.

Corner simulations were also executed. For the worst temperature case namely 85°C, the nominal positive settling time is decreased to 0.91μs with drop in DC gain to 103dB. At speed worst-case corner, the settling time is increased to 0.98μs.

The opamp can be designed using the proposed equations but with the procedures of [1] and [2] for the same C_{C1}, C_{C2}, t_S and V_{Swing}. With [1], calculations show that there would be 20% increase in power consumption and about 16.2% increase in active area occupied by transistors. The approach in [2], on the other hand, leads to respectively 28% and 15.6% increase in these two parameters (the increase in area is due to larger bias currents and larger aspect ratios for the same overdrive voltages).

The proposed design flow is especially helpful for the design and optimization of switched-capacitor circuits. The efficiency of the algorithm has been verified in design and optimization of a 100kS/s switched-capacitor unity-gain sampler. The sampler is shown in Fig. 8. In this architecture, C_S is sampling capacitor which is charged with input voltage during the sampling phase ($p1$). In feedback phase ($p2$), the output settles to the sampled value when C_S is disconnected from the input and connected to V_O. The feedback factor is equal to unity during the sampling phase. In amplification phase, the actual value is

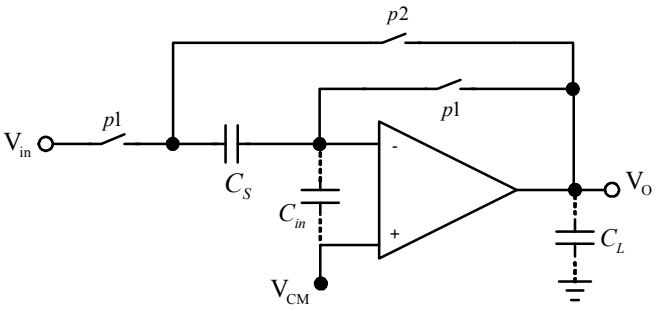


Figure 8: Simulated unity-gain sampler

$$b = \frac{C_S}{C_S + C_{in}}, \qquad (18)$$

which is close to unity. With V_{DD} = 3V, a unity-gain sampler is designed for C_S = 20pF. The three-stage NMC opamp used in this architecture is shown in Fig. 1. The load capacitance seen at the output including parasitic capacitances, the input capacitance of next stage and the series combination of C_S and C_{in} is roughly equal to 60pF. The required peak-to-peak voltage swing is 0.4Vp-p. Based on the required accuracy and sampling frequency, the small-signal settling error is calculated to be less than 0.05% in 4μs settling time. The opamp is designed, using the proposed algorithm. Before beginning simulations, the optimized phase margin and damping factor are determined. According to the noise and settling considerations, C_{C1} and C_{C2} were set to 20pF and 10pF respectively. Table III compares between simulation and calculated results. Fig. 9 depicts the loop-gain frequency response of the sampler. Fig 10 shows the settling response of the circuit.

VI. CONCLUSION

In this work, a design methodology based on settling time is presented for three-stage nested-Miller-compensated opamps. To include settling time into the analysis, the relationship between bandwidth, voltage swing, and settling time is presented. Based on the derived equations, optimization of the circuit based on settling time is preformed to minimize power consumption. Simulation results confirm the efficiency of the proposed approach in meeting all the given specifications. The most important advantage of this methodology is the possibility to design the amplifier based on settling time.

TABLE III. SIMULATED AND CALCULATED RESULTS OF THE SWITCHED-CAPACITOR SAMPLER (FIG. 9)

Parameter	Simulation	Calculation
Voltage Swing (Vp-p)	0.4	
C_{C1},C_{C2} (pF)	20,10	
Feedback Factor	0.999	1
DC Gain (dB)	109	---
Damping Factor	0.57	0.60
Phase margin (deg.)	72	70
GBW (*k*Hz)	425	386
SR (V/ μs)	0.27	0.24
0.05% T_S (µs)	3.86	4.00
Power (μW)	120	>95

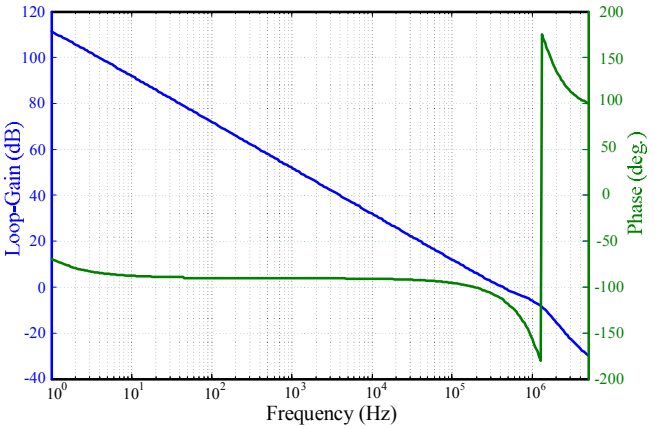


Figure 9: Loop-gain frequency response of the sampler

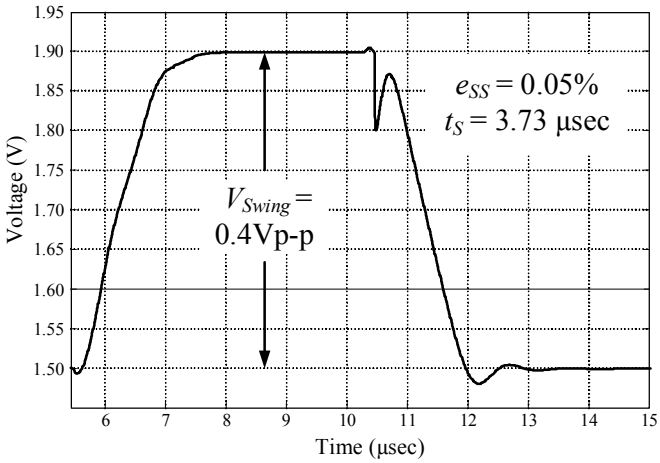


Figure 10: Settling response of the sampler

Appendix A

The equivalent definition of time-constant coefficient as (4), will be derived here for the third order systems. The goal is to obtain a relationship between n and open-loop specifications. In contrast

with (4) which is for a first-order system, the relationship between time-constant coefficient, small-signal settling error and open-loop parameters is non-linear and complicated here. The required analysis has been undertaken in [19]. In particular, the relation between open-loop and closed-loop parameters has been extracted. The settling error is obtained from [19]

$$e_{SS} = \frac{1}{1-2ax^2+a^2x^2}\exp(-a.x.W) + \frac{ax\exp(-x.W)}{1-2ax^2+a^2x^2}[(-2x+ax)\cos(W\sqrt{1-x^2}) + \frac{1-2ax^2+a^2x^2}{\sqrt{1-x^2}}\sin(W\sqrt{1-x^2})], \quad (A.1)$$

where W is

$$W = w_n t_{SS} \quad (A.2)$$

Denoting ω_d as the closed-loop dominant pole, α is obtained from

$$a = \frac{w_d}{xw_n}. \quad (A.3)$$

In the above equations, ξ and ω_n are the closed-loop damping factor and closed-loop natural frequency respectively. The relation between these parameters and open-loop specifications is [19]

$$x_0 = \frac{x+0.5ax}{\sqrt{1+2ax^2}}, \quad (A.4)$$

$$w_{n0} = w_n\sqrt{1+2ax^2} \quad (A.5)$$

The open-loop gain-bandwidth product is derived as [17]

$$GBW = \frac{g_{mi}}{C_{C1}} = \frac{1}{b}\frac{axw_n}{1+2ax^2} \quad (A.6)$$

Combining (10) with (A.5) and (A.6) yields

$$x_0\tan(PM) + \sqrt{1+x_0^2\tan^2(PM)} = \frac{(1+2ax^2)^{1.5}}{ax}. \quad (A.7)$$

As it is seen in (A.1), (A.4) and (A.7), when phase margin, damping factor and small-signal settling error are specified, α, ξ and $W=\omega_n.t_{SS}$ can numerically be obtained. Hence, (A.6) can be used to obtain the time-constant coefficient according to

$$n = \frac{t_{SS}}{1/(bGBW)} = \frac{axW}{1+2ax^2} = f(e_{SS}, x_0, PM). \quad (A.8)$$

To obtain α, ξ and W, at first, (A.4) and (A.7) should be combined to find two single variable (but non-linear) equations for α and ξ. These equations might then be solved by a computational program. After solution of these equations are α and ξ for particular ξ_0 and PM. Hence, (A.1) can be simplified into a single variable relationship between e_{SS} and W. This equation can be solved numerically. The key point to solve this equation for W is the fact that e_{SS} is the maximum allowable error. Hence, it may become smaller than e_{SS} in a particular W. However, when W increases, it may eventually become bigger. Therefore, if the result is smaller than e_{SS}, then several points with bigger W are to be checked. The solution will be found when a point which satisfies this condition is achieved.

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