Statistical Modeling of Static Leakage Power and its Variability in CMOS Circuits

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***Abstract*—This paper focuses on the impact of process variations on the estimation of static leakage power and its variability. A statistical methodology for the estimation of static leakage power dissipation due to subthreshold leakage and gate tunneling leakage in 65 nm CMOS digital circuits, in the presence of process variations, is presented. A 2-input NAND gate is used as a representative library element, whose leakage power is extensively characterized, by rigorous mixed-mode simulations. Also, an analytical model for leakage power is proposed at the gate level in terms of the device resistance data, for computational simplicity. The proposed methodology is demonstrated by characterizing the variations in the leakage power of a 4-bit $\times$ 4-bit Wallace tree multiplier by an extensive Monte Carlo analysis. To extend this methodology to a generic technology library for process characterization, an optimal second order hybrid model is proposed by combining a piece-wise quadratic model obtained by Least Squares Method (LSM) and Response Surface Modeling (RSM) of leakage power of NAND gate directly in terms of process parameters, using Design of Experiment (DOE). We demonstrate that our hybrid models based statistical design approach can result in upto 95% improvement in accurate prediction of variability with an error of less than 0.7%, with respect to worst case design. In terms of standard deviation, the predictability of leakage power distributions get tighter by atleast 13X, leading to considerable savings in the power budget of low power CMOS designs. This work aims to bridge the manufacturing to design gap, through the characterization of standard cell libraries for leakage power, in the presence of process variations.**

Index Terms - mixed mode simulations, Design of Experiments, Response Surface Methodology,Least Squares Method, Monte Carlo analysis, hybrid model, analytical resistance model, leakage power distribution

I. INTRODUCTION

Process variability and its impact on circuit design is becoming extremely critical to address power optimization and management issues in sub-90 nm CMOS designs for mobile applications. In sub-90 nm high performance CMOS designs, the static leakage power dissipation contributes about 33% of the total power consumption of the circuit [1] and is expected to increase further with technology scaling. It is estimated that across successive technology generations, subthreshold leakage increases by about 3-5X [2] while gate leakage can increase by as much as 30X [3]. Traditionally, the supply voltage (V_{dd}) is being scaled to achieve the twin objectives: to limit the dynamic power dissipation and to maintain reliability across process generations. Along with V_{dd} scaling, the threshold voltage (V_t) of the MOS transistors has been scaled down to sustain performance enhancements. As a result, sub-threshold leakage power is increasing drastically due to its inverse exponential dependence on V_t. Also, with scaling, as gate oxide gets thinner, oxide tunneling current is increasing exponentially and contributing significantly to leakage power. Moreover, the increasing statistical variation in process parameters has emerged as a serious challenge in nano-scale regime and can result in significant increase in leakage power and its spread. Device sensitivity to variance is increasing faster than process engineers can reduce the variance. Process variations can no longer be hidden behind the defensive barrier of tight design rules. The traditional circuit design techniques based on worst case leakage result in excessive guard-banding, lower performance and extremely pessimistic and expensive design solutions, as worst case model files can easily

exhibit 10-100X larger leakage than a nominal device.

Several methods have been proposed for predicting and minimizing the leakage power and its variations. A full chip leakage estimation technique is presented to accurately account for power supply and temperature variations [4]. A probabilistic framework for full-chip subthreshold leakage power distribution considering within-die and die-to-die variations in process, temperature and supply voltage has been presented [5]. A full-chip subthreshold leakage power prediction model that takes into account within-die threshold voltage variation is presented and verified against statistical measurements in $0.18\ \mu m$ CMOS [6]. An analytical model is proposed to estimate mean and standard deviation of leakage current as a function of process parameter distributions [7]. Analytical models have been developed to estimate mean and standard deviation of the gate leakage, band-to-band-tunneling (BTBT) leakage and the total leakage with parameter variation and to model the correlation among the leakage components with respect to different process parameters [8]. An analytical model is derived to estimate the variation of leakage current due to both intra-die and inter-die gate length process variability and the need for statistical methods for leakage current analysis is demonstrated [9]. A novel statistically aware dual-V_t and sizing optimization method is presented considering both the variability in performance and leakage of a design [10]. A method is proposed to analyse the subthreshold and gate leakage power of a circuit that include spatial correlations due to intra-chip variation [11]. The feasibility of leakage-aware placement of dual V_t circuits to minimise leakage power variation due to correlated process variations has been explored using Monte Carlo simulations [12]. It has been shown that by upsizing the gate length of transistors in the non-critical paths by 6%, leakage power variability is reduced significantly by up to 41%, apart from reducing the leakage power by 24%-38%, while incurring a small delay penalties of under 10% [13]. Voltage interpolation technique is proposed as a post-fabrication tuning design methodology to demonstrate design tradeoffs between circuit tuning range and static power overheads in the presence of process variations. The analysis showed that the scheme can match the nominal delay target with a 10% power cost or for the same power budget, incur only a 9% delay overhead after variations [14]. Adaptive body biasing scheme that computes unique body biases for each voltage/frequency level as the dynamic voltage/frequency scaling control policy at chip power-on offers the best tradeoff in terms of area, performance and power metrics [15]. But none of these works directly relate the leakage power to the process parameters.

Earlier, we have presented a methodology, based on statistical modeling using DOE-RSM and LSM, to estimate the realistic variability in gate delay [16] and dynamic power [17] as a function of underlying process parameters. There is a need for such methodologies for reliable and accurate estimation of static leakage power as a function of process parameters. Such methodologies would facilitate "combination process-design mitigation techniques" exercising tight cooperation between process and design, which are key for managing process variations in future CMOS processes [18].

The major sources of static power are the subthreshold leakage current, the gate oxide tunneling current and the reverse-biased junction leakgage current. The junction leakage is typically negligible compared to the subthreshold leakge, especially for scaled down threshold voltages in nano scale technologies. A difference in T_{ox} of just $2\ A^o$ can lead to an order of magnitude change in I_{gate}, making it extremely sensitive to process variations [19]. Measured variations in chip level leakage current that is as much as 20X have been reported in literature [20]. The growing incidence of parameter variability in sub-100 nm CMOS designs has highlighted the need to consider the impact of leakage variations during design phase itself and to evolve leakage variability-aware design methodologies. Such power conscious CAD tools and methodologies that support design for low power can achieve technology independent gains of the order of 3X to 5X for power [21]. In this direction, we present a statistical methodology to evaluate the effect of individual and concurrent process parameter variations on the static leakage power variations of a complex digital circuit. The proposed methodology, unlike traditional techniques ([4] - [11]), directly relates the leakage power to underlying manufacturing process parameters through Process Compact Models (PCM). This enables the process engineers to tightly control the significant process parameters, to minimize the leakage variations. This will also facilitate the realistic estimation of variability in leakage power considering the actual short range and long range order of individual processes, as well as the correlations among process parameters. The design will, then, become more robust and less conservative. The proposed hybrid models can generate the probability distribution function of the leakage power and hence can also be used for estimating the yield. The static leakage mechanisms considered for study are the sub-threshold leakage and the gate leakage due to direct tunneling.

We perform mixed-mode simulations, which bring the process simulated devices directly into the netlist

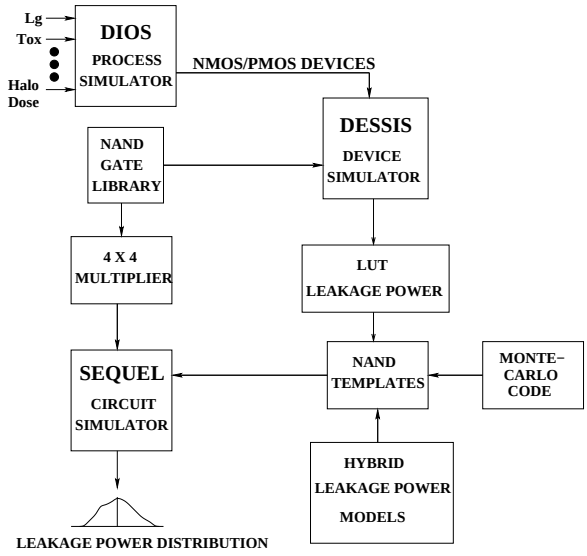

Fig. 1. Block diagram of simulation flow.

of the circuit, wherein both circuit and device equations are solved simulataneously. Process/device simulation is appropriate to the study of process sensitivity as it enables the precise control of process variations that are hard to realise experimentally. A commercial Technology Computer-Aided Design (TCAD) tool suite Sentaurus from Synopsys has been used for process and device simulations [22]. The general purpose circuit simulator SEQUEL (A Solver for circuit EQuations with User-defined ELements), has been used for circuit simulations [23].

II. Simulation methodology for characterization of leakage power of NAND gate

A 2-input NAND gate is selected as a library element for leakage power characterization, which can be extended to include any gate in the library. The overall flow of the events that transform the process variations to relevant leakage power distribution using various simulation tools and models is illustrated in Fig. 1. The nominal NMOS and PMOS devices with 65 nm physical gate length are designed and optimized for an off-state leakage current constraint of 10 nA/μm at V_{dd}=1.2 V. The disposable spacer process sequence, with pocket halo and Super Steep Retrograde Channel (SSRC) implants, has been used for source/drain and channel engineering. The 65 nm gate length NMOS/PMOS devices are generated using process and device simulation based design approach.

For the variability study in this work, we focus on within-die (WID) variations and not die-to-die (D2D) variations. The emphasis here is to model WID variations due to extrinsic factors including both systematic and random components.

A set of process parameters, whose variability has a significant impact on device parameters, is identified based on our simulations and published literature [7], [24], [25], [26], [27]. They include the gate length(L_g), gate oxide thickness(T_{ox}), halo dose, SSRC dose, halo tilt angle and source/drain anneal temperature. The process parameter variations are assumed to have Gaussian distribution with a $\pm 3\sigma$ variation of $\pm 10\%$ of the nominal value, except for the anneal temperature for which it is taken as $\pm 10^oC$. The amount of statistical variation used for these parameters is in accordance with [24], [25], [28]. A set of NMOS/PMOS devices with these assumed variations in each of the six process parameters, taking one at a time, are generated by process simulations, using the Sentaurus Process simulator. The measured gate direct tunneling current density at oxide thickness of 1.4 nm for NMOS is 10 A/cm^2 [29], [30], [31] and that of PMOS is about an order of magnitude less [28], [32]. The simulator is tuned to provide these experimentally measured values for the nominal device. All the devices are simulated, with appropriate models relevant at 65 nm, to obtain $I_d - V_g$ and $I_g - V_g$ characteristics, and their respective subthreshold leakage current I_{off} and gate leakage current I_g are measured. The gate current was measured with the source, drain and substrate tied to ground and by applying positive gate bias for NMOS and negative gate bias for PMOS.

Of the six process parameters considered, it is found that I_{off} is very sensitive to variations in halo dose, halo tilt angle, T_{ox} and L_g. The percentage variation in I_{off} with variations in process parameters are presented in Table I. The relative deviation of any parameter x, about its nominal value x_{nom} is calculated as $\Delta x = (x - x_{nom})/x_{nom}$. It is seen that halo dose and halo tilt angle have the maximum impact on subthreshold leakage variations, for both NMOS and PMOS. This can be attributed to the exponential dependence of I_{off} on threshold voltage which is affected by variations in halo dose and halo tilt angle.

The variation in gate tunneling leakage is very significant with variations in T_{ox} and L_g only [19], [33] and is assumed to be fairly constant with variations in other process parameters considered. The variation in I_g with variations in T_{ox} and L_g are presented in Table II. It is seen that I_g varies by about 8X for a 10% variation of 0.14 nm in T_{ox} for both NMOS and PMOS, with the gate leakage in PMOS being less than that of NMOS by an order of magnitude at all process corners. This is in accordance with the experimental results [19], [32]. As gate current versus gate length is a linear relationship, the gate current

TABLE I
PERCENTAGE VARIATION IN SUBTHRESHOLD LEAKAGE CURRENT I_{off} FOR NMOS AND PMOS. THE NOMINAL VALUES OF CURRENTS ARE $I_{off}(NMOS)$: $9.38\,nA$ AND $I_{off}(PMOS)$: $9.62\,nA$.

Process Variation	NMOS						PMOS					
	Halo	Halo Tilt	T_{ox}	L_g	SSRC	Anneal Temp	Halo	Halo Tilt	T_{ox}	L_g	SSRC	Anneal Temp
-10%	+74.8	+67.0	+52.7	+100.4	+26.2	-3.7	+51.9	+51.7	+22.3	+5.1	+32.0	-24.2
-5%	+32.9	+27.7	+15.2	+28.9	+12.9	-2.4	+19.6	+12.9	+8.2	+3.2	+18.5	-15.5
+5%	-21.6	-19.2	-16.5	-16.9	-9.1	+2.7	-25.7	-23.3	-24.6	-8.4	-14.0	+4.33
+10%	-39.1	-35.1	-26.4	-32.8	-18.0	+4.4	-40.7	-37.6	-34.9	-32.6	-22.2	+12.7

TABLE II
VARIATION IN GATE LEAKAGE CURRENT I_g FOR NMOS AND PMOS. THE NOMINAL VALUES OF CURRENTS ARE $I_g(NMOS)$: $6.44\,nA$ AND $I_g(PMOS)$: $0.65\,nA$.

Process Variation	NMOS		PMOS	
	T_{ox}	L_g	T_{ox}	L_g
-10%	8.8X	-26.2%	7.8X	-10.2%
-5%	3.9X	-23.7%	2.5X	-4.5%
+5%	0.1852X	+24.5%	0.3846X	+18.0%
+10%	0.1282X	+28.8%	0.1587X	+23.2%

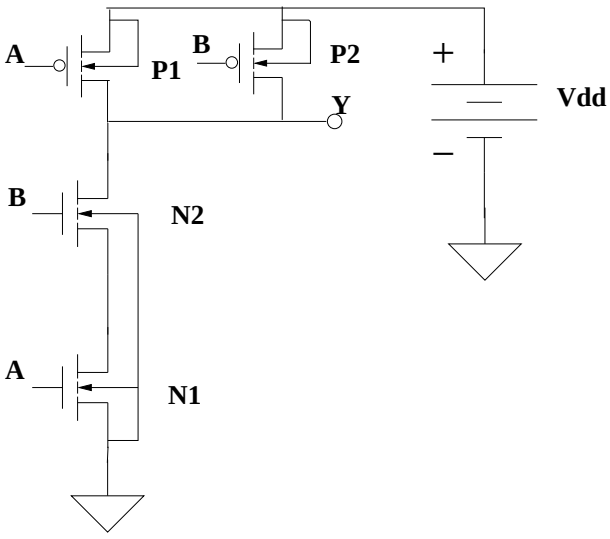

Fig. 2. Single-stage NAND gate.

changes in proportion to L_g with a slope of about 1.8 $\mu A/\mu m^2$, which is in line with the experimental data [33]. These observations validate our tuning of the simulator, against experimental data, for gate leakage simulations.

Using these devices, a single-stage 2-input NAND gate, as shown in Fig. 2, is simulated, to evaluate its steady-state behaviour. The mixed mode simulation approach is used with the Sentaurus Device simulator. Both NMOS and PMOS are simulated at full device level for DC analysis and the total leakage power values for all input combinations are obtained. The variation in the total static leakage power of NAND gate with respect to the nominal, with variations in process parameters, is presented in Table III and IV. The terms $spwr_{00}$ and $spwr_{11}$ denote the total leakage power of NAND gate when both A and B inputs are 0's and 1's respectively. The terms $spwr_{01}$ and $spwr_{10}$ denote the leakage power when A=1, B=0 and A=0, B=1 respectively.

The NAND gate leakage powers are most sensitive to variations in T_{ox}, which indicates the dominance of variations in gate leakage over subthreshold leakage at such low gate oxide thicknesses as 1.4 nm, even as both the subthreshold leakage and gate tunneling leakage increase. The complex nature of variations in NAND gate leakage power with L_g variations is due to the opposing nature of variations in subthreshold leakage and gate tunneling leakage. Among other process parameters, halo dose and halo tilt angle dominate in impacting leakage power due to the exponential dependence of subthreshold leakage on thereshold voltage which is dependent on them.

Look-up tables of NAND gate leakage power $spwr_{00}$, $spwr_{01}$, $spwr_{10}$ and $spwr_{11}$ for nominal, $\pm 5\%$, $\pm 10\%$ variations are generated, for all process parameters.

A. Resistive characterization of leakage power of NAND gate

The above method of characterizing the leakage power of NAND gate, though accurate, involves computationally expensive mixed-mode simulations at the gate level, by taking NAND gate as a library element. To avoid these mixed-mode simulations and to generalize this methodology in order to be applicable to any standard cell library element, an analytical resistive model of leakage power is developed at the transistor level.

The modeling of gate leakage is complicated by its strong state dependency, as determined by the set of applied inputs and its interaction with subthreshold leakage [34]. The gate leakage is primarily driven by ON-devices in contrast to subthreshold leakage, which is driven by OFF-devices. Hence the total leakage power of a gate is calculated for every state of the logic gate, independently. The 2-input NAND gate has 4 logic states corresponding to various combination of

TABLE III
PERCENTAGE VARIATION IN TOTAL LEAKAGE POWER $spwr_{00}$ AND $spwr_{01}$ OF NAND GATE DUE TO PROCESS VARIATIONS. THE NOMINAL VALUES ARE $spwr_{00} : 5.19\ nW$ AND $spwr_{01} : 20.54\ nW$.

Process Variation	$spwr_{00}$						$spwr_{01}$					
	T_{ox}	Halo	Halo Tilt	L_g	SSRC	Anneal Temp	T_{ox}	Halo	Halo Tilt	L_g	SSRC	Anneal Temp
-10%	+438.1	+26.2	+25.5	+17.0	+10.0	-2.5	+376.1	+41.0	+36.7	+44.4	+14.4	-1.0
-5%	+103.4	+12.5	+11.4	+4.3	+5.7	-1.3	+130.0	+18.0	+15.2	+6.6	+7.1	-0.5
+5%	-42.9	-6.6	-6.1	+10.4	-1.6	+1.85	-41.5	-11.8	-10.5	+1.3	-5.0	+1.5
+10%	-61.0	-13.1	-12.3	+12.1	-4.7	+2.2	-53.6	-21.4	-19.2	-5.4	-9.85	+2.4

TABLE IV
PERCENTAGE VARIATION IN TOTAL LEAKAGE POWER $spwr_{10}$ AND $spwr_{11}$ OF NAND GATE DUE TO PROCESS VARIATIONS. THE NOMINAL VALUES ARE $spwr_{10} : 10.69\ nW$ AND $spwr_{11} : 61.65\ nW$.

Process Variation	$spwr_{10}$						$spwr_{11}$					
	T_{ox}	Halo	Halo Tilt	L_g	SSRC	Anneal Temp	T_{ox}	Halo	Halo Tilt	L_g	SSRC	Anneal Temp
-10%	+148.7	+63.4	+57.3	+78.1	+22.6	-1.15	+213.7	+38.9	+31.55	-2.7	+24.0	-27.6
-5%	+37.45	28.3	+24.15	+22.2	+11.4	-0.7	+79.6	+14.7	+9.7	-3.6	+13.9	-11.6
+5%	-23.3	-17.7	-15.7	-9.1	-7.05	+2.9	-37.0	-19.15	-17.5	-0.1	-10.5	+3.2
+10%	-35.4	-32.55	-29.35	-21.0	-14.5	+4.3	-48.0	-30.5	-28.1	-17.2	-16.6	+9.5

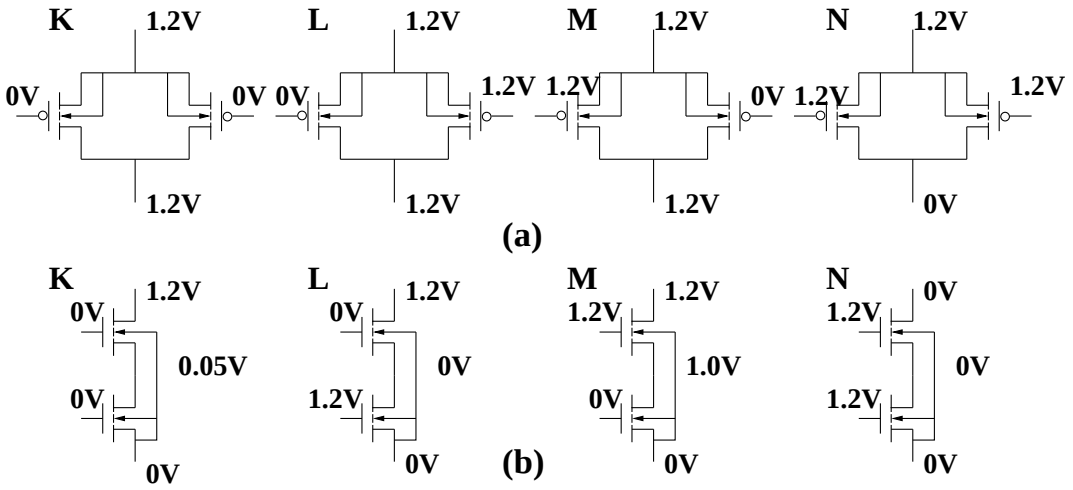

Fig. 3. Analytical resistance modeling of static leakage power of NAND gate: (a) PMOS network (b) NMOS stack.

inputs. The logic states of NAND gate K, L, M and N correspond to inputs 00, 01, 10, and 11 respectively. The PMOS pull-up network and the NMOS pull-down stack corresponding to all logic states are shown in Fig. 3, with bias voltages indicated for individual transistors. The bias voltages are obtained through mixed-mode simulations of NAND gate of nominal NMOS and PMOS devices. These bias voltages are assumed to be constant for all NMOS/PMOS device splits at various process corners. This assumption is validated by rigorous mixed mode simulations at process corners to compute the node voltages. We observe an error of less than 6% for drain bias voltage of NMOS1 of NMOS stack and less than 0.001% for bias voltage at node Y. Also the characterized resistances with these assumed bias voltages are in error by less than 1% with respect to those values with actual bias voltages.

The NMOS and PMOS devices at all process corners are simulated to obtain drain current and gate current individually, with the indicated bias voltages. The respective drain and gate resistances of NMOS/PMOS are calculated. Then effective drain resistance and effective gate resistance between V_{dd} and ground is calculated for the NMOS/ PMOS NAND gate structure for all its logic states. They would model resistively the subthreshold leakage power and gate leakage power of the gate for individual logic states, respectively. Thus NAND gate leakage powers $spwr_{00}$, $spwr_{01}$, $spwr_{10}$ and $spwr_{11}$ are modeled in terms of device drain and gate resistances. This resistive model can be generated, as part of the process characterization effort, for different standard cells of different gate topologies and can be reused for different gate sizes, by appropriately scaling them.

III. Modeling Methodology

To model the relationship between the static leakage power with simultaneous variations in multiple process parameters, the statistical technique of Design of Experiments (DOE) is used. The Box-Wilson design is performed and second order models are built for static leakage power, using response surface methodology (RSM) [35].

A 3-level Face Centered Central Composite (FCCC) design of resolution VI [36], for six process parameters is designed with 52 experimental runs and second order models are obtained by regression using simulation data as described in our earlier work [16]. The models are long polynomials of the form,

$$\begin{aligned} y =& \beta_0 + \beta_1 x_1 + \beta_2 x_2 + ... + \beta_6 x_6 + \beta_{12} x_1 x_2 \\ &+ \beta_{13} x_1 x_3 + ...\beta_{23} x_2 x_3 + \beta_{24} x_2 x_4 + ... \\ &+ \beta_{56} x_5 x_6 + \beta_{11} x_1^2 + \beta_{22} x_2^2 + ... + \beta_{66} x_6^2 \quad (1) \end{aligned}$$

where β_0 is a fitting constant representing the nominal value of the response function, x_is are the normalized process parameters, varying between -1 to +1, and β_is are the corresponding regression coefficients determined by the data obtained from the response surface DOE, for i = 1, ..., 6. Thus an optimum second order model is obtained for the leakage power of NAND gate for all input combinations.

Fig. 4 shows the percentage variation of static leakage power as a function of percentage variation of process parameters, obtained by mixed-mode simulations and the DOE-RSM model. The variation in leakage power is calculated at each X value as a percentage of its value for the nominal design. To detect and fit the cubic effects seen in the leakage power response due to variations in L_g and T_{ox}, as shown in Fig. 4, we have adopted the Hybrid modeling methodology as elaborated in our earlier work [16] by performing piece-wise quadratic modeling using Least Squares Method (LSM). This piece-wise modeling is justified because the nominal device in sub-100 nm technologies is typically designed very aggressively, with the roll off in any given device response below the nominal design being significantly different from the one above the nominal design. Thus, we have been able to capture these responses with just 52 experimental runs, which otherwise would have required 240 experimental runs of a third order rotatable design, resulting in savings of 5X in computations. To account for the wide variations, about an order of magnitude or more, in gate leakage powers due to variations in T_{ox}, natural logarithmic transformation is applied for LSM modeling of gate leakage power component.

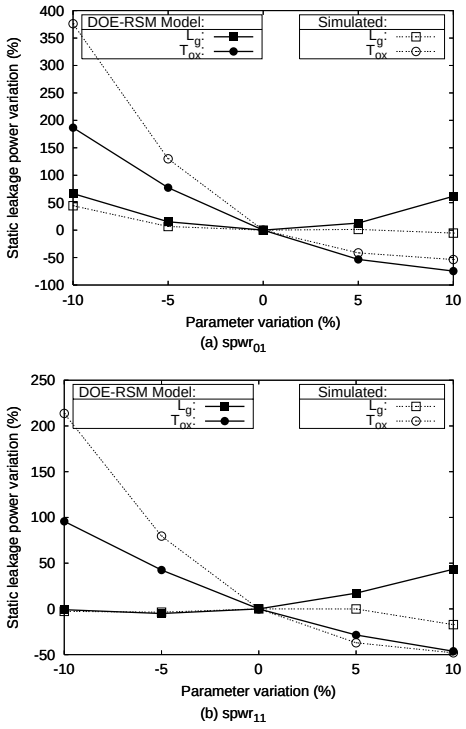

Fig. 4. Comparison of simulated and DOE-RSM modeled leakage power variation with respect to process parameter variations: (a) $spwr_{01}$ (b) $spwr_{11}$.

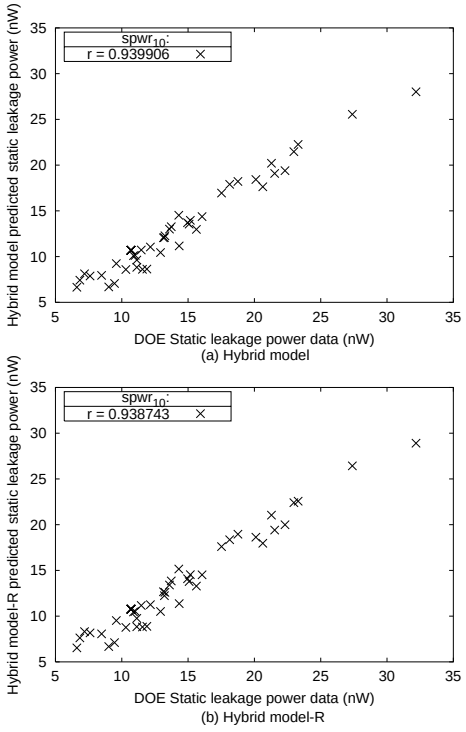

Fig. 5. Correlation plot of hybrid model predicted leakage power data versus simulated DOE data: (a) Hybrid model (b) Hybrid model-R.

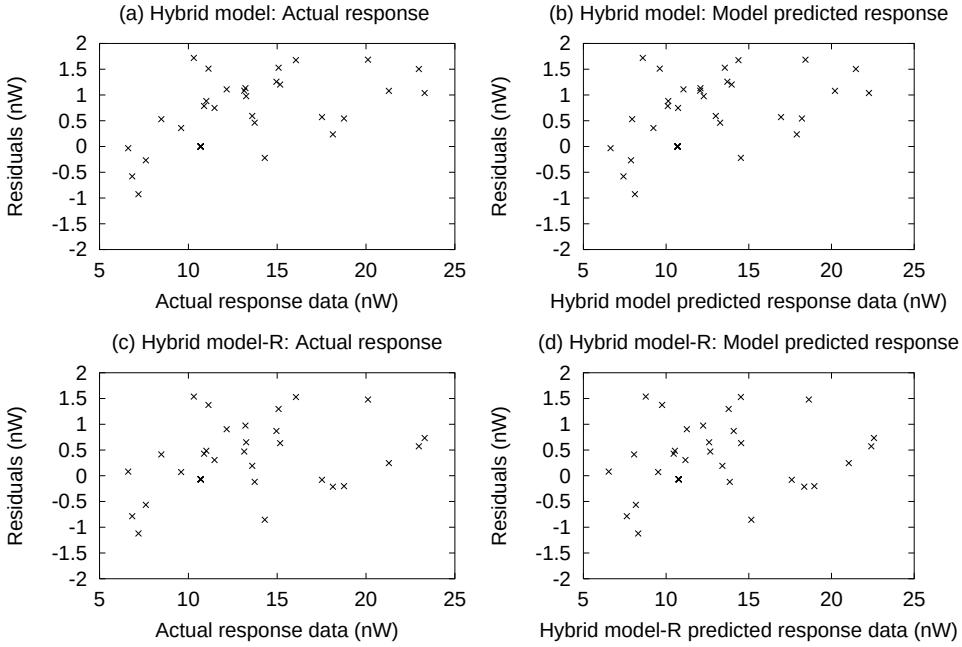

Fig. 6. Residual plots of hybrid model predicted leakage power $spwr_{10}$: (a) Residuals Vs. Actual response with Hybrid model (b) Residuals Vs. Hybrid model predicted response with Hybrid model (c) Residuals Vs. Actual response with Hybrid model-R and (d) Residuals Vs. Hybrid model predicted response with Hybrid model-R.

Following this methodology, two sets of hybrid models are obtained; "Hybrid model" by taking the DOE experimental data generated from mixed-mode simulations for accuracy and "Hybrid model-R" by taking the DOE data generated from the analytical resistive model of static leakage power of Section II-A, for computational simplicity.

The hybrid models for leakage power response functions have been tested for their validity to predict the response values, by correlation plots, which are found to be satisfactory. The correlation plots for the leakage power variables along with their correlation coefficient (r) are shown in Fig. 5 for both Hybrid model and Hybrid model-R. Good correlation between the original experimental response and the model predicted response is observed with the correlation coefficient (r) in the range 0.88 to 0.94 for Hybrid model and in the range 0.86 to 0.94 for Hybrid model-R. The leakage response variables and their correlation coefficients for Hybrid model and Hybrid model-R are tabulated in Table V.

TABLE V
LIST OF HYBRID MODELED STATIC LEAKAGE POWER RESPONSE FUNCTIONS AND THEIR CORRELATION COEFFICIENTS.

Static power response variable	Correlation Coefficient	
	Hybrid model	Hybrid model-R
$spwr_{00}$	0.881911	0.862528
$spwr_{01}$	0.876409	0.875172
$spwr_{10}$	0.939906	0.938743
$spwr_{11}$	0.873845	0.859715

The model accuracy obtained is taken to be very good considering that we have fitted cubic or higher order response effects with piece-wise quadratic models using 3-level FCCC design with some improvisation. The plots of residuals and predicted/actual response for Hybrid model and Hybrid model-R, shown in Fig. 6, provide further evidence that the hybrid model fits the data adequately, as the residuals are randomly scattered around zero, with no visible systematic structure. The magnitude of residuals is less than 10% of the actual values for the Hybrid model and Hybrid model-R, indicating reasonable accuracy. It can be seen that the Hybrid model-R has slightly lower accuracy than Hybrid model, but offers significant computational benefits, as it has been generated using resistance characterization data avoiding mixed-mode simulations at the gate level. Thus the model adequacy for reasonable leakage power prediction is demonstrated.

Fig. 7 shows the percentage variation of static leakage power as a function of percentage variation of process parameters, obtained by mixed-mode simulations, hybrid model and hybrid model-R. It can be seen that hybrid models track the mixed mode simulated variations very well.

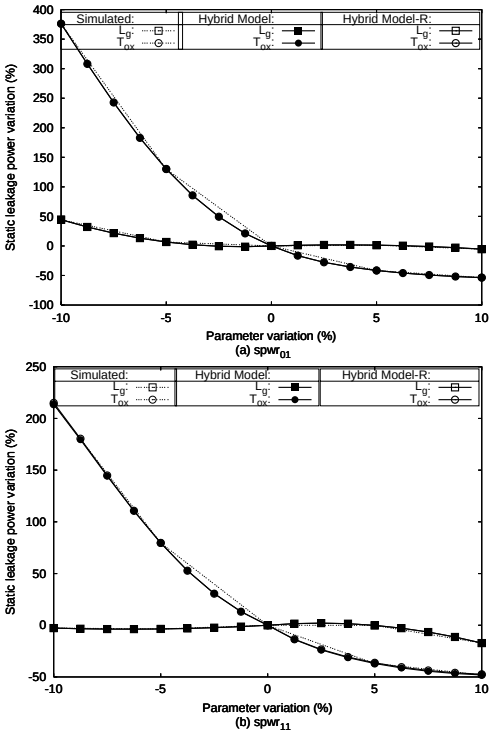

Fig. 7. Comparison of simulated, hybrid model and hybrid model-R leakage power variation with respect to process parameter variations: (a) $spwr_{01}$ (b) $spwr_{11}$.

IV. Leakage Power Distributions of a Digital Circuit

A 4-bit $\times$ 4-bit Wallace tree multiplier circuit is designed using 2-input NAND gate as a library element. This circuit is sufficiently large consisting of 3 half adders, 9 full adders and a few NAND gates. The circuit consists of 266 2-input NAND gates, totalling 1064 transistors. The input vector that results in worst case total static leakage power is identified and is used in all subsequent simulations. The steady state analysis of the circuit is carried out in a gate level simulation, to obtain its leakage power, using the event driven simulation capability of SEQUEL circuit simulator. The within-die systematic variations are modeled by assuming that the process parameters vary as per Gaussian distribution with varying mean of 0% , $+5\%$ and -5% of the nominal value. The within-die random variations are modeled by assuming a $\pm 3\sigma$ variation of $\pm 5\%$ of the nominal value around respective mean values. The $\pm 5\%$ variation is for the short range process variation and is a subset of the worst case of $\pm 10\%$ variation.

A probability distribution for the static leakage power of the circuit is obtained, using rigorous Monte Carlo simulations, by randomly varying different process parameters, individually and then concurrently. A custom Monte Carlo code is written that considers each of the process parameters as an uncorrelated random input variable and is integrated with SEQUEL simulator. As a result, every NAND gate in the circuit gets various process parameter values, as per the Gaussian distribution of respective process parameters, with specified mean and variance. The two NMOS and two PMOS devices constituting the NAND gate are assumed to be closely spaced as to suffer identical process variations. If the data for spatial correlation is known, it can be incorporated to account for correlation between parameters of transistors belonging to different gates. Thus we have considered within-die correlated variations at the intra NAND gate level and within-die uncorrelated variations at the inter NAND gate level.

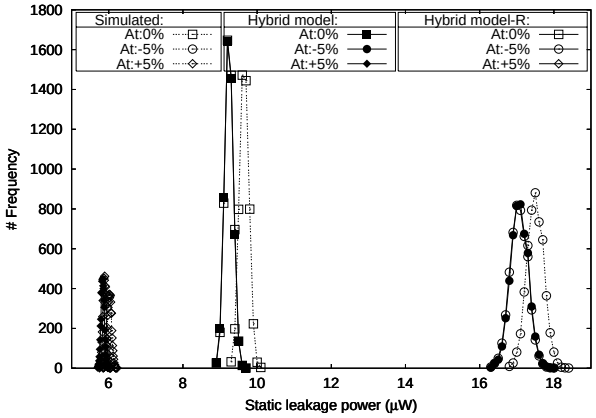

Fig. 8. Simulated and hybrid modeled leakage power distribution for variations gate oxide thickness (T_{ox}).

The leakage powers are assigned to all the gates in the circuit based on their inputs, from a look-up table, by applying linear interpolation. For accurate results, at minimum computational cost, 5,000 Monte Carlo trials are performed. Fig. 8 shows the static leakage power distribution for systematic and random variations in oxide thickness (T_{ox}), when varied individually, using mixed mode simulation generated and hybrid model generated static leakage power values. The distribution obtained using rigorous mixed-mode simulation power values is overlaid with the distributions obtained using the hybrid model and hybrid model-R. We observe a fairly good match for these distributions. The statistics for variations in T_{ox}, obtained by analyzing the resulting distributions, are presented in Table VI. While the hybrid model predicted distribution mean and the standard deviation are in error by less than 4.2% and 16% respectively, against their respective simulated values, the best and worst corner powers are

TABLE VI
STATISTICS OF LEAKAGE POWER DISTRIBUTION FOR VARIATIONS IN T_{ox} (IN μW).

Statistics	Simulated			Hybrid Model			Hybrid Model-R		
	At -5%	At 0%	At +5%	At -5%	At 0%	At +5%	At -5%	At 0%	At +5%
Nominal leakage power	16.79	9.17	5.75	16.79	9.17	5.80	16.77	9.17	5.75
Distribution mean	17.49	9.65	6.02	17.07	9.24	5.88	17.06	9.24	5.84
Median	17.49	9.65	6.02	17.07	9.24	5.88	17.06	9.24	5.84
Std. deviation	0.2251	0.1223	0.0512	0.2362	0.1129	0.0430	0.2375	0.1117	0.0423
Best leakage power	9.17	5.75	4.69	9.17	5.75	4.69	9.17	5.80	4.74
Worst leakage power	30.64	16.79	9.17	30.64	16.79	9.17	30.10	16.77	9.17

exact. The hybrid model-R predicted distribution mean, standard deviation and the corner powers are in error by less than 4.2%, 17% and 1.1% respectively, against their respective simulated values. Nominal power is the leakage power that the circuit dissipates when all the devices in the circuit get the nominal process parameter values. Similarly, best and worst powers are obtained when all devices in the circuit get the best or worst process parameter values respectively. The model statistics track the actual statistics well, thus validating the hybrid model approach.

To generalize the methodology for simultaneous variations in multiple process parameters, simultaneous variations in two significant process parameters are considered. A large look-up table is generated containing 25 power values, corresponding to 25 device/circuit splits with nominal, $\pm 5\%$ and $\pm 10\%$ variations for two parameters. All 25 pairs of NMOS/PMOS devices are generated and mixed-mode simulations of NAND gates using these devices are carried out. Then Monte Carlo simulations are performed, by generating two uncorrelated random numbers for every NAND gate in the circuit, one for each parameter, as per their respective assumed statistics. The power values for different logic states of different gates in the circuit are assigned from the look-up table, by applying two-dimensional interpolation. Then leakage power distribution plots are obtained by the above method and by using the hybrid model equations for the simultaneous variation in T_{ox} and halo dose. This parameter combination is selected as they are the significant process parameters from the perspective of static power variability. The leakage power distribution plots for simultaneous variations in T_{ox} and halo dose is shown in Fig. 9 and their statistics are given in Table VII. The hybrid model predicted distribution mean, standard deviation and corner powers are in error by less than 6.7%, 16%, and 6.6% respectively, against their respective simulated results. The hybrid model-R predicted distribution mean, standard deviation and corner powers are in error by less than 7.4%, 17.3%, and 7.7% respectively, against their respective simulated results. The model statistics track the actual statistics reasonably well, thus validating the hybrid model approach for simultaneous variations in two process parameters.

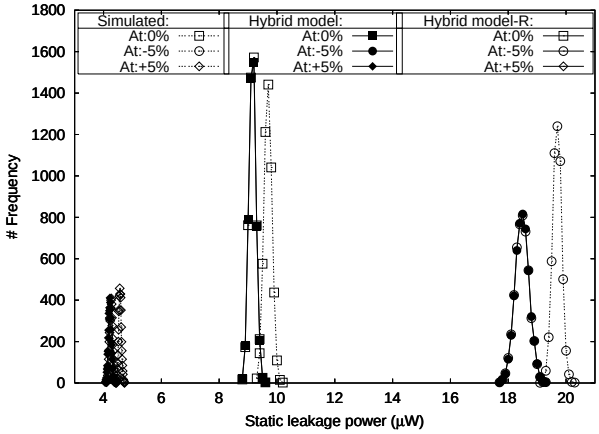

Fig. 9. Simulated and hybrid modeled leakage power distribution for simultaneous variations in gate oxide thickness (T_{ox}) and halo dose.

The proposed model is validated against several benchmark circuits like half adder, full adder and the 4×4 multiplier and their corresponding error data for simultaneous variations in T_{ox} and halo dose are tabulated in Table VIII. It follows that the error scales down as circuit size scales up, before the error becomes somewhat constant.

A rigorous verification for simultaneous variations in more than two process parameters requires 5^n device/circuit splits, where n is the number of process parameters that are varying simultaneously. This leads to the required number of device/circuit splits to increase in a power series fashion, as n increases. The predictive ability of hybrid models has been demonstrated for simultaneous variations in two ($n = 2$) process parameters, indicating that hybrid models have adequately captured the correlation effects between process parameters apart from main effects. Since all correlation terms have come from the same single step of DOE-RSM modeling, it is reasonable to extend this methodology to multiple process variables.

The hybrid models can be used to determine the power budget of a circuit for design closure. In the traditional worst case methodology, all the NAND gates in the multiplier take identical set of process

TABLE VII
STATISTICS OF LEAKAGE POWER DISTRIBUTION FOR SIMULTANEOUS VARIATONS IN T_{ox} AND HALO DOSE (IN μW).

Statistics	Simulated			Hybrid Model			Hybrid Model-R		
	At -5%	At 0%	At +5%	At -5%	At 0%	At +5%	At -5%	At 0%	At +5%
Nominal leakage power	20.44	9.17	4.36	18.18	9.17	4.15	18.17	9.17	4.11
Distribution mean	19.69	9.68	4.56	18.48	9.15	4.26	18.48	9.15	4.22
Median	19.69	9.68	4.56	18.48	9.15	4.26	18.48	9.15	4.22
Std. deviation	0.2152	0.1316	0.0442	0.2395	0.1172	0.0513	0.2408	0.1161	0.0518
Best leakage power	9.17	4.36	3.75	9.17	4.15	3.50	9.17	4.11	3.46
Worst leakage power	20.25	20.44	9.17	19.54	19.18	9.17	19.34	19.17	9.17

TABLE VIII
PERCENTAGE ERROR IN MEAN, STANDARD DEVIATION AND CORNER POWERS OF DIFFERENT CIRCUITS WITH SIMULTANEOUS VARIATIONS IN T_{ox} AND HALO DOSE (IN $\%$).

Circuit	Hybrid Model			Hybrid Model-R		
	Mean	Standard deviation	Corner powers	Mean	Standard deviation	Corner powers
Half adder	15	19	11	15	19	11
Full adder	7	17.9	11.1	7	18.1	11.2
4 × 4 multiplier	6.7	16	6.6	7.4	17.3	7.7

TABLE IX
STATISTICS OF LEAKAGE POWER DISTRIBUTION FOR VARIATIONS IN 6-PARAMETERS FOR $\pm 3\sigma$ = $\pm 10\%$ AT NOMINAL (IN μW).

Statistics	Hybrid Model		Hybrid Model-R	
	Worst case design	Statistical design	Worst case design	Statistical design
Nominal leakage power	9.17	9.17	9.17	9.17
Distribution mean	9.43	9.38	9.40	9.36
Median	8.90	9.37	8.91	9.36
Std. deviation	3.6919	0.2788	3.6088	0.2712
Best leakage power	2.13	8.44	1.98	8.34
Worst leakage power	39.4	10.58	35.05	10.34
Variability (%)	39.15	2.97	38.40	2.90

parameters for any given trial in the Monte Carlo loop. On the other hand, with the statistical design approach, each of the NAND gate can take a random set of process parameters in every Monte Carlo trial. All the six process parameters considered are assumed to vary by $\pm 10\%$. The distribution obtained by statistical and worst case approaches, using hybrid model and hybrid model-R, are overlaid in Fig. 10. The power spread, expressed as a ratio of standard deviation to distribution mean (σ/μ), called "variability", is 39.15% for worst case design and 2.97% for statistical design using the hybrid model. The respective values are 38.40% and 2.90% for the hybrid model-R, which closely matches with that of hybrid model. The statistical design with either hybrid models gives tighter distribution with respect to worst case design, as indicated by atleast 13X reduction in their respective standard deviations. In percentage terms, with respect to worst case design, the improvement in accurate prediction of variability is 94.3% with hybrid model and 94.0% with hybrid model-R. These huge gains in power budget have come at a nominal error in distribution mean of less than 0.5%. The hybrid model-R is in error with respect to the hybrid model by less than 0.2%, 2.7% and 2.2% in the prediction of distribution mean, standard deviation and corner powers respectively, by statistical design. Table IX summarizes these results. Thus the results predicted by the hybrid model-R closely matches with that of hybrid model, with a slight decrease in its accuracy.

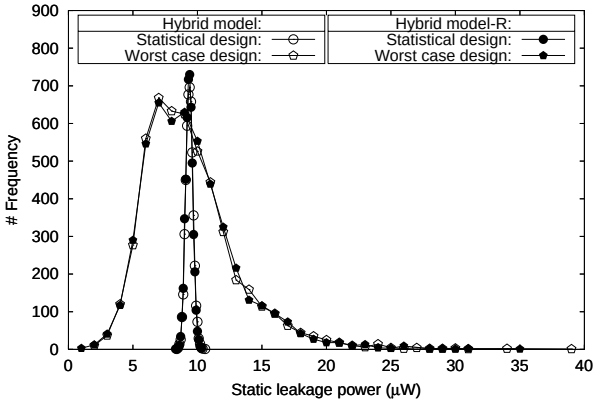

Fig. 10. Leakage power distribution with statistical design and worst case design for simultaneous variation in 6-parameters, for $\pm 3\sigma$ = $\pm 10\%$ at nominal, with Hybrid model and Hybrid model-R.

However, the $\pm 10\%$ variation in process parameters considered is very pessimistic and it is more realistic to

TABLE X
STATISTICS OF STATIC POWER DISTRIBUTION OBTAINED USING HYBRID MODEL FOR VARIATIONS IN 6-PARAMETERS WITH $\pm 3\sigma = \pm 5\%$ AT NOMINAL(IN μW).

Statistics	Worst Case Design			Statistical Design		
	At -5%	At 0%	At +5%	At -5%	At 0%	At +5%
Nominal leakage power	16.78	9.17	3.17	16.78	9.17	3.17
Distribution mean	16.91	9.02	3.16	16.18	9.00	3.15
Median	16.91	8.94	3.11	16.18	9.00	3.15
Std. deviation	2.5364	1.6492	1.0876	0.1854	0.1258	0.1008
Best leakage power	6.96	2.27	1.02	15.48	8.53	2.83
Worst leakage power	33.10	20.75	9.22	16.90	9.50	3.49
Variability (%)	15.0	18.3	34.4	1.1	1.4	3.2

TABLE XI
STATISTICS OF STATIC POWER DISTRIBUTION OBTAINED USING HYBRID MODEL-R FOR VARIATIONS IN 6-PARAMETERS WITH $\pm 3\sigma = \pm 5\%$ AT NOMINAL.

Statistics	Worst Case Design			Statistical Design		
	At -5%	At 0%	At +5%	At -5%	At 0%	At +5%
Nominal leakage power	16.72	9.17	2.72	16.72	9.17	2.72
Distribution mean	17.02	8.99	2.97	16.99	8.98	2.95
Median	16.76	8.92	2.90	16.98	8.98	2.95
Std. deviation	3.0829	1.6274	0.9586	0.2280	0.1242	0.0792
Best leakage power	9.13	4.44	1.01	16.14	8.49	2.65
Worst leakage power	32.22	18.34	8.37	17.81	9.43	3.23
Variability (%)	18.1	18.1	32.3	1.3	1.4	2.7

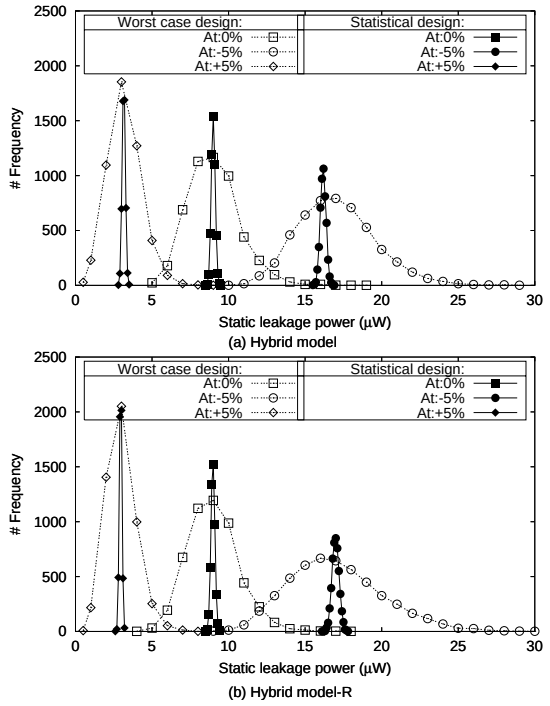

Fig. 11. Hybrid modeled leakage power distribution with statistical design and worst case design for simultaneous variation in 6-parameters for $\pm 3\sigma = \pm 5\%$ at nominal: (a) Hybrid model (b) Hybrid model-R.

consider that the process could be centered around either -5%, 0% or $+5\%$ points with a random variation of $\pm 5\%$ around these points. Monte Carlo analysis is performed by worst case design and statistical design using hybrid model and hybrid model-R to obtain leakage power distributions which are shown in Fig. 11. It can be seen that with the hybrid model, the variabililty is upto 34.4% for worst case design and less than 3.2% for statistical design, with an improvement in accurate prediction of variability of upto 94.75%. The corresponding values are 33%, 2.7% and 93.25% when hybrid model-R is used. In terms of standard deviations, the prediction of leakage power distributions become tighter by upto 14X. Again, these gains in power budget have come at a price of less than 0.7% error in distribution mean. Table X and XI summarize these results. Thus significant performance gains can be achieved by budgeting the static leakage power to lower but realistic values by adopting the statistical circuit design using our hybrid models.

V. CONCLUSIONS

We have proposed a systematic methodology to predict the variability of static leakage power due to the underlying process variations. The methodology takes into account variability in multiple process parameters, and correlations among them, in nano meter scale circuit designs. A 2-input NAND gate is used as a representative library element, whose leakage power is extensively characterized by rigorous mixed-mode simulations. An analytical model for leakage power at the gate level in terms of the device resistance data is proposed. An optimal second order hybrid model is obtained, through response surface model-

ing using design of experiments and least squares method, for leakage power of gate directly in terms of process parameters. The hybrid models are derived based on mixed-mode simulation data for accuracy and the analytical device resistance characterization data for computational simplicity. These process compact models (PCM) are used for characterizing the leakage power of a large digital circuit namely, a 4-bit $\times$ 4-bit multiplier. We have shown that the conventional worst case design approach is very pessimistic, whereas our hybrid models based statistical design approach can result in considerable savings in the power budget of low power CMOS designs with upto 95% improvement in accurate prediction of variability at an error of less than 0.7%, with respect to worst case design. In terms of standard deviation, the prediction of leakage power distributions get tighter by atleast 13X. Though the proposed methodology has been demonstrated for NAND gate library for 65 nm CMOS process, the simplicity and generality of the approach makes it equally applicable to a large library of cells of any process. This methodology, for static leakage power estimation in the presence of process variations, is useful in bridging the gap between the Technology CAD and Design CAD through characterization of standard cell libraries for leakage power, in the face of ever decreasing power budgets for mobile applications.

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