Simple modelling and method for the design of a sigma delta class D power amplifier

Ph.Dondon, M.Cifuentes, G.Tsenov, V. Mladenov

***Abstract*—** The class D amplifier is well known in audio applications since a few ten years. The MOS transistors switching power stage is able to drive a useful power up to 500W to the loud speaker with an excellent power ratio (greater than 90%). Designing such an amplifier is obviously more difficult than designing a classical class A or AB power amplifier. Unfortunately, only mathematical and very complex theoretical approaches are found in the scientific literature. So, we present here a simple and concrete method for students and young designers to design a sigma delta class D amplifier as easily as possible. The experimental results are given to illustrate the design method. Finally, we explain how we exported this work towards pedagogical application and practical lessons for our engineer students.

***Keywords*—** Power electronic, circuit modelling and design, class D, sigma delta modulation, pedagogical approach.

I. Introduction

A. Study context overview

This study was carried out at the "Ecole Nationale Supérieure d'Electronique, Informatique et Radiocommunications de Bordeaux" ENSEIRB-MATMECA (France) in collaboration with Technical University of Sofia (Bulgaria); ENSEIRB is one of the oldest national graduate engineering schools, known as 'Grandes Ecoles' in France founded in 1920. Mathematic and Mechanical department joined ENSEIRB in 2009, to merge in a biggest entity ENSEIRB-MATMECA. It is now member of IPB (institute polytechnique de Bordeaux) strongly linked to the Bordeaux 1, Science and Technology University.

B. Class D basics

The Class D amplification [1] uses MOS power transistors in switching mode [2]. It is able to obtain a power ratio close to 95%. It is then possible to reduce the size and thereby to miniaturize the audio amplifier. The principle is given in figure 1 [3], [4]. The audio signal is converted in a Pulse Width Modulated intermediate signal or Sigma delta modulated signal. This two level signal drives a full bridge MOS power transistor [12] which works in switching mode. Free running diodes are not shown in figure 1. The power supply over 30V enables it to carry a high current in the load. A low pass output filter between the MOS stage and the speaker restores the audio signal. And the feed back active network set the voltage gain of the circuit.

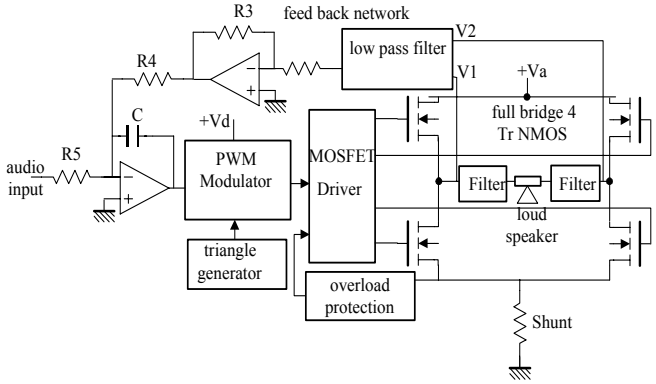

Fig.1: Class D PWM amplifier block diagram

C. Principle of Pulse width modulation (PWM)

The analogue signal is compared to a high frequency triangular waveform. The output is a two level pulsed signal as shown in figure 2.

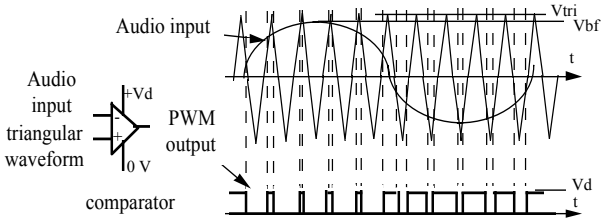

Fig 2: PWM modulation

Let F_{tri} be the frequency of the triangular signal and F_{bf} the frequency of the LF input signal. As a complete mathematical approach is very difficult, we can simplify it, by assuming that the PWM signal is periodic. Then, we can write: pwm(t) =

$$\frac{Vd.\tau}{T_{tri}} + 2Vd\sum_{n=1}^{\infty}\left(\frac{1}{\pi n}\sin\left[(1+m\sin F_{bf}.t)\frac{n.2\pi.F_{tri}.\tau_0}{2}\right].\cos(n2\pi F_{tri}.t)\right) \quad (1)$$

The spectrum of the output signal contains the useful LF signal and also frequencies around $n.F_{tri} \pm k.F_{bf}$.

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D. Principle of the Sigma delta modulator

The sigma delta modulator [15], [16] generates at its output, a digital serial pulse signal, similar to the analogical PWM, but the width of the impulses, by the principle, is sampled and multiple of the period of the clock ($1/F_e$). (Cf. figure 3b)

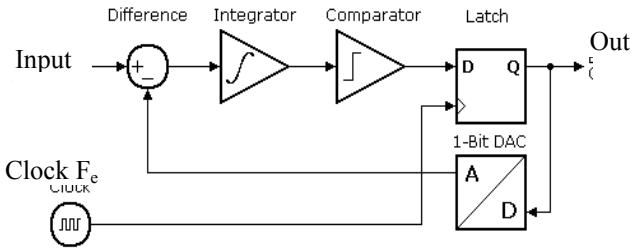


Fig 3a: First order Sigma delta analogue modulation

The figure 3b shows the modulated signal spectrum. This one contains the useful LF frequency of the input signal (which interests us for the later reconstitution of the signal). It contains also a series of lobes (looks like the spectrum of a "pseudo random" bits stream clocked by a clock at F_e) with cancellations all the $n.1/T_e$ (related to sampling by the D latch) and a null DC value.

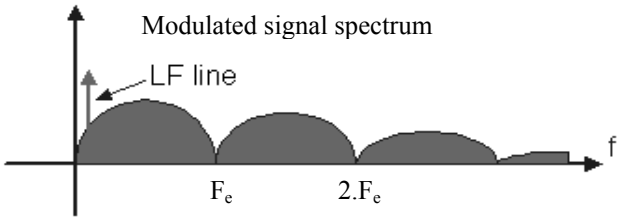


Fig 3b: Sigma delta spectrum waveform

At the maximum modulation rate, the maximum value of the LF frequency line V_{max} will be: $V_{max} = 0{,}5.V_d$, like for PWM modulation, where V_d is the supply voltage of the D latch [4].

E. Sigma delta modulator versus PWM

In the sigma delta version, the PWM stage is replaced by a sigma delta modulator as indicated in figure 4.

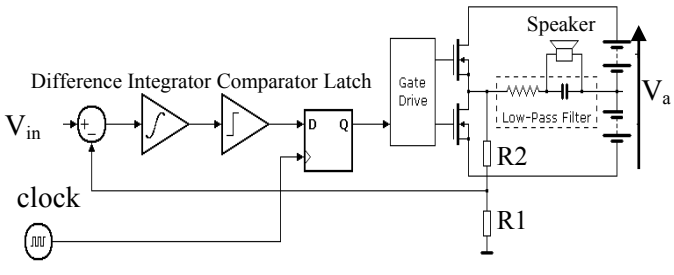


Fig 4: Half bridge first order sigma delta Class D amplifier

Each of the two versions has its own advantages and inconvenient: Sigma delta modulation can be built with analogue circuits or fully synthesised in digital circuit such as FPGA but there is inherent quantification noise due to the sampling. In the two cases the clock frequency must be at least 10 times the maximum frequency of the input signal.

F. Commercial circuits state of art

With the advent of new integrated technology which allows to associate on a same substrate power transistors and small signal components, many integrated class D amplifiers are now available for commercial uses [6], [7] such as automobile radio receivers. Philips, National semiconductor, Texas Instrument, Analog Devices have designed some dedicated sigma delta class D amplifiers for audio application with power up to 50 W. (For example: Philips 2 ×50 W class-D amplifier TDA 8920, Texas instrument 2W class-D power amplifier TPA00514, TPA2000D2, Analog Devices AD1996)

II. INTEREST OF THE WORK

A. Theory missing

In one hand, the mathematical theory of Class D amplification is quite complex due to a mix of analogue digital and power circuits. The mix between continuous time circuit and discontinuous time circuit make a complete modelling difficult. Software such as MATLAB allows simulation and modelling using the "z" transform [11]. In an other hand, these class D amplifiers circuits often look like a "black box" in traditional literature and in technical data books. Finally, a simple description of such amplifier is thus rarely found in the literature. What we suggest here, is a pedagogical and concrete approach to understand the design of such class D amplifier.

B. Pedagogical interest

Whatever the taught electronic field, the link between the theory and practice is often the most important difficulty that appears for the students. Our approach helps them to make this link. Moreover a such practical design allow to sweep, in one project, analogue, digital, power and signal processing aspects of electronic. So, it might be seen as a synthesis's project for our engineer students.

III. DESIGN SIMPLFIED APPROACH

A. Sigma delta modulation equivalent modelling

The spectrum of the feed back V_4 signal (Cf. figure 5a) after sampling was given in figure 3b in the case of a sinusoidal input signal V_{in}: it contains the spectral line LF (Low Frequency) of the input signal and the periodic lobes related to the sampling. In the case of an unspecified input LF signal V_{in}, the spectrum of the V_4 signal will contain by extension, the LF contribution of V_{in} and - instead of the lobes- an almost "white" spectrum (flat) extending until the infinite frequency.

Consequently, it is possible to establish a first equivalent modelling [8], [9], in which one replaces the D latch by a

equivalent switch, switched at the sampling frequency Fe as indicated in figure 5a.

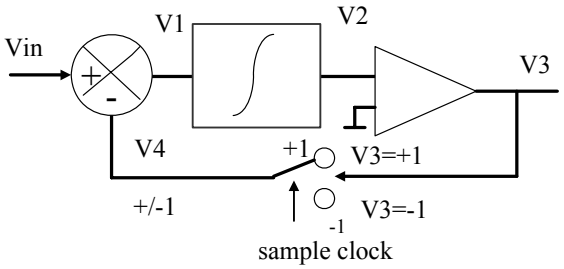
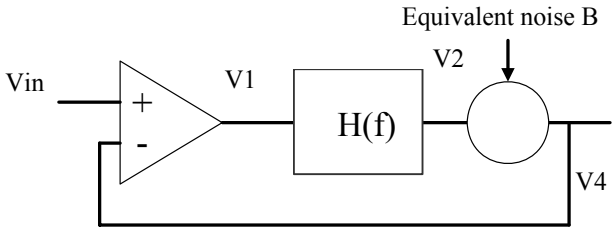


Fig 5a: Simplified modelling

In the second time, the comparator (nonlinear component by nature) and sampling are replaced by an equivalent noise



source "B", which is superimposed on the V_2 signal.
The "linear" diagram thus obtained makes it possible to compute an equivalent linear transfer function. (Cf. figure 5b)

Fig 5b: Simplified noise equivalent modelling

Indeed, we can write:

$$V_1(p) = V_{in}(p) - V_4(p)$$

$$V_2(p) = H(p).V_1(p) \text{ and } V_4(p) = V_2(p) + B(p)$$

With $H(p) = 1/T_c.p$ (with T_c time constant of the integrator)

It yields:

$$V_4(p) = (T_c.p/(1+T_c.p))\, B(p) + (1/(1+T_c.p))V_{in}(p) \quad (2)$$

Thus, the noise B is high pass filtered while the input signal V_{in} is low pass filtered with the same time-constant T_c of the integrator (Cf. figure 6). One must thus choose T_c to let pass the maximum frequency F_{max}, of the input signal V_{in}.

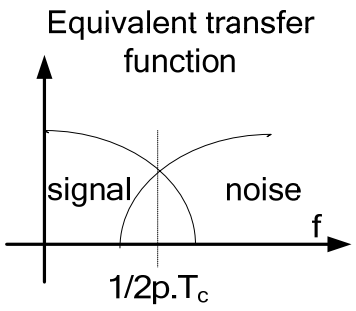


Fig 6: Modulator equivalent Laplace transfer function

B. *Class D amplifier modelling*

Referring to the previous paragraph and from a LF small signal point of view, the class D amplifier (including sigma delta modulator, H bridge and feed back as indicated in figure 4) can be modelled as shown in figure 7.

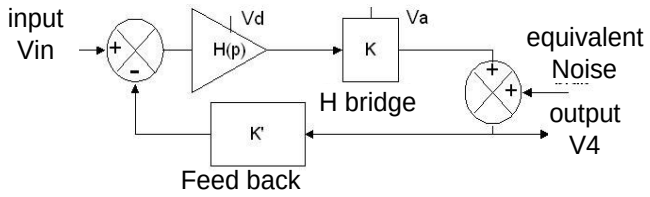


Fig 7: Equivalent class D amplifier LF modelling

Where H(p) is the transfer function on the integrator, K factor, the ratio between the power supply voltage V_a of the power H bridge and the supply voltage V_d of the rest of the circuit. K' the feed back factor can be seen as the ratio of the resistors: $R_1/(R_1+R_2)$ (Cf. figure 4)

After a similar calculus than in § 3.1, it yields:

$$V_4(p) = \left(\frac{\frac{T_c}{K.K'}.p}{(1+\frac{T_c}{K.K'}.p)}\right).B(p) + \frac{1/K'}{1+\frac{T_c}{K.K'}}.V_{in}(p) \quad (3)$$

The equivalent LF gain is 1/K' and do not depends on power supply voltage. At the opposite, V_a supply affects the LF bandwidth.

C. *Stability aspects*

The modulator being a feed back system, it is necessary to wonder about its stability. According to whether one uses an integrator inverter or not, that one will connect on the entry + or – of the comparator, one will need to loop the output Q or /Q of the D latch to ensure stability. In the contrary case, the system is divergent and the output will be locked in a high or low state.
As increasing the order of modulator can cause instability, a simple first order modulator will be used.

IV. DESIGN STRATEGY

A. *Generalities*

A kind of linear « cooking guide » has been written in order to facilitate the design of such amplifier. It includes the mains steps to size the amplifier as follow.

B. *Design "cooking guide"*

The first step of the design is to size the circuits and components.

Let the supply voltage for all low voltage circuits to be $+/-V_d$ and the power supply voltage for the bridge $+V_a$.
One can first calculates the minimum required supply voltage of the full or half bridge as follow: Starting from the specified maximum electrical power Pm to be delivered to the load R_L,

"to be supposed resistive in the audio bandwidth" (Speaker 8 or 4 Ω),

- One determines first the RMS voltage value V_{bfs} of the useful LF line in the modulated signal by:

$$P_m=(V_{bfs})^2/R_L.$$

- Knowing the Fourier composition of the output signal at its maximum modulation rate, the output LF line can reach $\sqrt{2}*V_{bfs} = V_a$ for a full H bridge and $0.5*V_a$ for an half bridge.
- The minimum value of the supply voltage V_a is thus :

$$V_a = \sqrt{(P_m.R_L)}.\sqrt{2}$$

for a full bridge and the double for a half bridge.

Closed LF loop gain determination

- For a correct operation, all voltages through the circuit must be compatible with low voltage power supply +/-V_d. However, the modulation rate is maximum when the peak value of the input signal V_{in} is equal to the peak voltage of the feed back square signal V_4. The consequence is that the maximum value of input voltage V_{in} is :

$$V_{inmax}=V_d/2.$$

As the maximum output peak voltage LF line is equal to V_a, there is a minimum possible LF closed loop gain

$$G_{min} = 2.V_a/V_d$$

for a full H-bridge.

- While the LF closed loop gain is greater than G_{min} and the LF output voltage do not exceed V_a, the gain value will be set by the resistance ratio $(R_1+R_2)/R_1$ (see figure 4) and do not depends on power supply V_a.

Notes: The saturation phenomenon of the amplifier looks similar in the two versions sigma delta or PWM. In the two cases, the closed loop bandwidth expressions look also similar.

V. Detailed Design Guide

A. Generalities

For pedagogical, perennially and cost reasons, the design is done only using discrete, multisource and reliable components.

The main specifications are:

- Output audio power 10W
- Supply voltage +/-5V and power bridge supply +15V,
- Sampling clock frequency adjustable from:
  F_e = 200 kHz to 800 kHz
- Input audio signal: V_{in}, 20Hz-15kHz, 0-2,5V max.
- Amplifier voltage gain: G_v = 10.

B. Sigma delta modulator [21], [22],[23]

It consists of a classical low cost, fast op amp LF355, a fast comparator AD 790 (switching time must be smaller than $(1/10)*T_e$) and a simple CD4013D latch (Cf. figure 8).

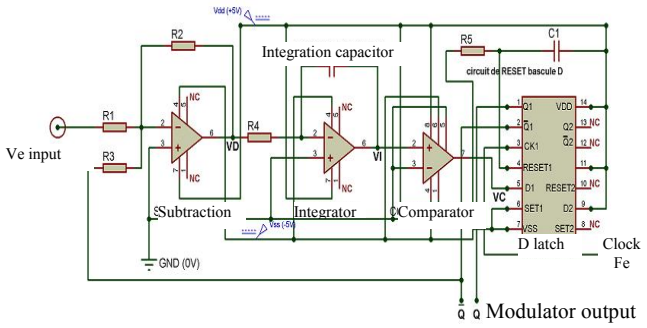


Fig. 8: Sigma delta modulator schematic

-Choosing the integrator constant R.C using intuitive and experimental observation:

The figure 9a shows the waveform in the class D amplifier when removing the integrator capacitor: the sigma delta modulator obviously does not operate correctly: The D latch works as a divider by 2 (/Q looped on the D input through a "equivalent delay cell" due to the delay time into the comparator and OP amps). Thus, the output signal looks like a square waveform at $F_e/2$ (figure 9a).

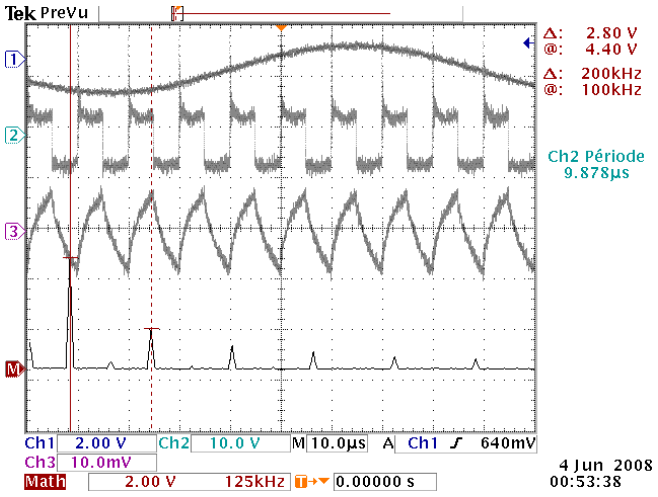


Fig 9a : Choosing the C capacitor value

Trace 1: input sinus signal 1 kHz
Trace 2: "no modulated signal at $F_e/2$ (D latch output)
Lower trace: Spectrum of the "non" modulated signal, odd lines at $(2n+1).F_e/2$

Under theses conditions, the minimum value of R.C is evaluated as follow:

The output voltage of the integrated stage must not reach the saturation limits during a half period of the $F_e/2$ signal. Thus, R.C value must be greater than T_e to avoid saturation.

Reminding the first condition we found in § III.A, we can finally summarize the choice of R.C time constant integrator as indicated in figure 9b:

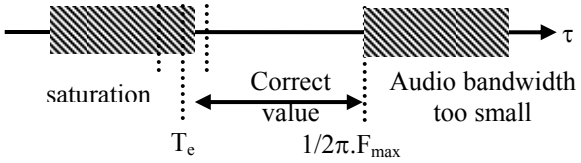


Fig. 9b: Value of RC time constant for sigma delta modulator

- When assembling the sigma delta modulator and the H-bridge to build the D class amplifier, we must take care of the K and K' factors: from equation (3) in § III.B, we can thus determine the RC time constant.

- Choosing the sample frequency:
The sample frequency F_e must be at least greater than 10 times the maximum audio frequency F_{max}. Increasing the sample frequency allows to reject noise in higher frequency, but it also increases the switching losses into the H-bridge. A good compromise is to choose F_e=60 F_{max}. (In our application, F_{max} =15 kHz and F_e =600 kHz)

C. Driver stage

The driver circuit (in our example the well known IRF2113 [3]), located between the PWM modulator and the full bridge, allows the MOS transistors to switch under the best conditions by:

-delivering a 10V voltage pulse and a peak current of 3A to improve the switching times.
-generating a dead time to avoid the cross conduction of two transistors at the switching times.
-inhibiting the gates command signal in case of current overload.

D. Power MOS stage

The power stage consists of a Full H bridge [14], [18] with four discrete matched low "R_{on}" NMOS IRFZ44 (or equivalent) with a bootstrap circuit connected to the driver stage [24, 25] (Cf. figure 10).

If the maximum current or voltage can not be supported by classical bridge integrated circuits such as LM 18200 (NS), L6201, L298 (SGS) for example, the students choose a discrete NMOS transistor reference, by looking at the breakdown voltage $V_{(BR)DSS}$ of the transistor and maximum current with the lower R_{on} to minimize the conduction losses.

R_6 and R_7 are small value resistor (less than 10Ω) placed into the gate to reduce the parasitic oscillations due to MOS internal capacitance and parasitic connexion inductance, without increasing the switching time of NMOS.

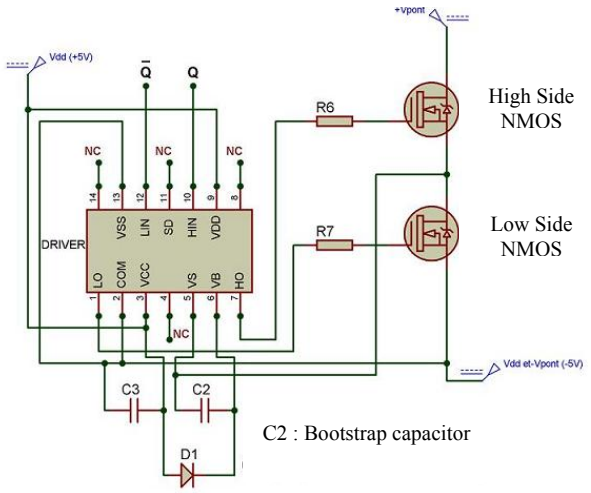


Fig. 10: Driver and MOS stage (half schematic)

E. Overload protection circuit (optional)

The current overload protection [3] consists of one "shunt" resistor, a low pass filter, a threshold comparator, and a MOS transistor driver inhibition circuit (generally included in the driver circuit).

F. Feed back network

Why and where placing the feed back network is most frequent question:
The feed back can take place on the sigma delta modulator (just before the full bridge). In this case the LF equivalent closed loop gain will directly depend on H bridge supply voltage value. Thus, it is better to take feed back as close as possible from the load to reduce the defaults and the sensitivity to the supply voltage, noise etc.
The feed back can take place after the H-bridge on one arm or two arms with a simple resistor ratio or a more sophisticated network.
In our case, it consists of two resistors Bridge (gain set up and signals scaling), two fast follower op amps and a adder/ subtraction circuit LF 355 (because of the full H-bridge structure)

G. Mixed SPICE simulation

In order to check the design, a mixed ORCAD Spice simulation is performed. The schematic is given directly to students to avoid times losses. The simulated circuit do not represent exactly the final electronic design (MOS driver missing). It is only a simplified schematic version just to check the main characteristics of the amplifier (Cf. figure 11a). This simplified simulation approach avoids to loose time with the simulator in order to save time for the concrete experiments.

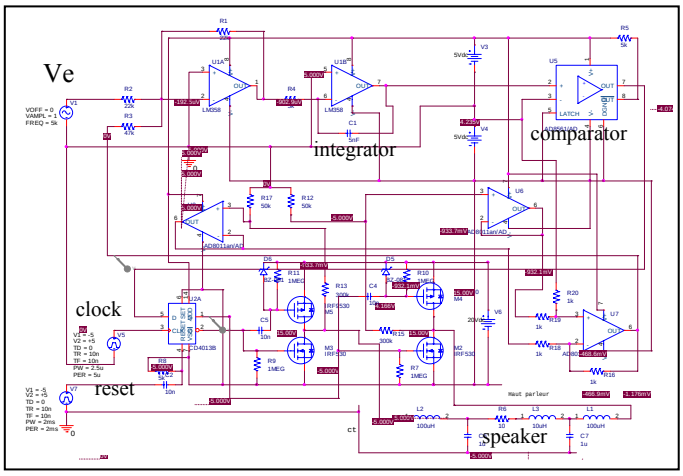


Fig 11a: Simulated class D amplifier schematic

The audio load is simulated by an R, L, C, serial circuit. The values of theses components have been previously extracted from true speaker characteristics with HP 4194A impedance meter (from 100Hz to 1MHz). (Cf. figure 11b). From asymptotic diagram (or internal modelling), we extract R = 8Ω, L=120µH, C= 1,6mF. We can notice that the speaker is almost resistive in the audio bandwidth and fully inductive upper than 20 kHz.

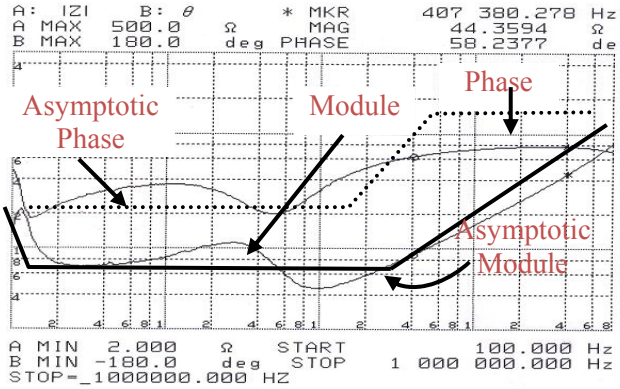


Fig 11b: 3 ways loud speaker parameters extraction

The transient analysis allows to verify the correct behaviour of the circuit and also to check the correct connection of the feed back network to ensure the stability. (Cf. Figure 11c)

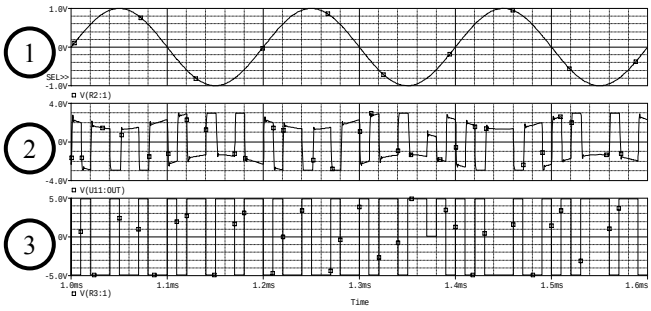


Fig. 11c: Simulated waveform in transient mode

Trace 1: input sinus signal 1V, 5 kHz (full vertical scale -1 to +1V)
Trace 2: output of comparison stage (full vertical scale -4 to +4V)
Trace 3: Scaled Modulated signal (D latch) F_e = 100 kHz, +/- 1V); full horizontal scale: 0.6 ms

FFT analysis (Cf. figure 9d) checks the conformity between the simulated spectrum and the theory. In particular, zeros appears correctly at frequencies multiples of F_e.

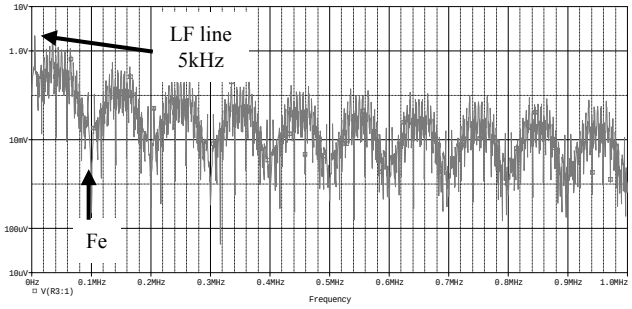


Fig 11d: Modulated output signal spectrum (FFT)

Horizontal linear scale: 1Hz ->1MHz , F_e =100 kHz,
Vertical log scale: 10µV->10V.

Both simulated curves must be compared to the figure 3b and to experimental curves in figures 13, 14.

VI. Experimental Results

The following figures show results of measurement that we performed on the hand designed board (Cf. figure examples of what the students can measure and check on the electronic wired board.

The figure 12 shows the true waveform observed on our sigma delta modulator powered in -5V, 0V, +5V.

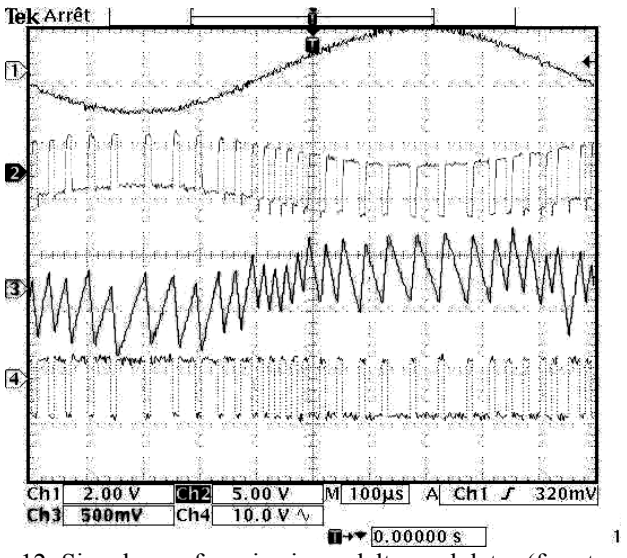


Fig 12: Signal waveform in sigma delta modulator (four traces oscilloscope Tektronix TDS 3114)

Trace 1: input sinus signal 1 kHz,
Trace 2: output of input comparison stage,
Trace 3: output of integrator stage,
Trace 4: Modulated signal (D latch),
(Horizontal scale: 0,1ms/div).

The figure 13 shows the spectrum of sigma delta modulated signal (has to be compared with figure 3b)

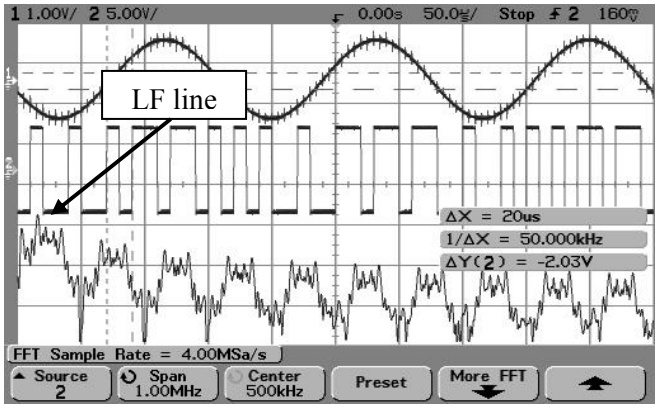


Fig 13: Modulated signal and spectrum waveform (oscilloscope Agilent 54602A)

Trace 1: input sinus signal 5 kHz (Vertical scale 1V/div)
Trace 2: Modulated signal (D latch output) (Vertical scale 5V/div)
Trace 3: Spectrum of modulated signal (100 kHz/Div)
(Fe =100 kHz)

The effect of increasing the sample frequency is shown on figure 14 by setting F_e = 800 kHz: the noise is rejected in higher frequency (as to be compared to figure 13).

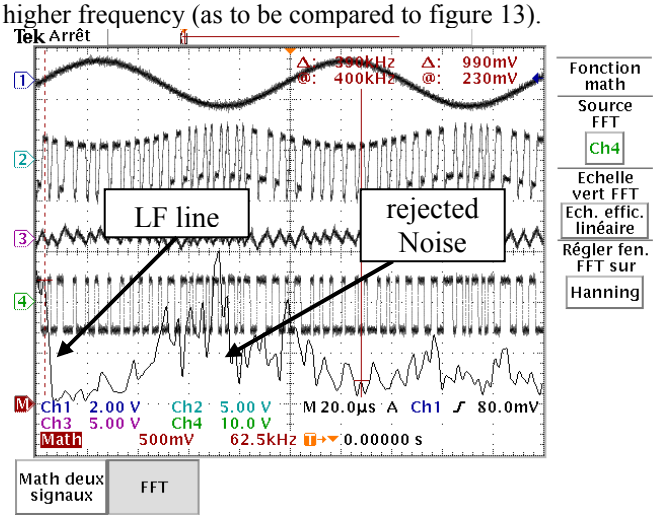


Fig 14: Impact of sample frequency value

Trace 1: input sinus signal 10 kHz
Trace 2: output of input comparison stage
Trace 3: output of integrator stage
Trace M: Spectrum of modulated signal F_e =800 kHz)

The figure 15 shows the effect of saturation (load: two ways speaker 8 Ω). When the input signal level is too high (>2V in our design), the output signal is totally "squared" and at the same frequency than the input LF signal (i.e. 10 kHz).So that a very high distortion rate appears exactly like in a linear class AB amplifier.

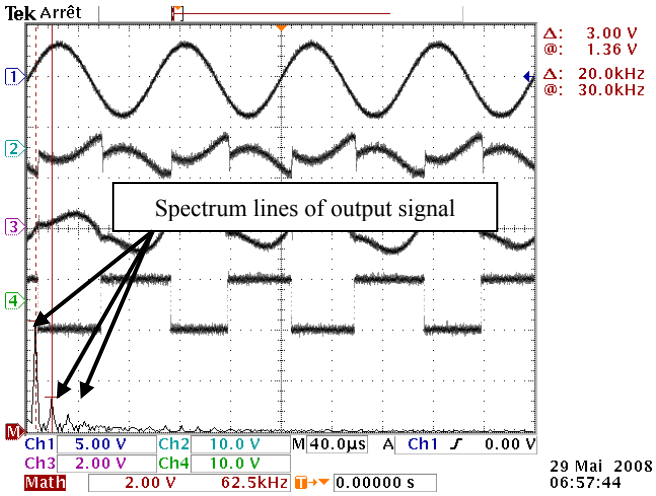


Fig 15: Saturation effect

Trace 1: input sinus signal 10 kHz
Trace 2: output of input comparison stage
Trace 3: output of integrator stage
Trace 4: output signal (squared 50% duty cycle)
Trace M: output signal spectrum (classical odd line decreasing in 1/n)

The experimental curves in figure 16 show the MOS gate control signals opposite phase on each arm. Switching times can be deduced from this observation.

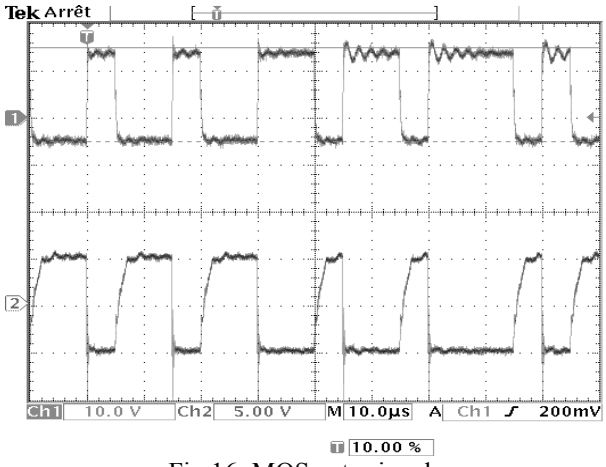


Fig.16: MOS gate signals

Trace 1: upper NMOS Gate signal (with bootstrap circuit) (Vertical scale 10V/div)
Trace 2: Lower NMOS Gate signal (Vertical scale 5V/div)

The last experimental figure 17 shows the power consumption of the amplifier at 10V H-bridge power supply with a true power wire-wound resistor load of 17 Ω instead of the speaker. Thank to the parasitic inductance of the load, it

represents perfectly the speaker's behaviour as well in audio frequencies as in high frequencies.

From similar measurements, students deduce the maximum power ratio (Cf. table 1) at 10 kHz input frequency and with a true audio load (three way speakers 8 ohms) at 3 different output useful power supply levels.

H bridge supply voltage	10V	12V	20V
Output power level	6,25 W	9W	25W
Power ratio	88%	91%	90%

Table 1: Power ratio vs. output level

Thank to the inductive behaviour of the speaker at high frequency, the useful power is dissipated only in audio LF spectrum lines.
We point out this aspect to explain to the students, the very good power ratio we obtained with class D compared to class A, or AB amplifier.

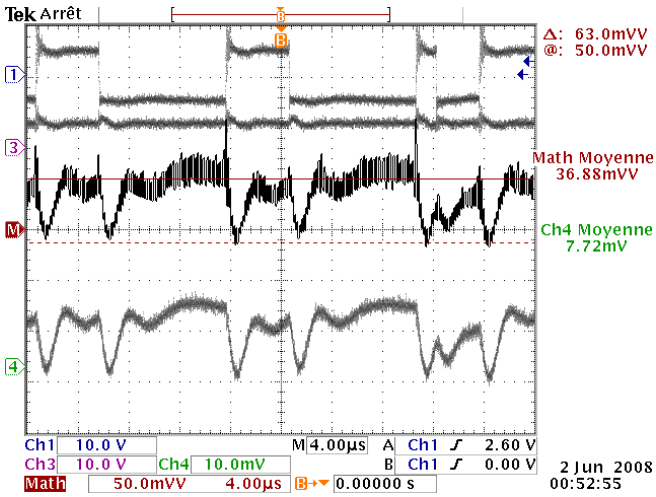


Fig 17: Power consumption

Trace 1: output modulated signal on MOS bridge (Vertical scale 10V/div)
Trace 3: H-bridge voltage supply (in this example case: 10V) (Vertical scale 10V/div)
Trace 4: supply current into the H bridge. (500mA/div) (With AM503 Tektronix DC to 100MHZ current probe)
Trace M: Instantaneous power consumption =Trace3*Trace4 (Vertical scale 5W/div).
(Resistive load = 17Ω)

Finally, a picture of the amplifier and the test bench for full audio tests, are given in figure 18a and 18b.

For safety reasons, heats sink have been added on power NMOS even they are not necessary from electronic point of view. The connexion points are mainly used to place probes, power supply and load.

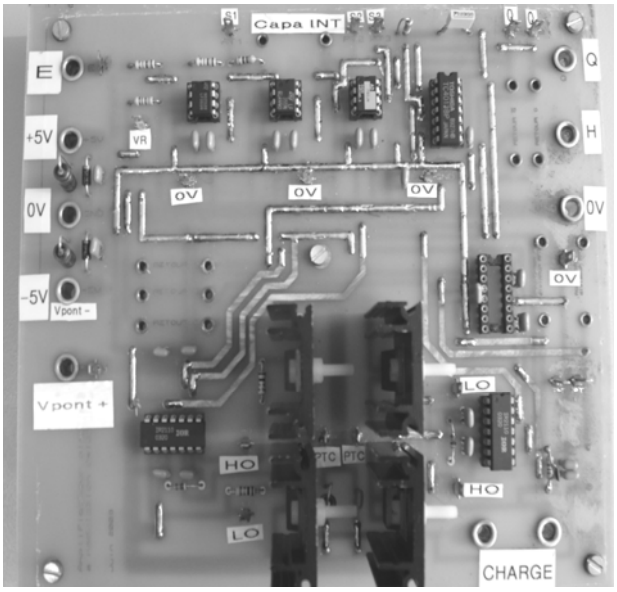


Fig. 18a: Class D amplifier board

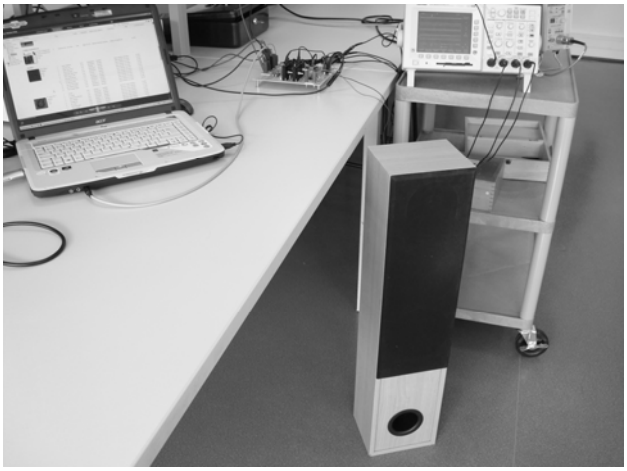


Fig 18b: View of test bench with a 100W, 8Ω, three ways speaker

VII. PEDAGOGICAL ASPECTS

A. Exporting the design method in a practical lesson for engineer students

Once the class D amplifier design tested and validated, a kind of linear « cooking guide » (based on § IV.B) has been written in order to facilitate the design of class D amplifier by the students. Then, we organized a specific optional 4 hours practical lesson as indicated in the next paragraph to test the design method.

B. Practical lesson organisation

The teacher presents first the class D subject and gives some general explanations. Then, our students compute the main components using the design strategy given in § IV.B. Then, they plug the calculated elements (integration capacitor, feed back resistors) on our electronic pre-wired circuit. And they

start the measurements in order to observe the signals in all "strategic" points of the class D amplifier. They can check some differences between the basic theory and the practical measurements (signal distortion, true switching times, parasitic oscillations and so on. They try to point out and identify the impact of each important component on global performances (power losses in particular). Finally, they understand how to improve the performances level (noise reduction for example).
Teachers ask for a written report with explanations, measurements and practical curves at the end of the lesson.

C. Student's first reaction

Despite this simplified and concrete approach, four hours of practical lesson seems too short for a majority of students regarding the numerous different electronic aspects (signal processing, power electronics, non linear feed back and so on). The global knowledge is acquired for all of the students while details are too fine and subtle to be understood in the dedicated time.

VIII. Possible Pedagogical Improvements

The aim of the pedagogical approach was first to understand the principle of the class D and then to understand how to design such amplifier. Even if the main goal has been reached, some improvement can be done.

Taking into account the students feed back, we are thinking about possible modifications:

- The first one is to start the description and the design as a course exercises in order to save time for practical lesson. This requires negotiations and coordination with the "power electronic course" manager.
- The second one is to remove some details and some measurements in the lesson such as overload protection to only focus on the "heart" of the design.
- The third one is to cut the practical lesson in two parts. But this second solution seems to be not possible because of high density of the student's time table.

IX. Conclusion

Far from the heavy and complex mathematical modelling, we presented a method to design a power switching sigma delta D class amplifier as simply as possible. Modelling the closed loop circuit at the audio frequency for small signals was the less intuitive step in this method. Thanks to this concrete approach, the students can thus make a design of a D class amplifier shortly, with an excellent efficiency.

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