Tunable LNA for 802.15.4 2.4 GHz Band for Zigbee Devices

Loay D. Khalaf, and Bassam Asir

***Abstract*—**A Low Noise Amplifier (LNA) with active inductance can be tuned over the desired operating range by changing certain variables such as the biasing voltage. A tunable LNA further reduces requirements on the blocking and linearity of a receiver by selectively amplifying the desired channel more than adjacent or alternate channels. This gain selectivity can simplify the analog to digital converters (ADC) of the receiver as well. A low noise amplifier (LNA) sometimes uses series resonance to amplify the voltage without adding noise generated by a transistor. One popular matching method for LNA's is the inductance degeneration that reflects an inductor connected to the source as a resistance at the gate. While an amplifier amplifies all the signals that fall in its band, a tuned amplifier can be selectively adjusted to change its center frequency or bandwidth, and its gain. We present a LNA in this paper that can be tuned simply by changing the biasing voltage.

***Keywords*—** Active tuned inductor, analog to digital converters, low noise amplifiers, tunable LNA, RFIC, 802.15.4, Zigbee.

I. Introduction

A modern radio front end (RFE) consists of an analog radio frequency (RF) section of minimal functionality, consisting of filtering, amplification, frequency down conversion, and an analog to digital converter, followed by a digital baseband section that performs the digital detection and synchronization [1]. The analog front end of a receiver is usually a bandpass filter and a variable gain low noise amplifier, followed by a mixer and a frequency synthesizer (variable frequency oscillator). The filter can be integrated in the LNA by using input matching sections. A widely used architecture is the inductor degenerated common source (CS) FET amplifier. This amplifier consists of an inductor in series with the FET gate, and another inductor in series with the transistor source. The source inductor looks like a resistance at the FET gate, thus the term inductive-degenerated LNA [1][2].

The loading of the amplifier is a tuned tank circuit consisting of an inductor in parallel with a capacitor. The inductors are the components with the largest areas and most dissipative (or largest thermal noise sources) [1]. Thus, it is desired to reduce the inductance, or use active inductors in LNA's [3]-[8]. However, active inductors can have higher noise figure (they produce high thermal noise), and consume more power than a passive inductor [1]. Thus, a compromise between area and power consumption is required.

The inductor in RFIC is usually of the spiral form. The area of a spiral inductor can be reduced by reducing the trace width, but that increases the skin effect resistance, and thus the noise, and lowers the Q-factor. LNA's with spiral or bond-wire inductors usually have better noise figure (NF) than active inductors, due to the fact that the active inductor transistors themselves generate noise. An active inductor greatly reduces the RFIC area, and thus the manufacturing costs. Keep in mind that the top layer thick metal used in the spiral inductors adds to the cost of manufacturing. While several authors addressed active inductor LNA [8]-[10], few presented work for tunable LNA. Zhou [12] presented a tunable LNA with center frequency around 1GHz. Our work differs in that the LNA is designed for the ISM band for personal communications, which allows a large headroom for implementation losses, but requires low power consumption for extended battery life.

Another important factor that is usually not addressed is the mixed-signal ADC and digital section complexity. The ADC dynamic range is chosen as to equalize the blocking signal requirements, i.e. the adjacent signals that falls within the input filter band when they have high energy as compared to the desired signal. If the input filter is a tuned one, then the selectivity requirements are reduced. The rule of thumb is that a one bit of the ADC is equivalent to 6 dB of dynamic range enhancement [14][16][20]. Given the datapath bitwidth and equivalent length of the digital section, and the complexity of the detection and synchronization, which in turn consumes a large section of the input power [14], a one bit reduction at the ADC is worth a compromise with an active inductor. A tunable selectivity of 12 dB can offer 2 bit reductions in the ADC requirements. The baseband requires around 6 bits for the ADC including digital signal processing and filtering for blocking signals. System analysis reveals that the 802.15.4 2.4 GHz PHY requirements give the designer a headroom around 20 dB for implementation losses [13]-[15][20][21].

Figure 1 shows a simplified block diagram of a radio front end receiver. It consists of an antenna, a bandpass filter (BPF),

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a low noise amplifier, a mixer, a local oscillator (in the form of a frequency synthesizer), and an analog to digital convertor (ADC).

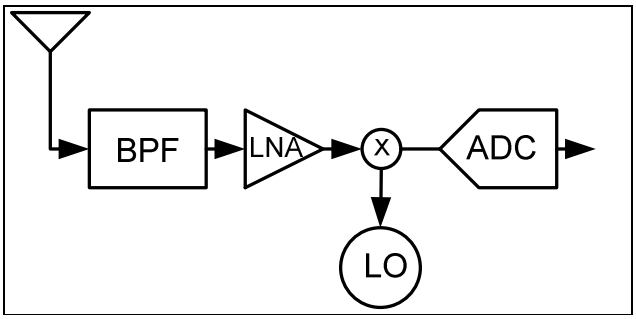

Figure 1: A radio front end (RFE)

The LNA presented here can be used in personal communication devices in the ISM band. We consider the 802.15.4 2.4 GHz Zigbee PHY, which has sixteen channels, spaced at 5 MHz, from 2405 to 2480 MHz [17].

II. Active Tuned Inductor Gyrator and Spiral Inductors

In RFIC's, spiral inductors are used often. These inductors are made from a thick metal, usually the top layer metal, of the integrated circuit manufacturing process. The thicker metal layer produces lower resistance per unit length as compared to the other layers, and thus lower thermal noise generation. The thermal noise process can be described by the following equation

$$p_n = k\,T\,B$$

where p_n is the thermally generated noise power, k is Boltzman's constant (1.38 10^{-23} / Hz/ K), T is the temperature in Kelvin (K), and B is the bandwidth (the measurement bandwidth) [1]. As can be seen, the factor that can reduce the thermal noise is the temperature, thus cooling a device can reduce its generated noise power. However, it is not feasible to reduce the temperature of a consumer device below room temperature. Regarding the bandwidth, it is desired to make the receiver bandwidth the same as the desired channel bandwidth. However, that is not simple, mainly due to the fact that the receiver is a narrowband (NB) device, and the components have some tolerances. The tolerances are few parts percent, while the channel bandwidth to the carrier is few parts per million (PPM). Low tolerance, or precision, devices are expensive to manufacture. Thus, we are left with a large bandwidth, which for our case is the complete 2.45 to 2.48 GHz, when using a direct conversion receiver [1].

The resistance is not obvious from the above equation, but when we consider maximum available power delivered to the load (which is the LNA of the receiver in our case), the following equation is used

$$V_n = 4\,k\,T\,B\,R$$

where V_n is the thermal noise voltage when the resistance of the load is matched to that of the generator (or the antenna in this case).

Spiral inductors consume a large area. Actually, the area of one spiral inductor can be as large as that of tens of thousands of transistors for a 0.5 um technology, and to hundreds of thousands for current technologies. The area of the spiral inductor can be computed from the inductance and metal properties. Approximate spiral inductance formulas are elaborate and can be found in [1].

For more accurate results, the spiral inductor requires extensive electromagnetic (EM) solver calculations for more precise values. The EM calculations take into consideration conductor dimensions, layout, coupling with adjacent turns, etc. These calculations are usually performed using expensive EM software packages. EM solver data can be converted into equivalent circuits that can be used in SPICE simulations. Figure 2 shows a spiral inductor.

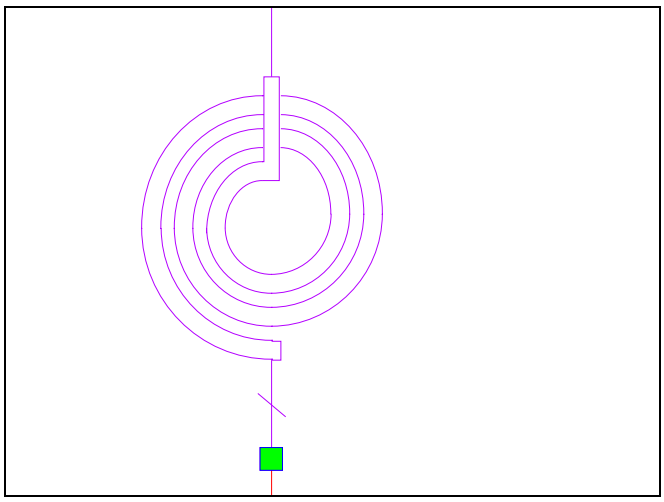

Figure 2: Spiral inductor

The spiral inductor equivalent circuit is shown in Figure 3 [1]. Extraction of the corresponding values for the equivalent circuit can be performed with some additional effort. However, accurate models and tolerances requires expert work.

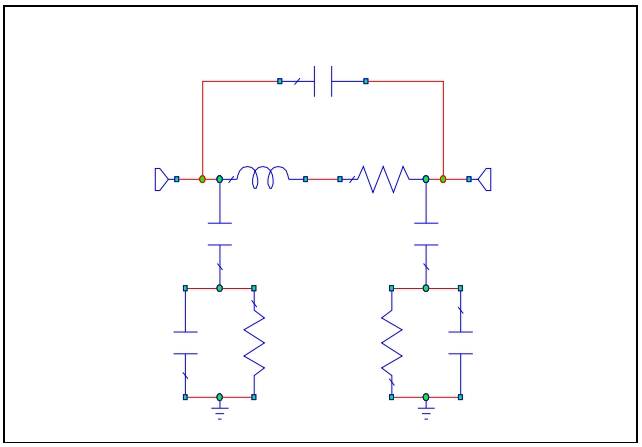

Figure 3: Spiral inductor equivalent circuit

Active inductors at low frequencies are synthesized using opamps. Most low frequency filters use opamps together with capacitors and resistors and avoid inductors. opamps contain a large number of transistors, and at high frequencies, this affects their maximum bandwidth. Instead, gyrator-C active inductors can be used. A gyrator is a circuit with two transconductors connected back-to-back [9]. A gyrator-C inductor consists of a gyrator and a capacitor, as shown in Fig. 4. The operation of the gyrator-C inductor can be easily explained in the frequency domain, where the impedance of a capacitor is a negative pure imaginary number, and that of the inductor is positive. By applying a negative sign to the capacitance, or a 180 degrees phase shift, the capacitor negative impedance can be turned into an equivalent inductance impedance. A straightforward analysis reveals that the capacitor is reflected into an equivalent inductor at the circuit input according to equations (1) and (2) below.

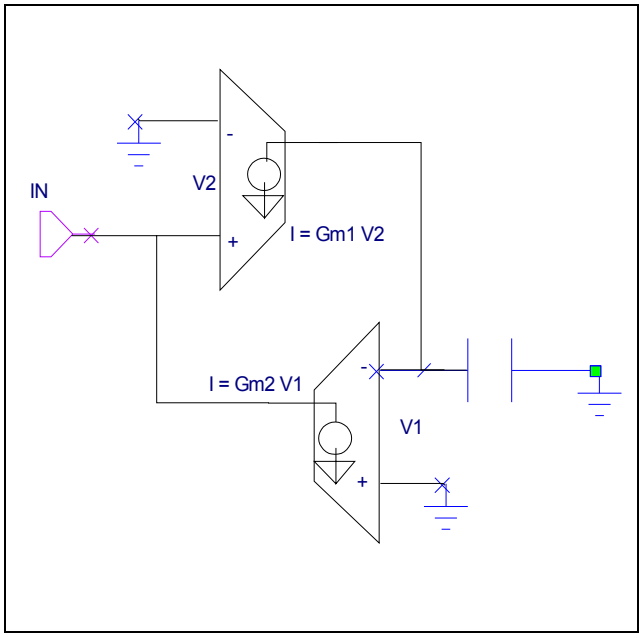

Figure 4: Gyrator-C inductor

The gyrator transconductors can be made from two NMOS FET transistors, as shown in Fig. 5, biased into the saturation region. The size of the transistors, their bias voltage, or their transconductance need not be the same. This allows the designer to use one transistor for tuning, by changing its bias voltage, and thus its transconductance. Of course, the two transistors can be tuned as well. The biasing condition can be controlled by a digital to analog converter (DAC) that is controlled by the baseband controller. Tuning algorithms include center channel frequency and variable LNA gain are discussed in communication courses [18]-[20]. The negative sign can be implemented by a CG amplifier, which has a phase shift of 180 degrees for its voltage gain.

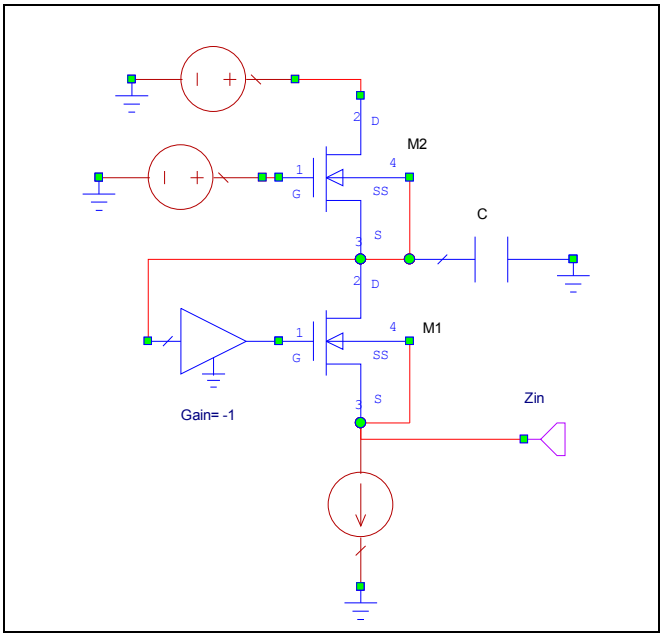

Figure 5: Gyrator active inductor

The inductance is governed by the following formulas [9]

$$Z_{in} = \frac{s\,C}{G_{m1}\,G_{m2}} \qquad (1)$$

with the inductance component as

$$L = \frac{C}{G_{m1}\,G_{m2}} \qquad (2)$$

It is clear how changing the transistor's transconductance leads to changing the inductance value of network, with a reciprocal relation. Keep in mind that the transconductance is related to the device parameter, specifically, the bias current and device width.

The quality factor of inductors with few nano Henries is in the range of 5 to 20, and it decreases as the inductance is made larger, since the larger inductance requires a longer length conductor. A longer conductor has a larger resistance, which will ultimately cause a larger thermal noise.

Active inductors can have a much larger quality factor than the spiral inductors mostly used in RFIC's, since they do not require a long length conductor and thus a corresponding resistance. However, spiral inductors can be made to have less noise generation as compared to the noise generated by the active inductors. The reason is due to the fact that the MOSFET transistor generates its own noise, due to the discrete nature of charge as in shot noise, and due to channel resistance [1].

On the other hand, the active inductor can suffer from nonlinear behavior if the input signal increases above some threshold. This is a major factor in wireless receivers, since the incoming signal can have a dynamic range of 50 dB's or more as the receiver is moved away from the transmitter [1][19][20]. Equation (3) below shows the dependence of Gm on the current through the transistor in the saturation region, and mostly for the small signal linear region, we assume that Gm is linear in Vgs. However, changing Gm causes the active inductance to change. Compare this to a real inductor with constant inductance that does not depend on the voltage across the inductor.

$$g_m = \sqrt{2\,\frac{W}{L} C_{ox} I_D\,\mu_n} \qquad (3)$$

Further, the large dynamic range of the input signal can drive the transistor in its triode region. Thus, as the biasing voltage increases, the current increases nonlinearly, and thus the transistor transconductance.

The main qualities that the active inductor posses over the spiral inductor are tunability, size, design, and manufacturing simplicity. The tunability of the active inductor can be compromised with the tolerances of the manufacturing process. The tunability also allows for selectivity in the receiver bandwidth for different channels, and lower noise and higher blocking capability. While the tenability requires extra control circuit, such as an analog to digital convertor, the area required by such circuits is much less than the spiral inductor area. (and thus its manufacturing costs), and the fact that the tunable inductor value can be changed in the field, as compared to a spiral inductor that needs EM simulation and RFIC design re-spin in case the inductance was not as obtained in simulations.

III. LNA Design Procedure

The design of an LNA might have conflicting goals, such as input and output impedance matching and noise figure. Generally, the optimal impedance for the noise figure is different from the optimal impedance for power gain [1][19]. The actual design is a compromise between power gain, power consumption, and noise figure. Here we follow the design procedure outlined in [19].

LNA design can start either with impedance match then power gain and noise figure, or noise figure then power gain and impedance matching. Other methods can be used including S Parameter based procedures that are generally used in microwave circuit design [19].

In a CS inductive degenerated LNA, as shown in Fig. 6, three inductors are used, with two for input impedance matching, and one for the output tank circuit load.

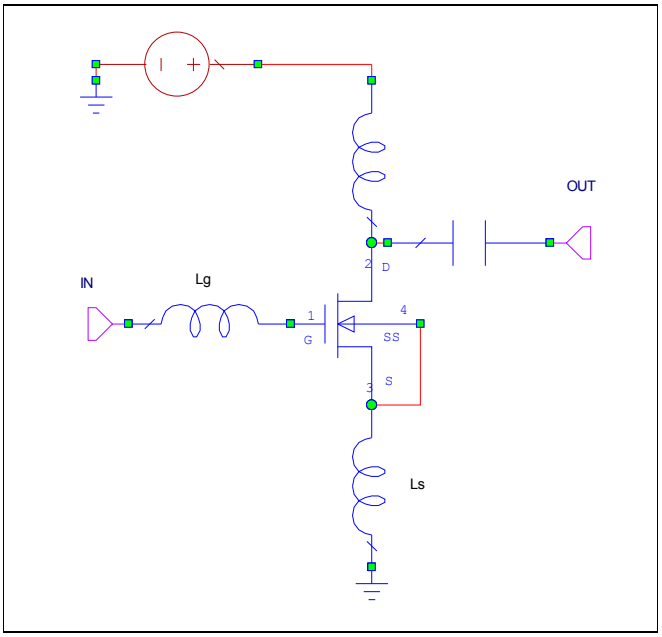

Figure 6: Inductive degenerated LNA

Using the procedure of impedance matching first, and given the input impedance and resonant frequency, the inductor values at the input can be easily computed from the following equations [19]. First, assuming the unity-gain frequency of the radio frequency integrated circuit (RFIC). We can compute the source inductor value from equation (4)

$$L_s = \frac{R_{in}}{\omega_t} \qquad (4)$$

where the unity-gain frequency is given as

$$\omega_t = \frac{G_m}{C_{gs}}$$

Next, the gate inductor value is computed from the NF using equation (5) below

$$NF = 1 + \frac{2}{3}\frac{1}{1+\frac{L_s}{L_g}} \qquad (5)$$

Finally, the gate capacitance, or the gate channel width is computed from equation (6) below

$$(L_s + L_g)C_{gs} = \frac{1}{(2\pi f)^2} \qquad (6)$$

Where R_{in} is the input impedance, usually 50 Ohms, G_m is the transistor transconductance, L_s is the inductor at the source, L_g is the inductor at the gate, and C_{gs} is the capacitance of the gate-to-source. The total load inductor is usually resonated at the desired carrier frequency using the parallel impedance formula as

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad (7)$$

The gate-source capacitance depends on the transistor channel area, as given by the equation

$$C_{gs} = \frac{2}{3} W L C_{ox} \qquad (8)$$

Finally, the voltage gain of the degenerated inductor LNA is given in terms of the tank circuit inductor L_t, and capacitor, C_t, by

$$A_v = \frac{1}{j\omega L_s}\frac{j\omega L_t}{1-\omega^2 L_t C_t} \qquad (9)$$

The series network of the gate inductor and the capacitance of the gate of the FET act to amplify the signal voltage at the gate by the Q factor of the network, without adding noise.

The active tuned proposed LNA is shown in Fig. 7 below.

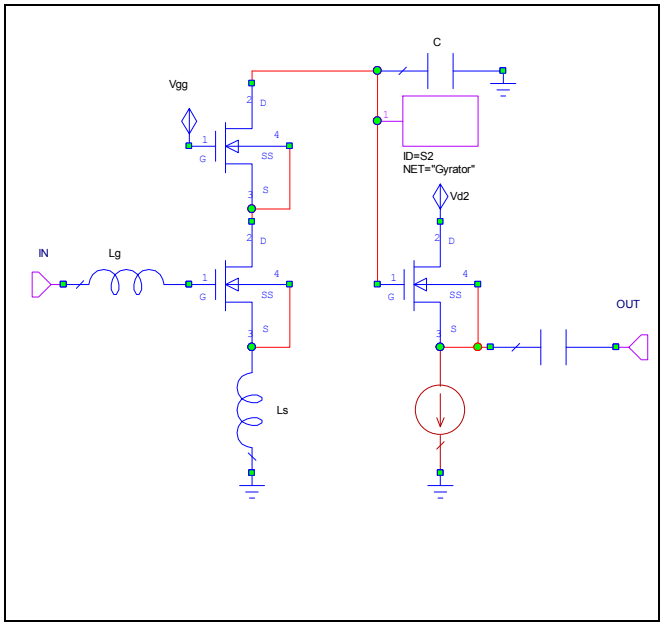

Figure 7: Active tuned LNA

The amplifier architecture is that of a cascade type, with the input stage as a common source loaded by a common gate. The common gate cascode acts to reduce the Miller capacitance thus increasing the bandwidth. The input matching and low noise is performed by the source degenerated inductor, and the gate inductance. The active inductor is connected to the drain of the common gate, where it replaces the inductor of the tuned tank circuit. The output stage is that of a common drain acting as a buffer stage.

The analysis equations are similar to the common source LNA discussed above. Same equations are used for the gate and source inductors, and voltage gain.

IV. Simulation and Results

This section presents the simulation results obtained from SPICE and Harmonic Balance Simulators for the active tuned LNA.

A. LNA Gain - Scattering Parameters

It is desired to minimize power reflection at the input, as can be indicated by the input reflection coefficient scattering parameter S_{11}. Usually, a standard input impedance of 50 Ohms and a value of -10 dB is sufficient [19]. The gain of the first stage of the receiver is desired to be high, and its noise figure to be low, since it is the most influential factor of the overall system noise figure. The gain is indicated by the insertion gain scattering parameter, S_{12}, again using a standard impedance of 50 Ohms at the input and output, with a gain of 10 to 20 dB [1]. The proposed LNA S-Parameters for a 2.455 GHz midband frequency is shown in Fig. 8 below. A selectivity around 12 dB for the S_{12} at 2.455 GHz to that at 2.405 GHz can be read from the figure. The gain is around 42 dB. For extremely low input signals (down to -85 dBm), further gain can be provided by the following sections of the receivers, such as another amplifier stage and the mixer. However, the noise figure of the following stages can be relaxed, since it is not of much importance as the first section.

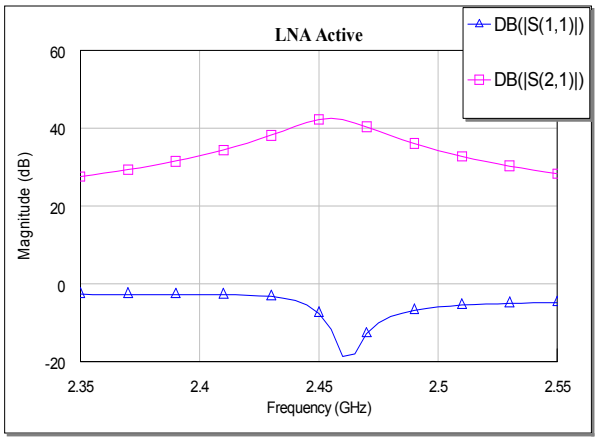

Figure 8: Tuning response at 2.455 GHz

We see in Fig 8 that maximum gain is at 2.455 GHz is around 40 dB, while away from this maximum at 2.48 GHz, the gain drops to around 30 dB. Thus, the signal at the 2.48 GHz channel looks attenuated by over 10 dB, which can be looked at as extra blocking capability of 10 dB. This can also be seen in Fig.9, where extra selectivity can be observed from the maximum at 2.48 GHz as compared to the 2.45 GHz. Similar observations can be seen in Fig. 10.

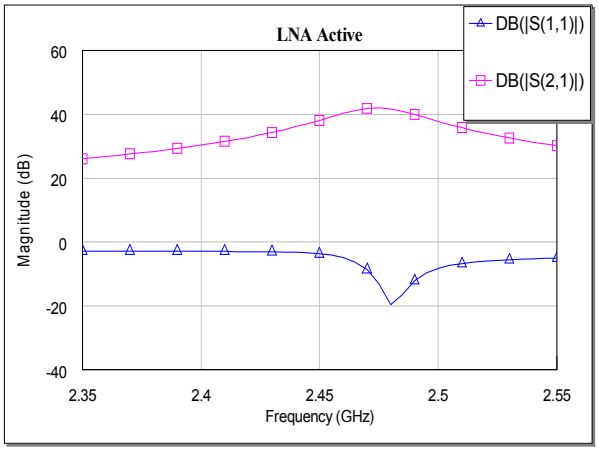

Figure 9: Tuning response at 2.48 GHz

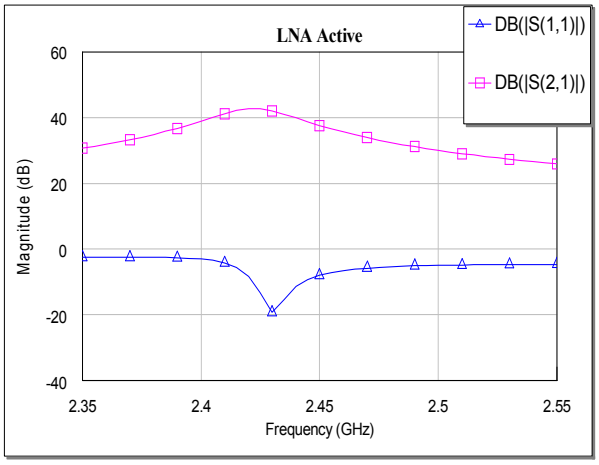

Figure 10: Tuning response to 2.42 GHz

B. Noise Figure

The 802.15.4 Zigbee Phy standards for personal communication devices is geared towards low cost consumer devices. This provides for a great deal of implementation loss headroom and simplifications. More than 10 dB of NF can be afforded in the receiver as shown in [16] [20].

The Noise Figure of the device is shown in Fig. 11 and Fig. 12, for two representative center frequencies, as shown. The NF does not exceed 5.8 dB starting at 2.4 GHz, which leaves a great deal of simplification for the baseband digital demodulator.

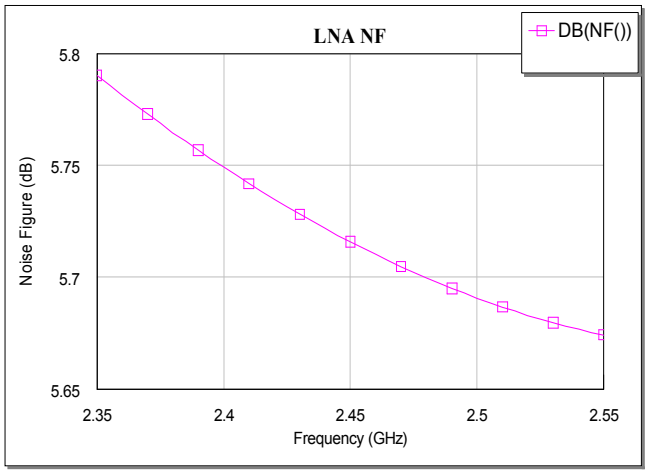

Figure 11: NF at center frequency of 2.42 GHz

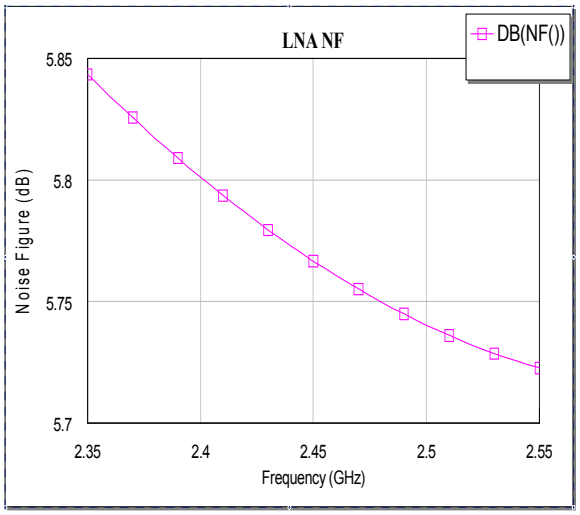

Figure 12: NF at center frequency of 2.48 GHz

C. *Power Consumption*

The simulated power consumption (DC) of the LNA is around 3.9 mW. This is a very low value due to the 0.18 micro-m technology and the large gain of the resonant LC network (large Q factor) at the input of the LNA.

D. *Comparisons to similar publication*

Table 1 shows comparisons to other published low noise amplifiers using active or tuned inductors. The proposed LNA provides an acceptable noise figure with minimal power consumption as compared to other works.

Table 1: Comparisons to other LNA's

Reference	Tech. Micron	NF (max) (dB)	Power (mW)
This work	0.18	5.8	3.9
Nair [4]	0.18	6.7	7.1
Reja [7]	0.13	4	13.5
Zhou [8]	0.50	3.65	14

V. Conclusion

It was demonstrated how active inductors can be used in tuned low noise amplifiers to reduce LNA area, dynamic range of the ADC, and the bit width of the baseband digital signal processing circuits, leading to reduced power consumption and reduced manufacturing costs. This method is very useful in personal wireless links such as Zigbee and Bluetooth where the implementation losses are of several dB's by the standards.

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