Flexible FPGA-based BPSK Signal Generator for Space Applications

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***Abstract*—**This paper presents the implementation of a versatile BPSK (Binary Phase Shift Keying) signal generator targeted to FPGA (Field Programmable Gate Array). The proposed model, taking advantage of the intrinsic flexibility of reprogrammable logic devices, allows adjustments to be made to the BPSK signal parameters such as amplitude, carrier frequency and bit rate. It additionally allows the insertion of the following propagation channel effects: frequency shift, phase shift, time delay and additive noise. Following a practical and fast methodology for the FPGA design flow, the attained results show that the signal generator architecture can be efficiently developed and reconfigured according to the application requirements. Another remark of this BPSK signal generator is the excellent balancing of phase and amplitude, a property that is hardly feasible with traditional modulators. These achievements represent a technological improvement from the perspective of applications that demand robust communication systems to be tested and validated against space channel impairments.

***Keywords*—** FPGA, Phase Shift Keying, Signal Generator, Space Channel.

I. Introduction

BPSK (Binary Phase Shift Keying) is a digital modulation technique that offers the best performance concerning bit error rate for power-limited systems [1]. For this reason, this modulation scheme is recommended by CCSDS (Consultative Committee for Space Data Systems) for the earth-space communication in telecommand links [2]. CCSDS recommends BPSK modulation for all telecommand systems, regardless the transmission speed and the mission category.

Considering the demands for highly complex satellites in the near future, the Instituto Nacional de Pesquisas Espaciais (INPE) is developing a BPSK modem with suppressed carrier, as recommended by the CCSDS, for high transmission capacity telecommand systems (up to 2048 kbps)**.** The BPSK modulated signal must be generated at an intermediate frequency (IF), nominally at 70 MHz, and after that, it is up-converted to be transmitted in the S-band (2 – 4 GHz).

In this paper it is presented a model of a BPSK signal generator designed to operate on earth and validate an onboard demodulator of the high capacity telecommand system being developed by INPE. The proposed generator is able to implement the imperfections introduced in the transmitted signal by the space channel [3]. Specifically, the most significant impairments of the space channel for this kind of system are the Doppler effect and the thermal noise at the receiver [4]. Therefore, it is possible to select frequency, phase and delay offsets, as well as to add AWGN (Additive White Gaussian Noise) to the generated BPSK signal. Furthermore, the design is flexible enough to allow changes in signal and noise amplitude, bit rate and the carrier frequency. As the modulation is performed at the IF stage, almost all the BPSK signal generator can be implemented using DSP (Digital Signal Processing) techniques [5].

The proposed solution is an entirely flexible DSP-based project, which exploits the benefits of a practical methodology for the FPGA (Field Programmable Gate Array) design flow [6], [7], based on Xilinx's *System Generator* graphical interface. Through *System Generator* it is possible to create the FPGA configuration file, known as bitstream, directly from a simulation environment, like Mathworks' *Simulink*, without the need for HDL (Hardware Description Language) implementation by the designer.

This article is organized as follows: The general architecture of the BPSK signal generator and its implementation is described at the methodology section; The outcomes for both simulation and hardware tests are shown at the results section; and, finally, conclusions are presented at the discussion section.

II. Methodology

A. Signal Description

The generated BPSK signal may be expressed by:

$$s(t) = A[\sum_{n=0}^{\infty} x[n]g(t-nT+\tau)]\cos[2\pi(f_c+f_d)t+\phi]+n(t), \qquad (1)$$

in which A, T, τ, f_c, f_d, and ϕ represent the amplitude, bit duration, symbol delay, carrier frequency, frequency error and phase error, respectively. The term $g(t)$ indicates a base-band pulse, which is a rectangular pulse in accordance with the CCSDS. The signal $x[n]$ represents the BPSK symbol and may assume values of +1 or -1. The Gaussian noise is denoted by $n(t)$ and has zero mean and a given power spectral density [1].

This work was supported by the Agência Espacial Brasileira (AEB) and Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq).

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The generated signal $s(t)$ can also be represented by:

$$s(t) = A[\sum_{n=0}^{\infty} x[n]g(t - nT + \tau)][\cos(2\pi f_d t + \phi)\cos(2\pi f_c t) - \sin(2\pi f_d t + \phi)\sin(2\pi f_c t)] + n(t). \tag{2}$$

It is important to note that $s(t)$ is generated through digital signal processing in FPGA, and for that reason, $s(t)$ is a result of a D/A (Digital-to-Analog) conversion of a discrete signal, $s[k]$. Fig. 1 depicts the structure of the proposed generator. The discrete version of the BPSK signal, $s[k]$, is generated inside the FPGA and it is then applied to a D/A converter, resulting in the analog signal $s(t)$.

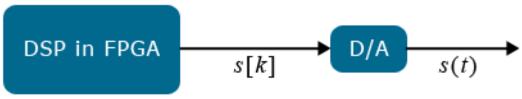

Fig. 1. Discrete BPSK signal, s[k], generated through DSP in FPGA and its analog version, s(t), after D/A conversion.

Assuming $t = k/f_s$, where f_s represents the sampling frequency, $s[k]$ can be expressed by:

$$s[k] = A[\sum_{n=0}^{\infty} x[n]g(\frac{k}{f_s} - nT + \tau)][\cos(2\pi \frac{f_d}{f_s} k + \phi)\cos(2\pi \frac{f_c}{f_s} k) - \sin(2\pi \frac{f_d}{f_s} k + \phi)\sin(2\pi \frac{f_c}{f_s} k)] + n[k]. \tag{3}$$

Fig. 2 shows a block diagram of the BPSK signal generator based on (3).

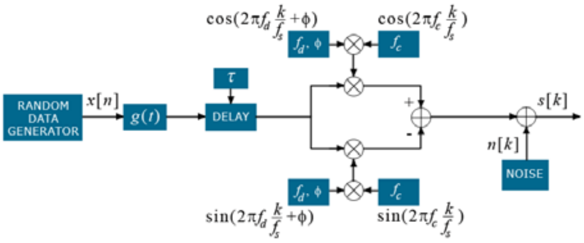
$\cos(2\pi f_d \frac{k}{f_s} + \phi)$
$\cos(2\pi f_c \frac{k}{f_s})$
f_d, ϕ
f_c
τ
RANDOM DATA GENERATOR
x[n]
g(t)
DELAY
+
-
s[k]
n[k]
NOISE
f_d, ϕ
f_c
$\sin(2\pi f_d \frac{k}{f_s} + \phi)$
$\sin(2\pi f_c \frac{k}{f_s})$

Fig. 2. Block diagram of the circuit that generates the discrete BPSK signal, s[k].

In the following sub-section the implementation of the FPGA-based BPSK signal generator is detailed.

B. *Detailed Functional Description*

This work is focused on the implementation of a circuit that is physically generated through automated synthesis tools taking as input a model of the system in a simulation environment.

Initially, a model [8] was developed with Mathworks' *Simulink*. This model served as a base circuit for testing and validating both the signal generator functional implementation and the space channel propagation effects.

The architecture of the BPSK signal generator, in the *Simulink* environment, is represented by the high-level diagram of Fig. 3:

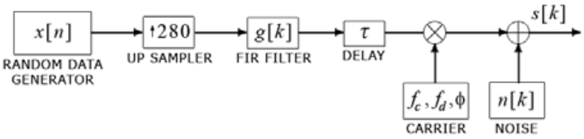

Fig. 3. High-level diagram of the BPSK signal generator in the Simulink environment.

Below we describe the function of each block:

- RANDOM DATA GENERATOR: Responsible for the generation of random +1 and -1 values at the sampling rate, simulating transmitted symbols;
- UP SAMPLER: Inserts 279 copies of each incoming sample at a rate 280 times higher than the input one;
- FIR (Finite Impulse Response) Filter: Implements a rectangular filter with unit amplitude and 280 taps;
- DELAY: Delays the input signal through linear interpolation;
- CARRIER: Generates a discrete sinusoidal waveform with frequency and phase errors;
- NOISE: Provides AWGN samples.

After validating the prototype illustrated in Fig. 3 through exhaustive simulations, the next step was its conversion to an FPGA description, i.e., re-designing the system so that it could be synthesized into a circuit that is loadable in an FPGA. To accomplish that, Xilinx's *System Generator* was used. Fig. 5 exposes the entire system in the graphical environment of *System Generator*.

Among the various implemented blocks, one can cite: LUT (Look-Up Table) blocks, multiplexers, adders, filters, interpolators, multipliers and delay blocks, properly organized and connected in such a way that produce a BPSK signal that holds most of the imperfections of a space channel [4]. Hereafter, each block that composes the BPSK signal generator will be explained.

The random data generator which represents the information signal was implemented as shown in Fig. 4 and allows configurable bit rate. The configurable counter block provides the address locations to the LUT. This LUT, as a memory, is filled with a random bit at each address location. The random binary value is obtained from the combination of *Matlab* functions `round()` and `rand()`.

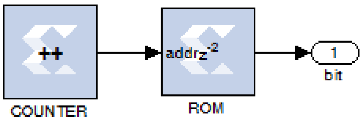

Fig. 4. Random Data Generator block comprised of a counter and a look-up table with preloaded values.

The output of the Random Data Generator block is connected to the Bipolar Encoder block which performs the conversion of binary digits into a signal whose amplitude

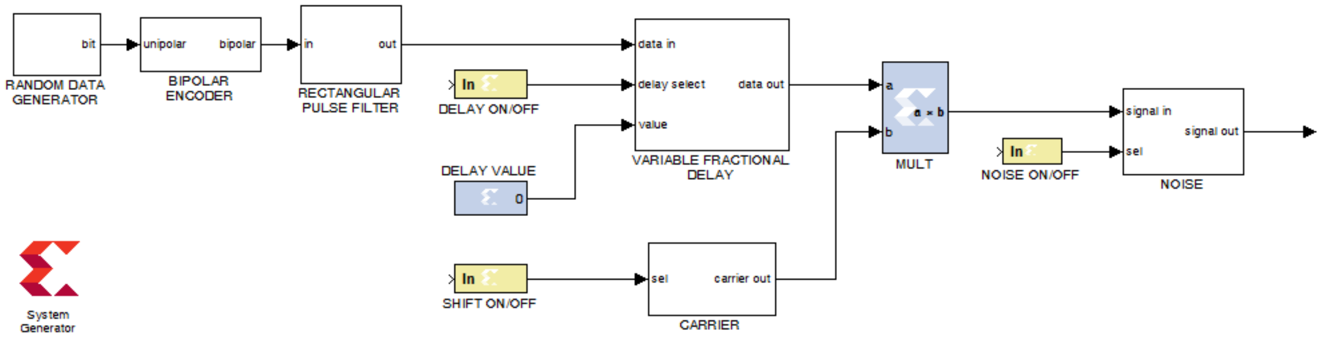

Fig. 5. Top-level circuit of the BPSK signal generator in the System Generator environment.

assumes either +1 or -1 values. The Bipolar Encoder block was implemented as shows Fig. 6.

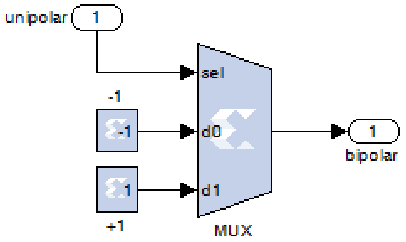

Fig. 6. The Bipolar Encoder block expanded. A multiplexer and two constants compose the encoder.

The output of this encoder is applied to the Rectangular Pulse Filter as indicated in Fig. 5. The rectangular pulse filter, using a native *System Generator* block, increases the input signal's sampling rate by a factor of $4f_cT$.

The next stage in the modulation process, following the diagram in Fig. 5, is the insertion of the time delay that is one of the space channel impairments. This is accomplished in the Variable Fractional Delay block. Fig. 7 illustrates the implementation of such block, which is composed of register blocks, adders and a multiplier that, together, perform a linear interpolation.

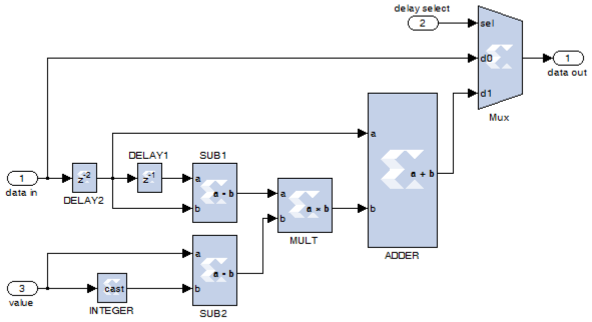

Fig. 7. Detailed implementation of the Variable Fractional Delay block. Adders, multipliers, subtraction and delay blocks perform linear interpolation of the input signal.

The implementation of the Variable Fractional Delay block allows the switching between two situations: "0" representing no delay added to the signal; and "1" for the opposite situation. The value of this delay is user-configurable.

The remaining steps of the generation of the BPSK signal are the multiplication with the carrier wave and the addition of Gaussian noise. The generation of the carrier wave is done in the Carrier block (see Fig. 5). Frequency and phase shifts are also performed in this block. Fig. 8 presents the circuit that generates the carrier wave.

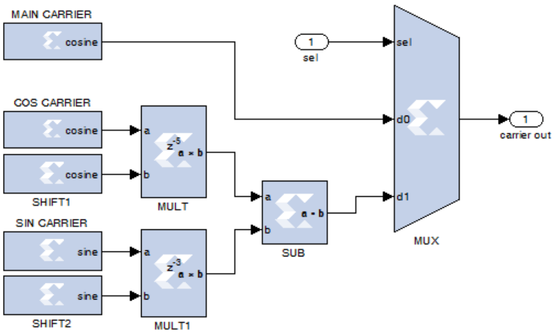

Fig. 8. The Carrier block with selectable phase and frequency shifts.

The Carrier block implementation allows the selection between two situations which are mathematically described as:

$$c[k] = \begin{cases} \cos(2\pi f_c \,{}^{k}\!/\!{}_{f_s}), & sel = 0; \\[2ex] \cos(2\pi f_d \,{}^{k}\!/\!{}_{f_s} + \phi)\cos(2\pi f_c \,{}^{k}\!/\!{}_{f_s}) \\ -\sin(2\pi f_d \,{}^{k}\!/\!{}_{f_s} + \phi)\sin(2\pi f_c \,{}^{k}\!/\!{}_{f_s}), & sel = 1. \end{cases} \tag{4}$$

By (4) we understand that when the input signal, *sel*, is equal to 0, the output signal is a pure carrier wave with frequency f_c. The opposite situation, when *sel* equals 1, adds a frequency error, denoted by f_d, and a phase error, represented by ϕ. The cosine and sine waves are generated by look-up tables, as illustrated in Fig. 8.

Finally, in the Noise block, the amount of noise to be added to the modulated signal is selected among many SNR (Signal-to-Noise Ratio) configurations. One can choose from 0 to 10 dB options for Signal-to-Noise ratio. Fig. 9 details the implementation of the Noise block.

A native *System Generator* module generates a noise signal with Gaussian characteristic. This noise source is built with the combination of the Box-Muller algorithm and the Central Limit Theorem and is able to output a 12-bit signed fixed-point value.

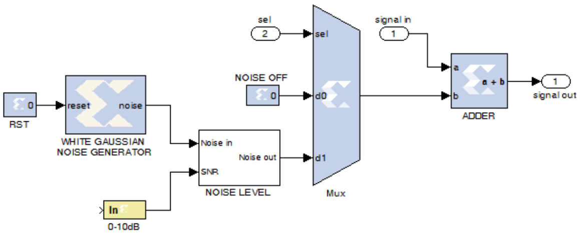

Fig. 9. The circuit that implements the Noise block. SNR and the presence of noise are selectable within this block.

The Noise Level sub-module controls the amplitude of the noisy signal so that it reaches a particular signal-to-noise ratio in relation to the power of the input modulated signal. A multiplexer enables the addition of noise to the input signal.

The following section presents the results obtained from both simulations, with *System Generator*, and from the real hardware test. It is noteworthy that for the validation of the proposed model with a real hardware implementation, it was used an FPGA development kit [9], a D/A converter board [10], an oscilloscope and a spectrum analyzer.

III. Results

This section presents the results from the simulations and circuit experiments of the proposed BPSK signal generator model. For the simulation runs, it was used the graphical environment of Xilinx's *System Generator* integrated with Mathworks' *Simulink*. For the hardware tests, we used the ML605 development kit, from AVNET [9]. It is equipped with a Virtex-6 FPGA with more than 240 thousand logic elements.

The simulation parameters were defined as:

- Symbol Rate: $1/T = 1$ Mbps;
- Carrier Frequency: $f_c = 50$MHz;
- Frequency Shift: $f_d = 10$ Hz;
- Phase Shift: $\phi = \pi/6$;
- Signal-to-Noise Ratio: SNR = 50 dB.

As described in Fig. 1, the discrete signal generated in the DSP section of the system is applied to a D/A converter. This converter consists of an additional piece of hardware [10] and is attached to ML605 through an FMC (FPGA Mezzanine Card) connector. Fig. 10 shows the test bench where it can be seen the main board (ML605), the additional D/A converter attached (FMC150), and a 4-channel oscilloscope from Agilent.

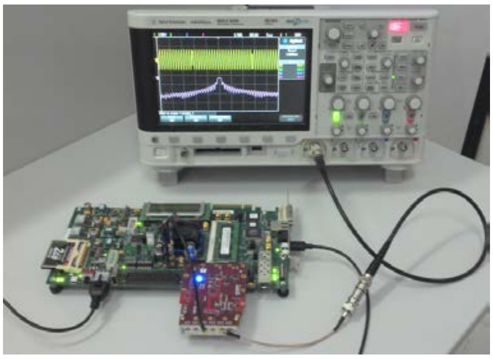

Fig. 10. Test bench showing the BPSK signal generator running in FPGA. The oscilloscope screen shows the input signal both in the time (top) and frequency (bottom) domains.

The results from the simulations are presented as follows. Fig. 11 depicts the analysis, in the time domain, of the discrete output of the BPSK signal generator. In this picture it is seen a reference waveform (at the top), without noise, frequency or phase errors, nor delays; in the middle, a delayed version of the reference signal; and a third version with frequency and phase errors added (at the bottom).

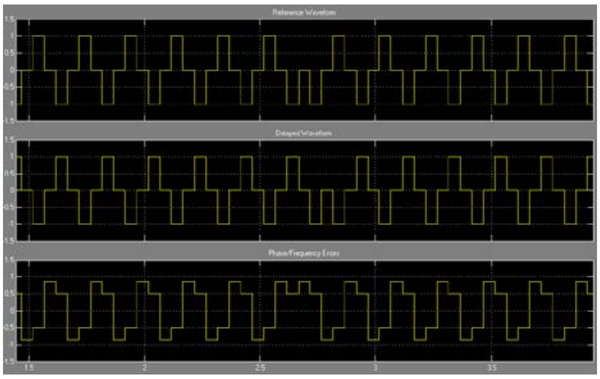

Fig. 11. Time-domain analysis of the discrete BPSK signal. Reference waveform (top). Delayed version of reference waveform (middle). Reference waveform with phase and frequency errors (bottom).

One can observe, from the signal at the top, a transition from the symbol +1 to symbol -1 represented by a change in the phase of the carrier wave. The waveform in the middle shows exactly the same signal, but delayed 56 samples. The last waveform shows a version of the signal distorted by frequency and phase errors. It is noticeable the perfect matching of amplitude and phase, as can be seen comparing the waveforms before and after a symbol transition. Such performance, in relation to phase and amplitude balancing, is hard to achieve with traditional analog implementations of BPSK modulators.

Proceeding with the presentation of the test results, it is shown, in Fig. 12, the BPSK signal spectrum. It can be seen a high similarity from this simulation output to the practical measurement with a spectrum analyzer (Fig. 13). In both pictures, the frequency is centered at 50 MHz and the span is defined at 10 MHz.

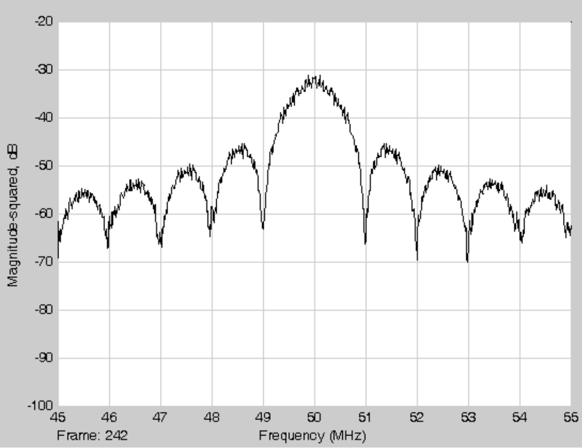

Fig. 12. Spectrum analysis of the BPSK signal in the System Generator environment.

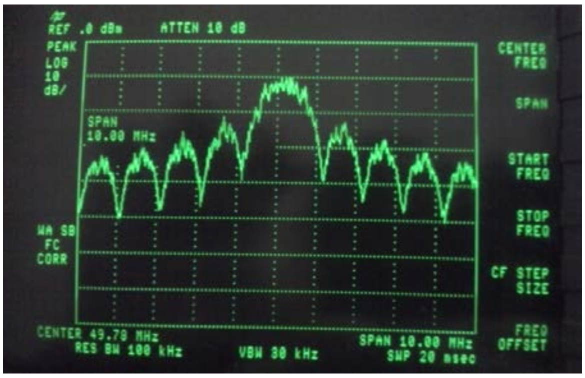

Fig. 13. Spectrum analysis of the BPSK signal in a Spectrum Analyzer.

Finally, Fig. 14 illustrates the time-domain analysis of two signals obtained from the D/A converter outputs. The upper waveform shows a reference signal with no errors and two symbol transitions. The lower waveform represents the same signal but with Gaussian noise (SNR = 8 dB) added.

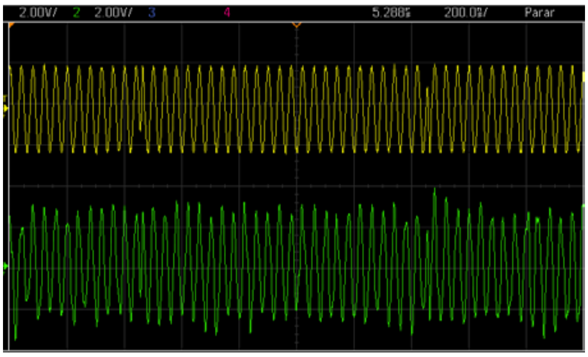

Fig. 14. Time-domain analysis of the BPSK signal with an oscilloscope. Reference waveform (top) showing two symbol transitions. (Bottom) Reference waveform with added Gaussian noise (SNR = 8dB).

IV. Conclusion

This paper presented a BPSK signal generator implemented in FPGA following an efficient methodology. The proposed model allows the insertion of the most common space channel distortions into the modulated signal. Every module in the BPSK signal generator was implemented through a design methodology based on automated circuit synthesis which allows fast prototyping of mathematical models.

The FPGA-based BPSK signal generator represents a technological improvement on the perspective that it enables telecommand systems, employed in space applications, to be flexibly tested against propagation effects existent in the space channel. The flexibility of this system is also evinced by the way how changes in some modulation parameters, such as carrier frequency, phase errors and noise addition, are performed.

Results show that the BPSK signal generator exhibits optimum performance with respect to spectrum characteristics, amplitude balancing and phase transitions in the time domain. The generator was validated for a broad range of frequencies up to the carrier frequency of 70 MHz, although other frequencies and bit rates might certainly be adopted.

Another remark of this work was the adoption of an efficient design methodology, in addition to the development of a parameterizable BPSK signal generator based on the concepts of digital signal processing aimed to reprogrammable logic devices. Future efforts might consider other propagation effects over the transmitted signal caused by the space channel and exploit further resources of this practical design flow.

Acknowledgment

We wish to thank Instituto Nacional de Pesquisas Espaciais (INPE) for the laboratory infrastructure made available.

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