Impact of MOSFET's structure parameters on its overall performance depending to the mode operation

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Abstract - The goal of this paper is to determine the influence of the main electrical and physical parameters that characterize MOSFET (the NMOS transistor), which control the device behaviour that depends on the selected parameter values. Furthermore, the paper provides directives that need to be followed during the design phase of MOSFET, which shall enable the desirable performance of the device depending on operation conditions, by controlling the fabrication process technology. Designing the MOSFET with appropriate parameters enables the design of integrated digital circuits with the best possible performance, depending on the selected MOSFET logic and the operation conditions.

Keywords - body-effect, channel length modulation coefficient, channel resistance, doping concentration, Fermi potential, gate oxide thickness, MOSFET, overdrive voltage, process transconductance parameter, threshold voltage.

I. Introduction

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is the fundamental building block of digital integrated circuits based on MOS transistors. Based on the structure, the technological advantages, as well the relative simplicity of MOSFET operation, have make the MOSFET the most widely used switching device in the designing of digital integrated circuits [1]-[6]. The MOSFET occupies a relativity smaller silicon area and has lower dissipation power compared to bipolar junction transistor. All of these properties have made it possible to pack large number of MOSFETs on a single integrated circuit, resulting in the highest density packing of the digital integrated circuits. The enhancement-type MOSFET is the most widely used field-effect transistor in the designing of the CMOS logic circuits. The MOSFETs are characterized by several electrical and physical parameters, which have significant effects on the MOSFET operation as in static and dynamic (transient) mode of operation. If the MOSFET parameters are controlled during the fabrication process of the MOSFET device, then the device behaviour can be controlled depending by operation conditions. The designing of the MOSFET digital integrated circuits (CMOS digital integrated circuits) with controlled MOSFET parameters will result on higher overall performance of the digital circuits or systems.

II. The Role of Physics and Electrical Parameters of the MOSFET on its Electrical Behaviour

The MOSFET is characterized with several of the physical and electrical parameters which determine the electrical behaviour of MOSFET device. These parameters are named the MOSFET parameters and will have impact on MOSFET operation and to its parasitic effects depending of the MOSFET dimensions [7]-[9]. For exploring the MOSFET characteristic parameters, will explore the n-channel enhancement-type MOSFET (or shortly NMOS transistor). In Fig.1 is shown the physical structure of the n-channel enhancement-type MOSFET under external bias voltages.

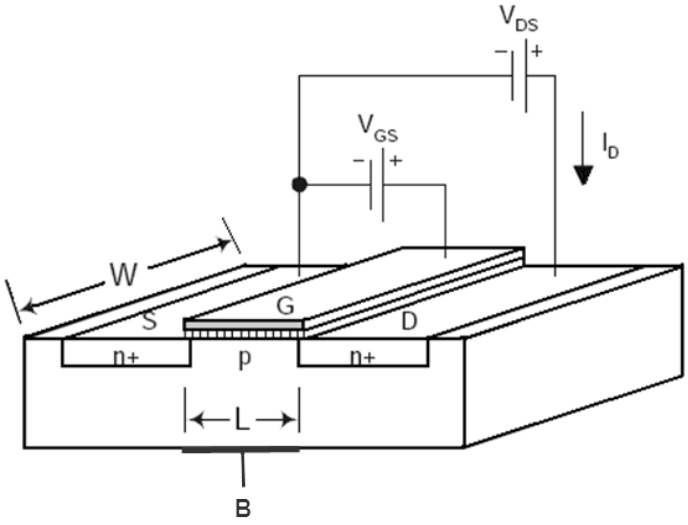

Fig.1 The structure of the n-channel enhancement-type MOSFET under external bias voltage.

The Fermi potential is a MOSFET electrical parameter, and for p-type substrate can be approximated by expression:

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A} \tag{1}$$

ϕ_{Fp} – the Fermi potential for p-type substrate,
q – the electron charge,
N_A – the doping concentration,

k– the Boltzmann's constant,
n_i – intrinsic carrier concentration of silicon (S_i).

For small positive gate-to-source bias V_{GS} (when source-to-substrate V_{SB}= 0V, i.e. source and substrate terminals are connected together or to ground), thus a depletion region is created near the surface of semiconductor-oxide interface (channel region). The thickness (the depth) of this depletion region on the surface near semiconductor-oxide interface and the depletion region charge density (the fixed acceptor ions) can be expressed:

$$x_d = \sqrt{\frac{2\varepsilon_{Si}\left|\phi_S - \phi_{F_P}\right|}{qN_A}} \tag{2}$$

$$Q_B = -q \cdot N_A \cdot x_d = -\sqrt{2q\varepsilon_{si}N_A\left|\phi_S - \phi_F\right|} \tag{3}$$

ϕ_S – the surface potential,

ε_{Si} – the dielectric constant of silicon (S_i)

For the certain positive voltage gate-to-source electrode V_{GS}, an n-type region is created near surface of the semiconductor-oxide interface and this created region is called the inversion layer. This condition requires that the surface potential to be equal by magnitude (but the reverse polarity), as the bulk Fermi potential. Thus, the maximum depletion region depth near semiconductor-oxide interface and the maximum depletion region charge density can be expressed (the depth of depletion region and the depletion region charge achieved at the onset of surface inversion remain constant for higher values of gate-to-source voltage V_{GS}):

$$x_{dm} = \sqrt{\frac{2\varepsilon_{Si}\left|2\phi_F\right|}{qN_A}} \tag{4}$$

$$Q_B = -q \cdot N_A \cdot x_d = -\sqrt{2q\varepsilon_{si}N_A\left|-2\phi_F\right|} \tag{5}$$

The MOSFET threshold voltage is an electrical parameter, which depends from physical parameters of MOSFET structure (when V_{SB} = 0V) and can be calculated by expression [10], [11]:

$$V_{t0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \pm \frac{qN_I}{C_{ox}} \tag{6}$$

Whereas, if the substrate (body) is biased by different voltage level to the source (V_{SB} > 0V), the device threshold voltage is expressed as follows:

$$V_t = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \pm \frac{qN_I}{C_{ox}} \tag{7}$$

or in general expression as:

$$V_t = V_{t0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right) \tag{8}$$

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}} \tag{9}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{10}$$

where:
Φ_{GC} - the work function difference between the gate and the channel,
t_{ox} – the gate oxide thickness (SiO_2),
γ – the body-effect coefficient
ε_{ox} – the dielectric constant of oxide,
Q_{ox} – the fixed charges density in the gate oxide and in silicon-oxide interface,
C_{ox} – the oxide capacitance per unit gate area,
Q_I – density of implanted impurities into channel region.

The excess of gate-to-source bias V_{GS} over the MOSFET threshold voltage V_t is called the effective voltage (or the overdrive voltage).

$$V_{OV} = V_{GS} - V_t \tag{11}$$

The magnitude of the electron charge in the channel depends by the overdrive voltage and dimensions of channel region and can be expressed as:

$$\left|Q_I\right| = C_{OX}V_{OV}(WL) \tag{12}$$

V_{OV} – the MOSFET overdrive voltage,
W – the MOSFET channel width,
L – the MOSFET channel length.

The value of drain current when between drain-to-source is applied a small voltage V_{DS} (the MOSFET device operate in linear region or linear mode) can be expressed as:

$$I_D = (\mu_n C_{0x})\left(\frac{W}{L}\right)V_{OV}V_{DS} \tag{13}$$

when:
μ_n – the mobility of the electrons at the surface of the channel.

In the MOSFET device, very important parameters, fabrication-process dependent, are [12]:

$$k_n^{'} = \mu_n C_{ox} \tag{14}$$

$$k_n = k_n^{'}\frac{W}{L} \tag{15}$$

$k_n^{'}$ – the process transconductance parameter, or process-dependent constant,
k_n – the MOSFET transconductance parameter.

By increasing the drain-to-source voltage V_{DS} the channel depth is no longer uniform (as result of increasing the voltage V_{DS}) and the MOSFET channel will take the tapered shape, with the deepest at the source and with shallowest at the drain end. Now, the MOSFET channel resistance will increase, as well the drain current can be expressed as follows:

$$I_D = (\mu_n C_{0x})\left(\frac{W}{L}\right)(V_{OV} - \frac{1}{2}V_{DS})V_{DS} \quad (16)$$

or in alternative expression:

$$I_D = (\mu_n C_{0x})\left(\frac{W}{L}\right)(V_{GS} - V_t - \frac{1}{2}V_{DS})V_{DS} \quad (17)$$

When the drain-to-source voltage V_{DS} excess the overdrive voltage V_{OV} (or the gate-to-drain voltage V_{GD} is smaller or equal to MOSFET threshold voltage V_t) the MOSFET channel depth at the drain reduces to zero (pinch-off), and MOSFET device will operate in saturation mode. For idealized case, the drain current can be expressed by expression:

$$I_{DS} = \frac{1}{2}(\mu_n C_{0x})\left(\frac{W}{L}\right)V_{OV}^2 \quad (18)$$

But, in reality, increasing drain-to-source voltage V_{DS} beyond the overdrive voltage V_{OV} the channel pinch-off point is moved slightly away from the drain toward the source (an even larger portion of the channel becomes pinched-off). Consequently, the MOSFET effective channel length is reduced from L to L-ΔL, and this phenomenon is called as 'channel-length modulation'. Now, approximately the channel length shortening ΔL is proportional to the square root of (V_{DS} - V_{OV}), and this effect can be accounted in saturation drain current expression as:

$$I_{DS} = \frac{1}{2}(\mu_n C_{0x})\left(\frac{W}{L}\right)V_{OV}^2(1 + \lambda V_{DS}) \quad (19)$$

or in alternative expression:

$$I_{DS} = \frac{1}{2}(\mu_n C_{0x})\left(\frac{W}{L}\right)(V_{GS} - V_t)^2(1 + \lambda V_{DS}) \quad (20)$$

Here λ is an empirical MOSFFET parameter (electrical model parameter), which is called the channel length modulation coefficient, and its value depends on the process technology used to fabricate as well as on the channel length of the MOSFET device [13]. Because the newer technologies have very short channel, and the channel modulation constant of MOSFET will have more impact on the MOSFET operation characteristics compared to the older technologies. The value of the channel length modulation coefficient λ is inversely proportional to the MOSFET channel length L.

III. Results and Discussion

The dependence of the Fermi potential ϕ_{Fp} on the doping concentration N_A in p-type substrate is shown in Fig. 2. The achieved results indicate that for higher values of the doping concentration N_A, the Fermi potential will be more negative, i.e. the Fermi level in p-type semiconductor will have more negative value.

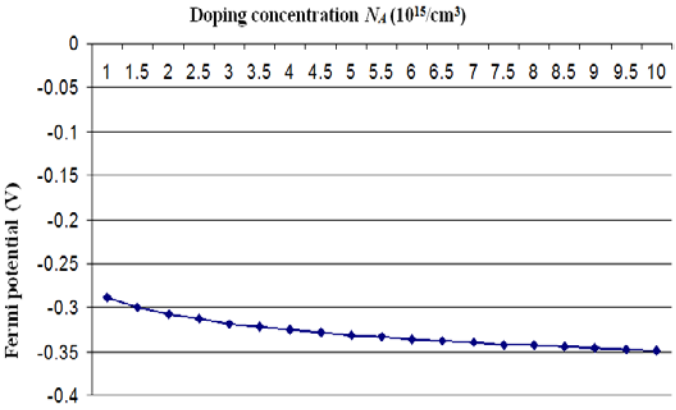

Fig. 2 Variation of the Fermi potential ϕ_{Fp} on the doping concentration N_A.

The influence of the doping concentration level N_A on the maximum depletion region depth at the onset of surface inversion is shown in Fig. 3, and for higher level of the doping concentration N_A the maximum depletion region depth x_{dm} will be shallower, i. e. the maximum depletion region depth near oxide-substrate interface will be smaller.

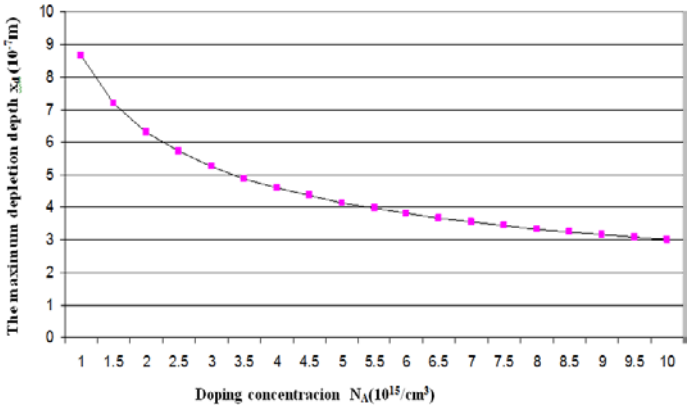

Fig. 3 Variation of the maximum depletion region depth x_{dm} as a function of the doping concentration N_A in p-type semiconductor (substrate).

The dependence of the depletion region charge density (which is due to the fixed acceptor ions located in depletion region) for surface inversion conditions related to doping concentration N_A into p-type substrate, is shown in Fig. 4. From results presented, we note that the depletion region charge density Q_B will be higher for higher values of the doping concentration N_A, but polarity of this charge is negative, as a result of solely fixed acceptors ions in this region.

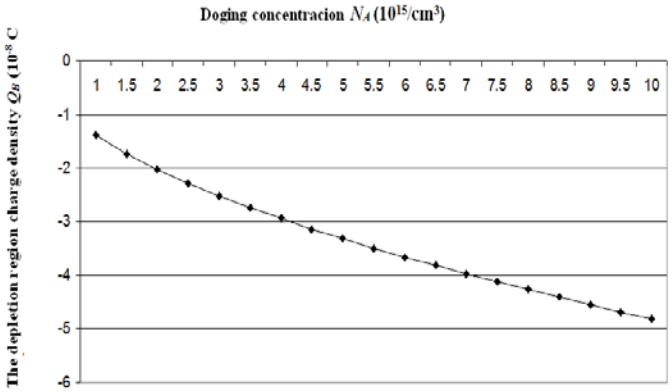

Fig. 4 Variation of the depletion region charge density Q_B at surface inversion as a function of the doping concentration in p-type semiconductor (substrate) N_A.

In linear mode of the MOSFET operations the device behaves as a linear resistance, because channel resistance r_{DS} value is controlled by overdrive voltage V_{OV}. The dependence of the MOSFET channel resistance on overdrive voltage is presented in Fig. 5. Based on achieved results, it could be concluded that for higher value of the MOSFET overdrive voltage, the channel resistance of device will be lower, but with a significant impact for lower values of the overdrive voltage.

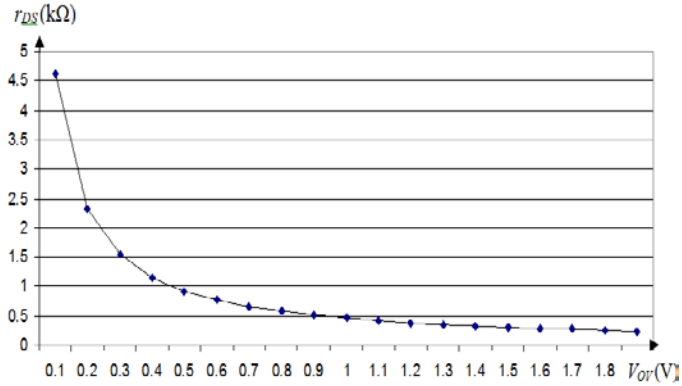

Fig. 5 The dependence of MOSFET channel resistance as a function of the MOSFET overdrive voltage, when device operate in linear mode and the MOSFET transconductance parameter is $k_n = 338.29$ μA/V^2.

The channel width W of the MOSFET device is the most significant parameter which can be controlled during design phase, besides the channel length L of the MOSFET device which is fixed parameter determined by process technology (the lithography process) used to fabricate it. The impact of the channel width W of MOSFET on the device channel resistance (NMOS device) is indicated in Fig. 6. Form achieved results, the channel resistance of the MOSFET will be smaller for higher values of device channel width W. But, the parasitic capacitance of the MOSFET device depends by its dimensions [14]-[17].

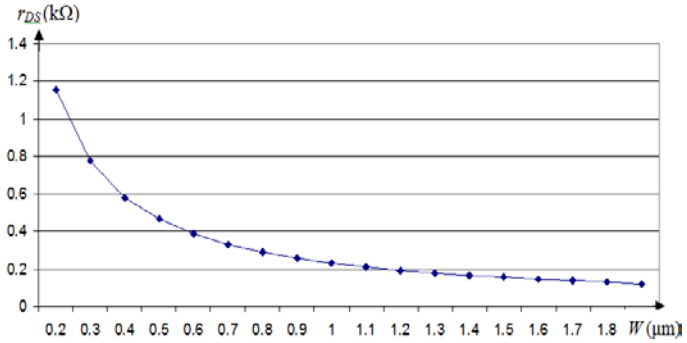

Fig. 6 The dependence of the MOSFET channel resistance r_{DS} as a function of device channel width W, when $V_{OV} = 2$V, $L = 0.18$ μm, $k_n^{'} = 338.29$ μA/V^2 and in linear mode operation.

The Fig. 7 and Fig. 8 indicate the influence of gate oxide thickness t_{ox} (device physical parameter) of the MOSFET on channel resistance r_{DS} and on process transconductance parameter $k_n^{'}$ that characterize the MOSFET device. For larger value of the gate oxide thickness t_{ox}, the channel resistance r_{DS} will increase, but the value of process transconductance parameter will decrease. The gate oxide thickness is a significant parameter of the MOSFET device which has to control during design phase depending on conditions and role of MOSFET device in different applications.

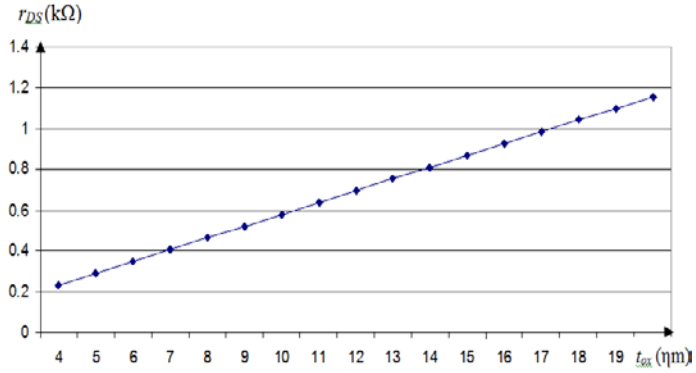

Fig. 7 The dependence of MOSFET channel resistance r_{DS} as e function of the gate oxide thickness t_{ox}, when $V_{OV} = 2$V, $L = 0.18$μm, $W = 1$μm, $\mu_n = 450$ cm^2/Vs and $V_t = 0.7$V.

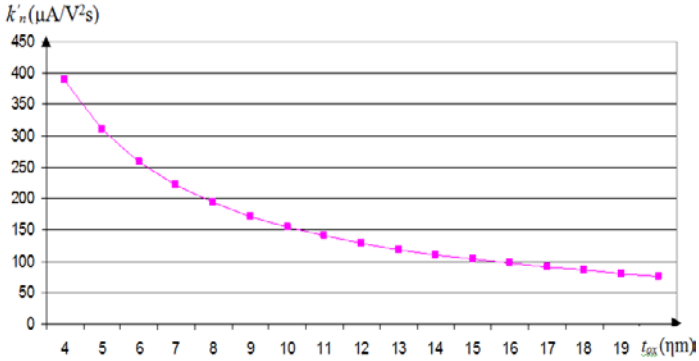

Fig. 8 The dependence of process transconductance parameter $k_n^{'}$ as a function of the gate oxide thickness t_{ox}, when $V_{OV} = 2$V, $L = 0.18$μm, $W = 1$μm, $\mu_n = 450$ cm^2/Vs and $V_t = 0.7$V.

In Fig. 9 is shown the current-voltage characteristic of MOSFET when it operates in linear mode and the drain-to-source voltage is kept small, by set of graphs when the overdrive V_{OV} voltage is used as parameter. For higher value of overdrive voltage the slope of the current-voltage characteristic will be higher, and the channel resistance will be smaller, whereas the drain current will increase. In this operation region the MOSFET device behaves as a voltage-controlled resistance.

The MOSFET current-voltage characteristic when the drain-to-source voltage is increasing but don't excess the overdrive voltage, is indicted in Fig.10. The described relationship by set of graphs show that the dependence of the current-voltage characteristic will decrease compared to lower value of drain-to-source voltage (the current-voltage characteristic will take the parabolic shape), with significant impact when the drain-to-source voltage is closer to the overdrive voltage.

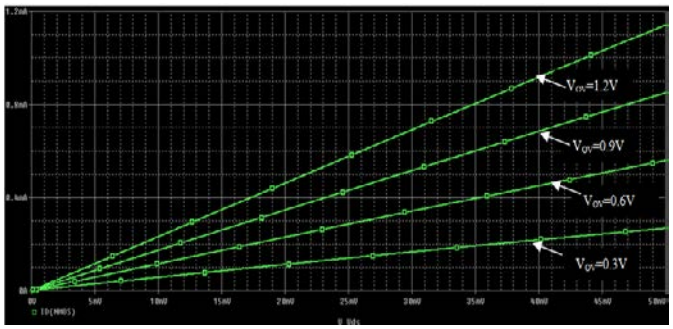

Fig. 9 The current-voltage characteristic of the MOSFET when the drain-to-source voltage V_{DS} is kept small.

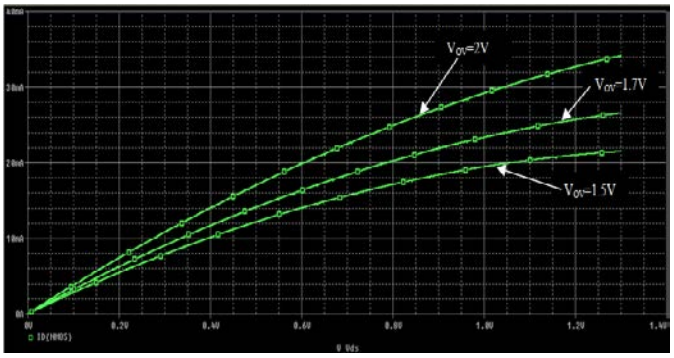

Fig. 10 The MOSFET current-voltage characteristic when MOSFET device operate in linear mode for some parametric values of the overdrive voltage V_{OV} and for higher values of V_{DS}.

Therefore, when during MOSFET operation which operates in linear mode is selected the larger value of the overdrive voltage, the slope of the MOSFET current-voltage characteristic will increase, and results on larger values of drain current for selected drain-to-source voltage. But, the MOSFET current-voltage characteristic will change the relationship to the drain-to-source voltage when this value is increasing and it reaches the overdrive voltage, compared to smaller values of the drain-to-source voltage.

The MOSFET current-voltage characteristic when the drain-to-source voltage is increased and it excesses the overdrive voltage (the MOSFET operates in saturation mode) for several different parametric values of overdrive voltage is shown in Fig. 11. From this characteristic, it could be indicated that when the drain-to-source voltage excesses the overdrive voltage the drain current is controlled only by overdrive voltage.

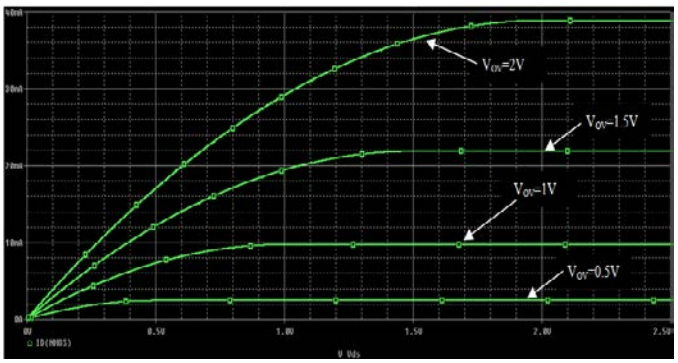

Fig. 11 The MOSFET current-voltage characteristic for several different overdrive voltage V_{OV}, when MOSFET device operate in linear and saturation mode.

The behaves of the MOSFET current-voltage characteristic when the channel length effect is included and when the device operate in saturation mode, and the overdrive voltage has four different values are indicated in Fig.12. From the set of graphs when the MOSFET device operates in saturation mode, it could be indicated that current-voltage characteristic in this region will have e slightly slope with significant impact for higher value of overdrive voltage, as result of drain-to-source voltage V_{DS}.

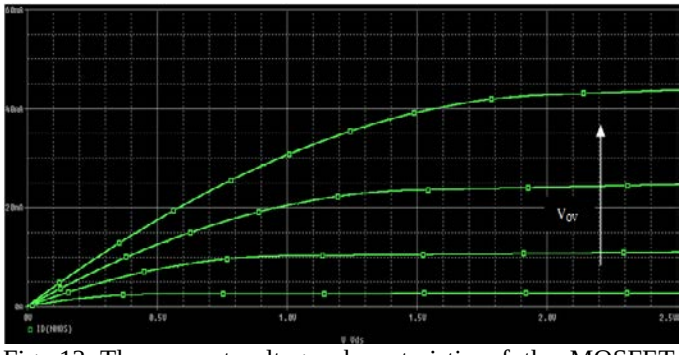

Fig. 12 The current-voltage characteristic of the MOSFET device when the channel length modulation coefficient has value $\lambda = 0.05V^{-1}$, for several different values of overdrive voltage V_{OV}.

When the MOSFET device operates in saturation mode the device channel resistance has a finite values which depends on the channel length modulation coefficient and the overdrive voltage. The influence of channel length modulation coefficient on MOSFET channel resistance is indicated in Fig.13, and device channel resistance r_{DS} will be larger when the modulation coefficient λ will be smaller.

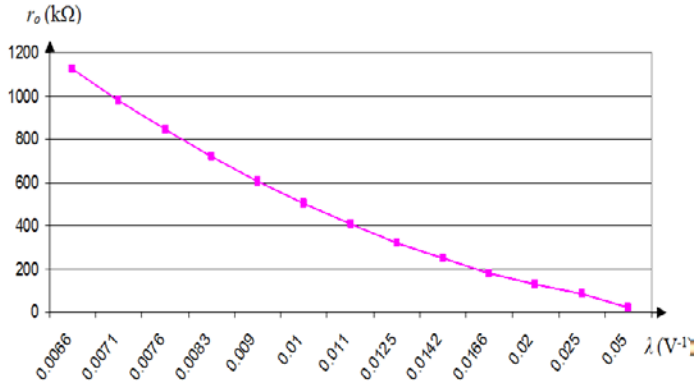

Fig. 13 The variation of the MOSFET channel resistance on channel length modulation coefficient λ, when the MOSFET device operates on saturation mode.

The impact of channel length modulation coefficient λ, the threshold voltage V_{t0} and the gate oxide thickness t_{ox} on MOSFET current-voltage characteristic are shown in Fig. 14, Fig. 15 and Fig. 16. Based from the set of graphs, for larger values of channel length modulation coefficient, the slope of the current-voltage characteristic will has slightly increase, likewise dependence will has for smaller values of the MOSFET threshold voltage and for smaller value of the gate-oxide thickness.

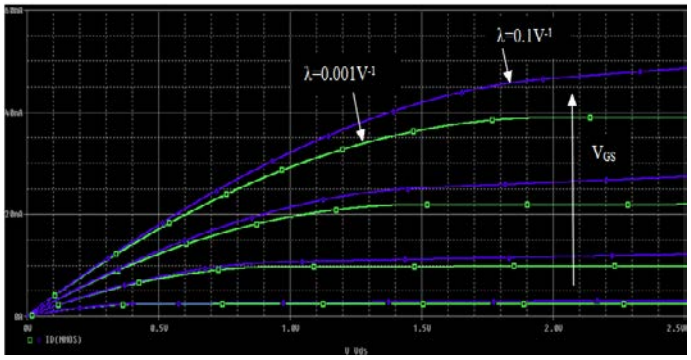

Fig. 14 The dependence of the MOSFET current-voltage characteristic for different values of the channel length modulation coefficient λ.

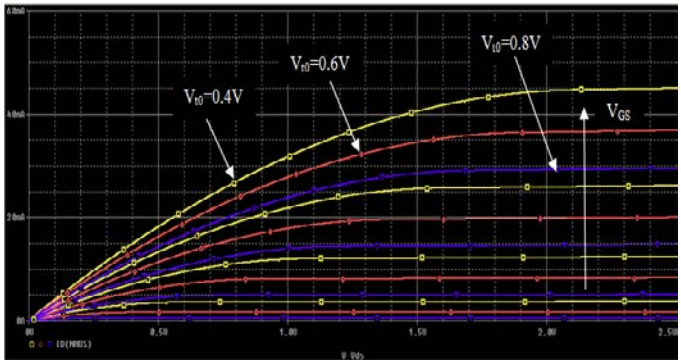

Fig. 15 The dependence of the MOSFET current-voltage characteristic for three different values of the MOSFET threshold voltage V_{t0}.

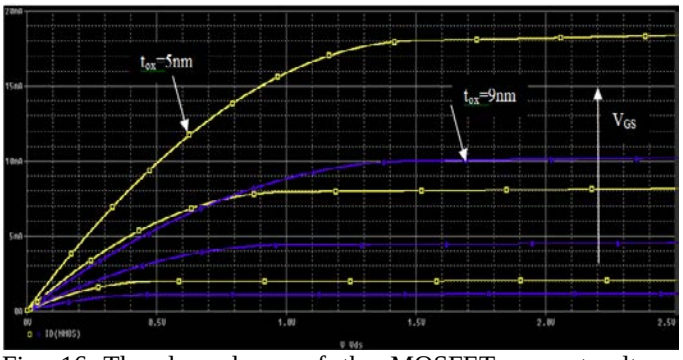

Fig. 16 The dependence of the MOSFET current-voltage characteristic on two different values of the gate oxide thickness t_{ox}.

The influence of the body effect reflected by V_{SB} (substrate effect) and the MOSFET aspect ratio (W/L) on its current-voltage characteristic are shown in Fig. 17 and Fig. 18. For smaller value of the source-to-substrate voltage V_{SB} and larger values of the MOSFET aspect ratio W/L, the drain current will be larger.

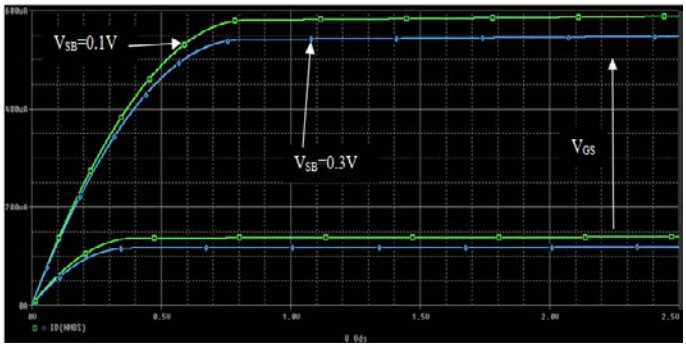

Fig. 17 The dependence of the MOSFET current-voltage characteristic for two different values of the source-to-substrate voltage V_{SB}.

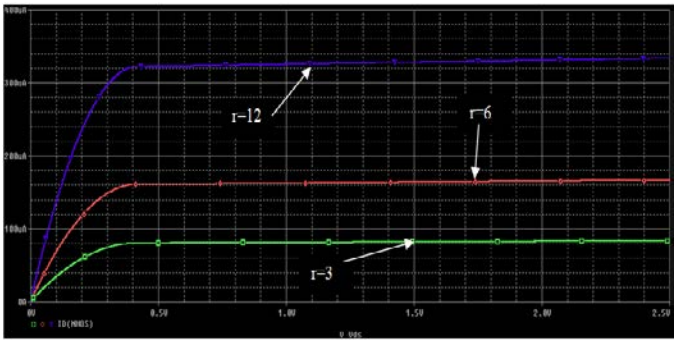

Fig. 18 The dependence of the MOSFET current-voltage characteristic for three different values of the MOSFET aspect ratio $r=W/L$.

When during design phase of MOSFET is selected the larger value of device aspect ratio ($r = W/L$), the MOSFET current-voltage characteristic will shift to larger values of drain current compared to smaller values of the device aspect ratio for same condition of source-to-drain bias.

IV. Conclusion

If during the design phase of the MOSFET device, the electrical and physical parameters which characterize the MOSFET device as: the substrate doping concentration (N_A), the threshold voltage (V_t), the body body-effect coefficient (γ), the process transconductance parameter (k'_n), the channel width (W), the channel length (L), the gate-oxide thickness (t_{ox}) and the channel length modulation coefficient (λ) are controlled and implemented by the selected technology process, the MOSFET device can be designed by requested performance by the device designer, depending to the operation conditions.

For larger values of doping concentration in p-type substrate (N_A), the Fermi potential ϕ_{Fp} and the depletion region charge density (Q_B) will be larger by absolute value, but the maximum depletion region depth (x_{dm}) will be lower (or shallower).

The MOSFET channel resistance (r_{DS}) in the induced inversion layer will be smaller for larger value of the overdrive voltage (V_{OV}), but with significant impact when in device is applied smaller value of the overdrive voltage (V_{OV}). Also, the device channel resistance (r_{DS}) will be smaller if during designed phase is selected the larger values of the MOSFET channel length (W).

When the gate oxide thickness (t_{ox}) of MOSFET device is selected to be smaller, the induced channel resistance (r_{DS}) will be larger, but the value of the process transconductance parameter (k'_n) will be larger.

For larger value of the channel length modulation coefficient (λ) when the MOSFET device operates in saturation mode, the slope of the MOSFET current-voltage characteristic will has a slightly increase which is directly proportional to the channel length modulation coefficient, which reflects in an increase of the drain current. But, the MOSFET channel resistance r_{DS} when the device operates in saturation mode will be smaller if the channel length modulation coefficient has larger value.

When the threshold voltage (V_{t0}) and the gate oxide thickness (t_{ox}) of the MOSFET are smaller, the current-voltage characteristic will shift to larger values of drain current, as result of increasing of the characteristic slope compared to larger values, for same drain-to-source voltage. Whereas, when the source-to-substrate (V_{SB}) voltage have larger value and device aspect ratio (r) has lower, the MOSFET current-voltage characteristic will shift to smaller values of drain current.

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