Modeling of Input Capacitance of IGBTs under Dynamic Conditions

Ji Tan, Yangjun Zhu, Shuojin Lu, Qiaoqun Yu

***Abstract*—**Insulated gate bipolar transistor (IGBT) input capacitance has significant influence on device dynamic behaviors, and consists of two nonlinear components: the gate capacitance and the miller capacitance. Although these two components are capacitance with MOS structure, they behave differently with the isolated MOS capacitance. The reasons leading to this are the influences of the nearby semiconductor layers and the collector current dependency. An analytical model of the input capacitance for the dynamic cases has been derived, and the collector current dependency is quantified. The predictions of the model are in good agreement with the results obtained from numerical simulation of IGBT transient.

***Keywords*—**Insulated gate bipolar transistor (IGBT), input capacitance, analytical model, semiconductor devices.

I. INTRODUCTION

IGBT(Insulated gate bipolar transistor), well known for the low conduction loss and easy gate control, is an important device in industrial and traction applications[1] [2]. Due to the complex device structure, IGBT has some parasitic capacitances. These capacitances have great effects on the behaviors of IGBT during switching period. The input capacitance of IGBT consists of two nonlinear components. They are commonly called the gate capacitance (C_{ge}) and the miller capacitance (C_{gc}).

To explicitly understand the characteristics and properties of IGBT, accurate model of the input capacitance should be set up. Conventional models [3]-[6] of C_{ge} and C_{gc} mainly focus on the operating-point-dependent characteristics. Baliga regards the input capacitance as MOS (Metal-Oxide-Semiconductor) type capacitance and focuses on the voltage dependency [3]. Rael presents more detailed analyses on the voltage dependency of IGBT input capacitance and thinks that interelectrode MOS capacitances of IGBTs are fundamentally of three-port coupling origin [4]. This model is accurate even under negative gate polarization, but the influence of the collector current is out of consideration. These models can be physically correct under quasistatic conditions. However, the C_{gc} behaves quite differently under dynamic cases. This is because the drift N region under the gate is full of carriers and can not be simply treated as "depletion layer". Yuan Teng gives an explanation of negative miller capacitance during the switching transients of IGBTs and analyzes the electric charge effects [7]. The current dependency of the input capacitance is mentioned in [8] and [9]. Palmer presents the simulation of IGBT capacitance under zero current and rated current, respectively [9]. The results show that the input capacitances increase at high currents, but the quantitative analysis of this current dependency is not mentioned. In this paper, a model of input capacitance for the dynamic cases is derived and a factor is used to describe the current dependency. The predictions of the model are in good agreement with the results obtained from numerical simulations.

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Ji Tan is with the University of Chinese Academy of Sciences. Ji Tan, Yangjun Zhu, Shuojin Lu, and Qiaoqun Yu are with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China Corresponding author: Yangjun Zhu (e-mail: zhuyangjun@ime.ac.cn).

II. DEVICE STRUCTURE AND INPUT CAPACITANCE MODEL

A. Basic MOS capacitance

Fig.1 shows the C-V characteristics for a MOS structure of P substrate. The C_0 in Fig.1 is the oxide layer capacitance of this MOS structure with the value related to the oxide thickness. When a negative or positive bias is applied to the metal electrode of the MOS structure, the carrier density in the semiconductor layer will change. Thus, the capacitance of the MOS structure changes with the outer voltage:

1) When a relatively high negative bias is applied to the metal electrode, mobile holes are attracted from the bulk toward the oxide-semiconductor interface and form an accumulation layer. As majority carriers in the P-substrate region, the holes can respond to an AC signal superposed on the negative DC voltage applied to the metal electrode. Consequently, the capacitance for the MOS structure becomes equal to that of the oxide layer capacitance under accumulation conditions.
2) As the negative voltage bias decrease to a lower value or even to zero, less mobile holes are attracted to the oxide-semiconductor interface. Thus, the capacitance for the MOS structure should be looked as an oxide layer capacitance in series with a semiconductor layer capacitance. So the value of the MOS capacitance slightly decreases compare to that in 1).
3) When a positive bias is applied to the metal electrode, a depletion layer forms near the oxide-semiconductor interface in the semiconductor region. The application of an AC signal superposed on the positive DC voltage applied to the metal electrode produces a response only from the P-substrate region located at the edge of the depletion layer because there are no mobile charges

within the depletion layer. The capacitance for the MOS structure should still be looked as an oxide layer capacitance in series with a semiconductor layer capacitance. As the width of the depletion layer increases, the semiconductor layer capacitance decreases. Consequently, the whole MOS capacitance reduces.

4) As the positive bias applied to the metal electrode continue to increase, eventually an inversion layer forms at the oxide-semiconductor interface. When in the weak inversion condition, the MOS capacitance behaves like the depletion condition and decreases as the outer voltage bias increases. However, when the strong inversion layer forms, any further increase in the DC voltage applied to the metal electrode is supported across the oxide layer. Thus, the thickness of the depletion layer reaches a maximum value. As the existence of the massive electrons, the capacitance for the MOS structure becomes equal to that of the oxide layer capacitance under accumulation conditions, just like the case in 1).

5) The above analysis is under the low frequency AC signal condition. The formation of the inversion layer takes about 10^0 to 10^2 seconds, so the generation and recombination in the inversion can not response to the high frequency AC signal. In this case, the capacitance for the MOS structure becomes equal to that of the series combination of the oxide layer capacitance and the semiconductor layer capacitance. As the thickness of the depletion layer reaching a maximum value, the MOS capacitance stays a minimum value.

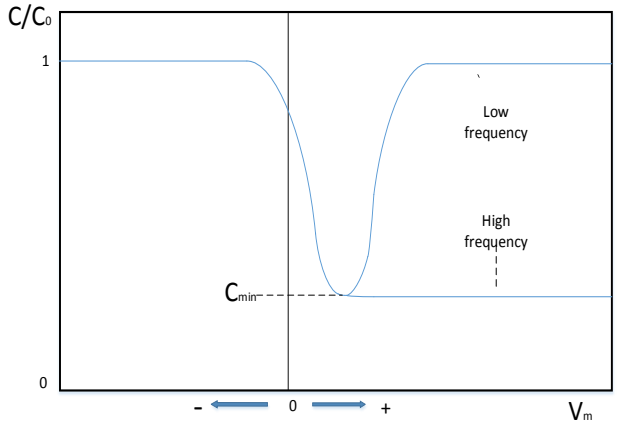

Fig.1. C-V characteristics for MOS with P substrate

Fig.2 shows the cross-section of a typical trench-FS-IGBT cell. The IGBT structure is formed by four (N-P-N-P) alternating layers. The thickness of the whole IGBT and the FS layer is 125um and 10um respectively. The parasitic input capacitances are defined in Fig.1. The capacitance between gate and emitter, C_{ge}, consists of three parts: the gate-P^+ overlapped component C_{p+}, the gate-N^+ overlapped component C_{n+}, and the gate-metal overlapped component C_{sm}. The capacitance between gate and collector, C_{gc}, is also called the miller capacitance.

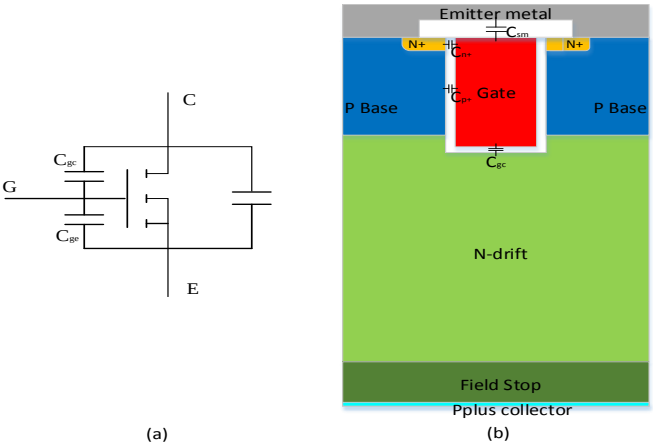

Fig. 2. (a) Input capacitive model for IGBT. (b) Cross-section of IGBT

B. *Characterization of* C_{ge}

For a MOS structure, the C-V characteristics are different under different frequency conditions. For the low frequency conditions, the inversion layer can be formed and MOS capacitance can be treated as a single oxide layer capacitance. However, the electron in the inversion layer can not be created instantaneously under high frequency conditions, so the MOS capacitance is seen as an oxide layer capacitance in series with a depletion layer capacitance.

Normally, the C_{n+} and C_{sm} are negligible compared to the C_{p+}. The C_{p+} is of the MOS type, with a P substrate. This P substrate is heavily doped and short-circuited to the N^+ region by emitter metal. Thus, the inversion layer can be formed in a quite short time [4], and the C_{p+} can be treated as a single oxide layer capacitance even under high frequency conditions.

The C_{ge} can be calculated by the following equation:

$$C_{\mathrm{ge}} = \varepsilon_{si}\varepsilon_0 \frac{A_1}{t_{ox}} \qquad (1)$$

where ε_{si} is the relative dielectric constant of silicon, ε_0 is the vacuum permittivity, A_1 is the overlapped areas between gate and P^+ region, and t_{ox} is the gate oxide thickness. When the bias voltages (V_{ce} and V_{ge}) change, the carrier distribution and the electric field change slightly. However, these changes will not influence the gate capacitance much. Thus, equation (1) can also be used during device switching period.

C. *Characterization of* C_{gc}

The miller capacitance C_{gc} is of the MOS type, with an N substrate. For the quasistatic conditions, we can treat the miller capacitance as an oxide layer capacitance in series with a semiconductor layer capacitance. With the change of the bias voltage, the semiconductor layer capacitance behaves differently, changing from the accumulation regime to the depletion regime.

The depletion layer approximation describes the miller capacitance under deep depletion as:

$$C_{gc} = \frac{C_{ox}C_{si}}{C_{ox}+C_{si}} \qquad (2)$$

$$C_{si} = \varepsilon_{si}\varepsilon_0 \frac{A_2}{W} \quad (3)$$

where C_{ox} is the oxide layer capacitance, C_{si} is the semiconductor layer capacitance, A_2 is the overlapped areas between gate and drift region, and W is the depletion width.

It should be noticed that the drift region (N substrate) under the gate can be full of carriers during switching period. When considering the IGBT turning off with an inductive load (which is the fact in many IGBT applications), the collector current of IGBT stays high until the voltage V_{gc} rise to bus voltage. To sustain the collector current the electron density or the hole density can still stay as 10^{14} cm^{-3} to 10^{15} cm^{-3}, even when the drift region starts to depleted. This carrier density exceeds the doping concentration of the drift region. That means the depletion layer approximation is not suitable for the device switching period, and (3) should be modified.

The effective carrier density in the depletion N_t can be described as [10]:

$$N_t \approx N_B + \frac{I_c}{qAv_{sat}} \quad (4)$$

where N_B is the drift region doping concentration, I_c is the collector current, q is the elementary charge, A is the effective conducting area, and v_{sat} is the carrier saturation velocity.

Under depletion layer approximation, C_{si} is a plate capacitor as (3) and the depletion layer is the dielectric of the plate capacitor. The added carriers make the dielectric different from a common depleted silicon layer. So, we introduce a current dependency factor γ (can be empirical related to the N_t) to modify (3):

$$C_{si} = \varepsilon_{si}\varepsilon_0 \frac{\gamma A_2}{W} \quad (5)$$

The value of the depletion width is needed to calculate the semiconductor layer capacitance correctly. During the switching periods of IGBTs, the depletion width changes with the collector voltage. An approximate equation can be used to calculate the depletion width:

$$W = \sqrt{\frac{\varepsilon_0\varepsilon_{si}V_{ce}}{qN_B}} \quad (6)$$

The effective carrier density can influence depletion width as well. N_t can be substitute for the drift region doping concentration N_B in (6) to for higher accuracy.

During the turn off of IGBT, the high-level injection carriers of the steady state are swept out and the depletion layer expends. The depletion width becomes larger with time goes on. The relation between depletion width and time can be described with following equations:

$$W(t) = \frac{\sqrt{(\alpha p_0)^2 + 4k\beta t} - \alpha p_0}{2k} \quad (7)$$

$$k = \frac{p_0 - \alpha p_0}{2d} \quad (8)$$

$$\beta = \frac{I_c}{2Aq} \quad (9)$$

where α is the a parameter related to the front-side structure of IGBT, p_0 is the carrier concentration at the boundary of the drift N region (the collector side), d is the width of the drift N region.

D. Current dependency factor

Simulations of a series of IGBT structures switching under different current are carried out to build a look-up table between the current dependency factor and the effective carrier density. According to (4), different value of effective carrier density comes from different switching current and different cell structure. The simulation results of the miller capacitance are used to calculate the current dependency factors under different switching conditions, using (5). Fig.3 shows the current dependency factor curve against the effective carrier density.

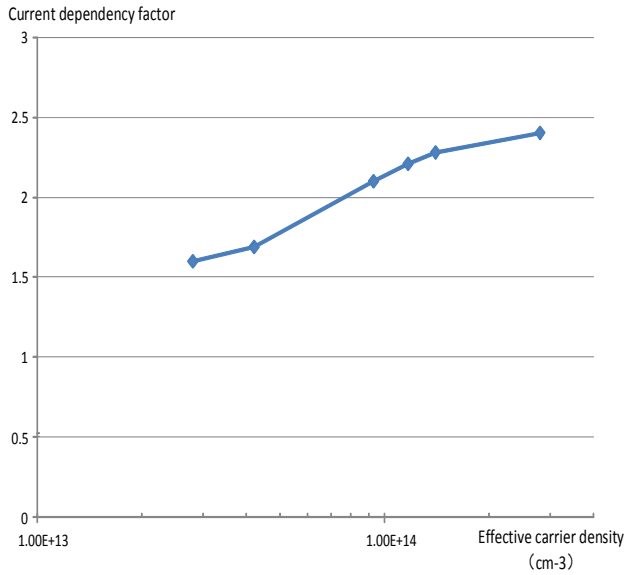

Fig.3. dependency factor curve against the effective carrier density

III. SIMULATION RESULTS

A series of simulation for trench-FS-IGBT have been carried out by Sentaurus TCAD to verify the proposed model. The structure simulated is shown in Fig.1. First, small-signal AC analyses of different bias voltage show the capacitive coupling under quasistatic conditions. Then, the transient simulation has been carried out. We calculate the input capacitance based on the transient waveform during the turn-off period, and compare the results to the proposed model.

A. Small-signal AC analysis

Small-signal analysis computes the Y-matrix when IGBT under specific bias voltage. The Y-matrix describes how the currents in a circuit would react if the applied voltages at different contact nodes change on small scales. The

small-signal frequency is 10^6 Hz in the simulation in this paper.

Fig.4 shows how the gate capacitance changes with V_{ge} when V_{ce}=0V. The results show that the C-V curve of C_{ge} (at a frequency of 10^6 Hz) is similar to the conventional MOS C-V curve under low frequency conditions. This phenomenon is assumed to result from the existence of the electron source, namely the N^+ region. To support this assumption, a simulation for a similar device structure without the N^+ region has been carried out. Results in Fig.4 show that the value of gate capacitance becomes low in inversion regime (when the gate voltage becomes high) in the structure without N^+.

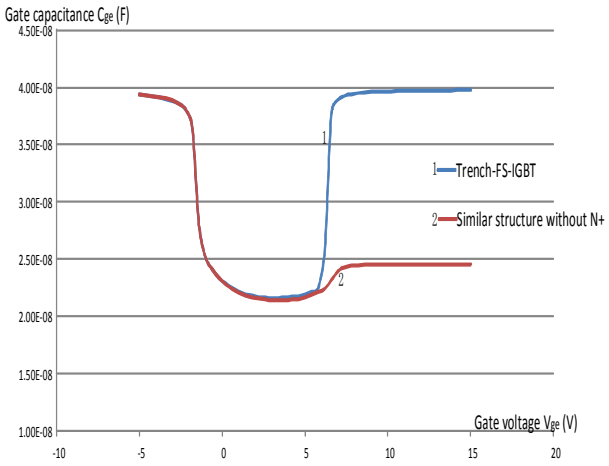

Fig.4. Gate capacitance versus V_{ge} under quasistatic conditions

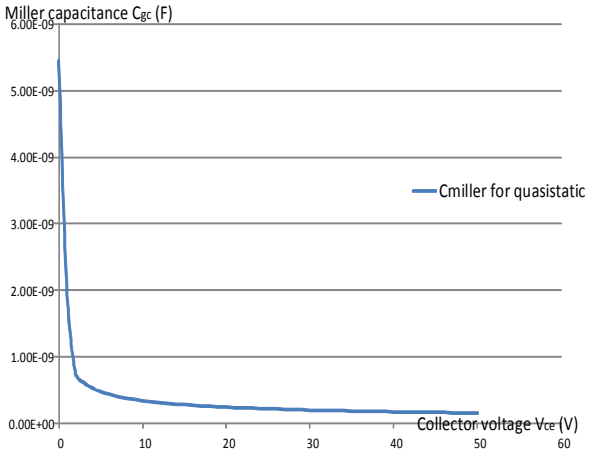

Fig.5. Miller capacitance versus V_{ce} under quasistatic conditions

Fig.5 shows how the miller capacitance changes with V_{ce} when V_{ge}=0V. The results show that the miller capacitance behaves like a MOS capacitance under quasistatic conditions.

B. Transient simulation

The device turn-off simulation under inductive load has been carried out. Fig.6 displays the typical turn-off waveform. Due to the large inductive load, the current of the IGBT will stay high until the voltage rises to the bus voltage during the IGBT turn-off. After that, the current starts to decrease and IGBT goes into the tail-current procedure withstanding high voltage. From t_1 to t_2, gate voltage decreases from V_{gm} to miller platform voltage, while collector voltage and current stay as a constant. The gate driver voltage source starts to discharge the gate capacitance C_{ge} with a RC circuit:

$$I_g(t) = C_{ge}\frac{dV_{ge}}{dt} \tag{10}$$

where I_g is the gate current and t is the time.

Using the C_{ge} from (1) and the dV_{ge}/dt from transient simulation results, we get the curve $I_g(t)$ during t_1 and t_2. Comparing this curve to the $I_g(t)$ curve from transient simulation and plotting them in Fig.7, we can find these two curves agree well.

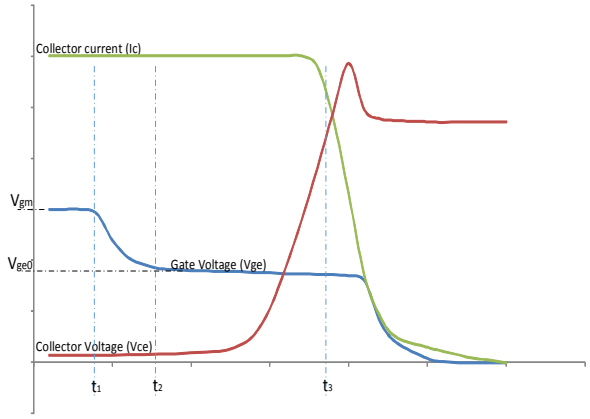

Fig. 6. Typical turn-off waveform of IGBT

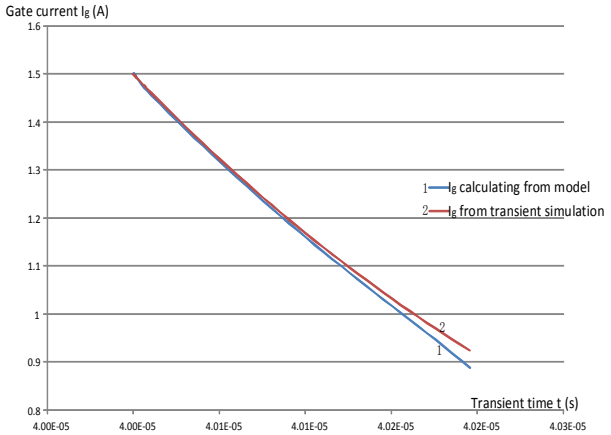

Fig.7. Gate current from t_1 to t_2 in IGBT transient

From t_2 to t_3 in Fig.6, gate voltage stays as a constant and collector voltage starts to increase. The gate driver voltage source starts to charge the miller capacitance C_{gc} with a constant gate current:

$$C_{gc} = \frac{I_{g0}}{dV_{cg}/dt} = \frac{I_{g0}}{dV_{ce}/dt} \tag{11}$$

$$I_{g0} = \frac{V_{ge0}}{R_g} \tag{12}$$

where V_{ge0} is the platform voltage, I_{g0} is the constant gate

current during t_2 and t_3, and R_g is the gate resistance.

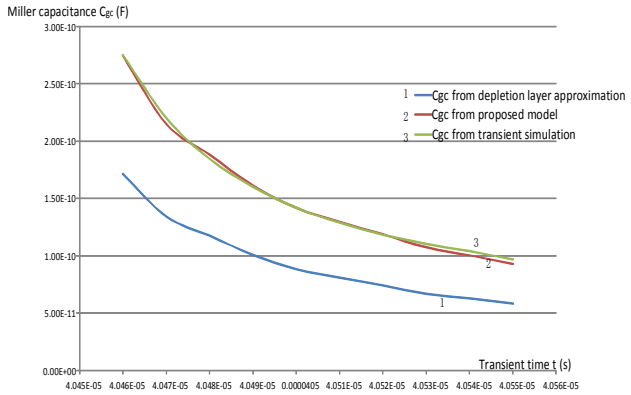

Fig.8. Miller capacitance from t_2 to t_3 in IGBT transient

The miller capacitance can be calculated with (11) and (12), using dV_{ce}/dt and V_{ge0} from the transient simulation results. Comparing this to the C_{gc} from (2), (3), (5) and plotting these curves in Fig.8, we can find that the proposed model agrees better with the simulation results than the depletion layer approximation model.

IV. CONCLUSION

In this paper, an analytical model for the input capacitance of IGBT is proposed. In this model, the gate capacitance is regarded as a constant due to the heavily doped P substrate and the electron source N^+ region. To make the model more precisely, the collector current dependency of the miller capacitance is quantified for the first time. The predictions of the model are in good agreement with the results obtained from numerical simulation of IGBT transient. This analytical model is effective in understanding, evaluating, and designing IGBT devices. The current dependency factor γ in this model is empirical related to the effective carrier density. Further researches can focus on the explicit relation between γ and effective carrier density.

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Ji Tan was born on Jan. 19, 1990**.** He received the bachelor's degree in electronics science and technology from Huazhong University of science and technology. Currently, he is a PHD student at the Institute of Microelectronics, Chinese Academy of Sciences, China. His major research interest is power semiconductor device.