The most significant MOSFET parameters impact in CMOS inverter switching characteristics

Milaim Zabeli, Nebi Caka, Myzafere Limani, Qamil Kabashi*

Abstract - The objective of this paper is to research the impact of electrical and physical parameters that characterize the complementary MOSFETs (NMOS and PMOS transistors) in the dynamic behaviour (time-domain) of the CMOS inverter. In addition to this, the paper also aims at exploring the directives that are to be followed during the design phase of the CMOS inverters that enable designers to design the CMOS inverters with the best possible dynamic performance, depending on operation conditions. The CMOS inverter designed with the best possible dynamic features also enables the designing of the CMOS logic circuits with the best possible dynamic performance, according to the operation conditions and designers' requirements.

Keywords - CMOS-inverter, load capacitance, NMOS transistor, PMOS transistor, propagation delay time, power supply current, threshold voltage, transconductance parameter.

I. Introduction

The CMOS inverter represents fundamental block of the CMOS digital integrated circuits based on CMOS inverter [1]. The switching characteristic (time-domain behaviour) of the CMOS inverter, essentially determine the overall operating speed of CMOS digital circuits. The dynamic (time-domain) performance requirements of CMOS digital systems are usually among the most important specifications that must be taken into consideration during the design phase by circuits' designer [2], [3]. Therefore the dynamic (transient) behaviour of the circuit must be estimated and optimized by designer during the design phase. The CMOS inverter structure consists of a pair of complementary MOSFETs (of an enhancement type NMOS transistor and an enhancement type PMOS transistor, because this type of MOSFET have better performance compared to depletion type of MOSFETs), which operate in complementary mode. The CMOS inverter circuit is shown in Fig. 1 [4]-[6].

Both complementary MOS transistors (MOSFETs) are characterized by electrical and physical parameters, which determine the behaviour of the CMOS inverter in dynamic (switching) and static condition of operation. Several of the main electrical parameters which characterize the complementary MOSFET transistors are: the process transconductance parameter (k'), the zero-bias threshold voltage (V_{t0}), the body-effect parameter (γ), the surface inversion potential ($|2\phi_F|$) and the channel-length parameter (λ). Whereas some of physical parameters of the complementary MOSFET transistors are: the surface mobility (μ), the thin oxide thickness (t_{0x}) and substrate doping (N_b). The values of all these parameters depend on the fabrication process technology. The MOSFET transistors also characterize a considerable number of other parameters, which should be taken into consideration for specific cases of device operation, but their impact in overall performance of the MOSFETs will be less meaningful.

If during fabrication process of MOSFET transistors the their electrical and physical parameters are selected by desired values dictated by technology process, the MOSFET device behaviour can be controlled according designer's needs, depending on their application in digital circuits [7]. By controlling the complementary MOSFET transistor behaviour will be able controlled the CMOS inverter.

The manuscript objective is to investigate the some typical MOSFET transistors parameters that have the most significance impact in dynamic (time-domain) behavior of the CMOS inverter, although the switching characteristics of the CMOS digital circuits and in particular of CMOS inverter circuits, essentially determine the overall operating seed of digital systems in common. Therefore, the switching characteristics of CMOS inverter must be estimated and optimized very early in the design phase. Using analytical and numerical methods supported with the circuit simulator (SPICE) usually provides a very accurate estimate of the CMOS time-domain behavior.

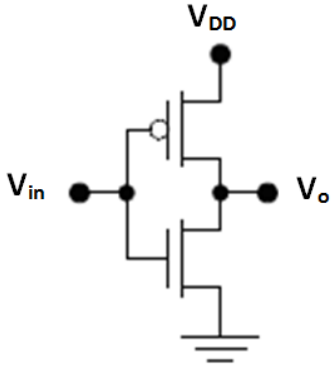

Fig. 1 The structure of the CMOS inverter which contains two complementary MOS enhancement-type transistors.

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II. The Role of the Complementary MOSFET (NMOS and PMOS) Transistors Parameters in Delay Time of the CMOS Inverters

For transient response of the CMOS inverter have to determine the nature and the amount of parasitic capacitances associated with the complementary MOSFET transistors, where their values are determined by layout geometries and the manufacturing processes. The most of these parasitic capacitances are distributed, and for simplification the problem, we first combine into an equivalent lumped linear capacitance.

The speed of the CMOS inverter operation is determined by propagation delay time of the CMOS inverter. To analyse the switching operation of the CMOS inverter to determine its delay time (or propagation delay time), there will be used CMOS inverter with an equivalent lumped linear capacitance, connected between the output node and ground, as in Fig. 2 [8], [9].

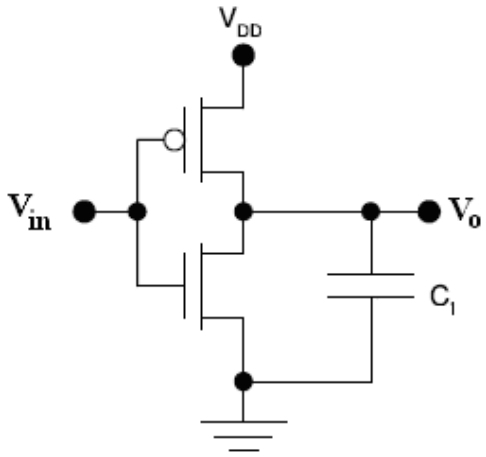

Fig. 2 The CMOS inverter with an equivalent lumped capacitance (equivalent lumped linear capacitance) at the output node

The value of the equivalent lumped capacitance is calculated by using parasitic capacitances of the NMOS and PMOS transistors, the lumped interconnect capacitance and input capacitance of load device (one or more identical CMOS inverter, fan-out parameter) connected at the output of the CMOS inverter, as in Fig. 3. The equivalent lumped capacitance at the output node will be called the load capacitance C_l, and it can be estimate by expression [4], [9], [10]:

$$C_l = 2C_{gd,n} + 2C_{gd,p} + C_{db,n} + C_{db,p} + C_{\text{int}} + nC_g \qquad (1)$$

$C_{gd,n}$ - the gate-drain capacitance of the NMOS
$C_{gd,p}$ - the gate-drain capacitance of the PMOS
$C_{db,n}$ - the drain-body capacitance of the NMOS
$C_{db,p}$ - the drain-body capacitance of the PMOS
C_{int} - the lumped interconnect capacitance
C_g - the input parasitic capacitance of load (the oxide-related capacitances)
n - number of identical stages (the CMOS inverters) connected at the output.

In load capacitance expression are not included some of parasitic capacitances shown in Fig. 3, because have no effect on the dynamic behavior of the CMOS inverter. The factor 2 arises before parasitic capacitances $C_{gd,n}$ and $C_{gd,p}$ as result of the Miller effect, which will have impact in CMOS inverter dynamic performance, or in time delays. This effect can minimized if during design phase of the CMOS inverter, the parasitic capacitances C_{db} of the complementary MOSFETs are minimized.

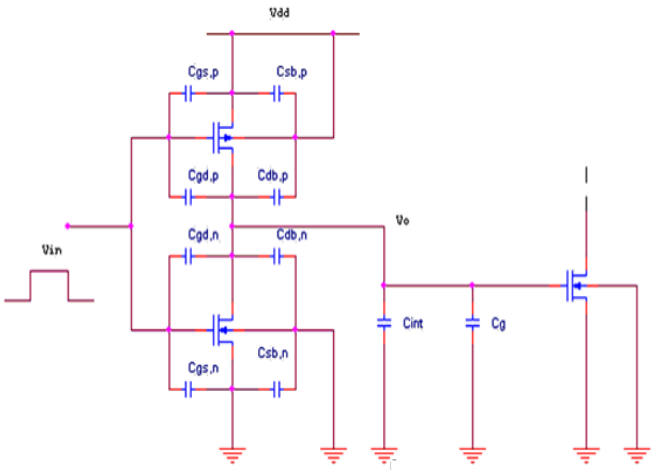

Fig. 3 The CMOS inverter associated with its parasitic capacitances, the lumped interconnect capacitance and load capacitance for analyzing the propagation delay.

In Fig. 4 is shown the CMOS inverter circuits with the equivalent load capacitance for analyzing the propagation delay time, when the problem of analyzing time-domain behavior is simplified. Now, the CMOS inverter switching characteristics are reduced to finding the charge-up and charge-down times of the load capacitance through one MOSFET transistor [4].

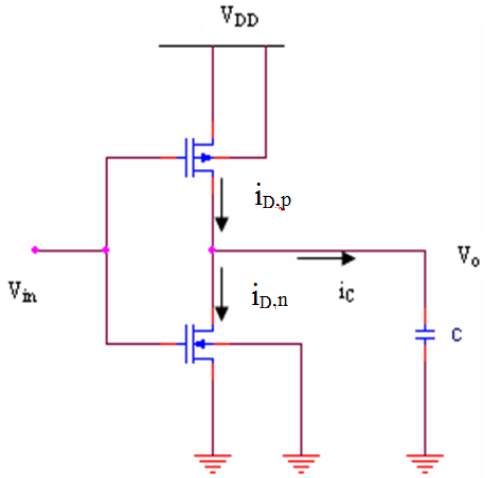

Fig. 4 CMOS inverter with an equivalent lumped (combined) load capacitance

The propagation delay times can be found by using the state equation of the output node in the time domain with acceptable accuracy, as:

$$C\frac{\mathrm{d}V_o}{\mathrm{d}t} = i_C = i_{D,p} - i_{D,n} \quad (2)$$

For calculating the propagation delay time t_{PHL} (propagation delay time of the output voltage during high-to-low transition), when the input voltage switches from low-to-high, the NMOS transistor is turned on and it starts to discharge the equivalent load capacitance, whereas the PMOS transistor is cut off. After calculation depending on mode operation of the NMOS transistor (the NMOS transistor will operates in the saturation region when the $V_o > V_{OH} - V_{t0,n}$, whereas for $V_o \leq V_{OH} - V_{t0,n}$ the NMOS operates in the linear region) of the CMOS inverter, and by combining these two separated intervals can be achieved the expression of the propagation delay [4]:

$$t_{PHL} = \frac{C_l}{k_n(V_{DD} - V_{t0,n})}\left[\frac{2V_{t0,n}}{V_{DD} - V_{t0,n}} + \ln\left(\frac{4(V_{DD} - V_{t0,n})}{V_{DD} + V_{OL}} - 1\right)\right] \quad (3)$$

For calculating the propagation delay time t_{PLH} (propagation delay time of the output voltage during low-to-high transition) when the input voltage switches from high-to-low, the PMOS transistor is turned on and it starts to charge up the equivalent load capacitance, whereas the NMOS transistor is cut off. After calculation depending on mode operation of the PMOS transistor (following a similar derivation procedure, as for calculating the propagation delay time t_{PHL}) of the CMOS inverter can be achieved the expression [4], [8]:

$$t_{PLH} = \frac{C_l}{k_p(V_{DD} - |V_{t0,p}|)}\left[\frac{2|V_{t0,p}|}{V_{DD} - |V_{t0,p}|} + \ln\left(\frac{4(V_{DD} - |V_{t0,p}|)}{V_{DD}} - 1\right)\right] \quad (4)$$

From the expression of the propagation delay time t_{PHL}, it is indicated that the impact on its value will have equivalent load capacitance (C_l), the value of the power-supply voltage (V_{DD}), the value of transconductance parameter of the NMOS transistor (k_n) and the value of the NMOS threshold voltage ($V_{t0,n}$). Whereas from the expression of the propagation delay time t_{PLH}, it is indicated that the impact on its values will have equivalent load capacitance (C_l), the value of the power-supply voltage (V_{DD}), the value of transconductance parameter of the PMOS transistor (k_p) and the value of the PMOS threshold voltage ($V_{t0,p}$). Therefore, the determining parameters of the propagation delay time t_{PHL} are the electrical and physical parameters that characterize only the NMOS transistor, whereas the determining parameters of the propagation delay time t_{PLH} are the electrical and physical parameters that characterize only the PMOS transistor.

For the usual case is assumed that $V_{t0,n} = |V_{t0,p}| = 0.2V_{DD}$, the expressions reduce as in:

$$t_{PHL} = \frac{1.6\ C_l}{k_n V_{DD}} \quad (5)$$

$$t_{PLH} = \frac{1.6\ C_l}{k_p V_{DD}} \quad (6)$$

The inverter propagation delay time (t_P) is defined as the average of propagation delay times:

$$t_P = \frac{1}{2}(t_{PHL} + t_{PLH}) \quad (7)$$

The dynamic power dissipation has two components, the first component is due of current which flows through the series of connection of NMOS and PMOS transistors, and current peaks is at the switching threshold voltage of CMOS inverter (for a symmetric case the threshold voltage of the CMOS inverter is $V_{th} = V_{DD}/2$). However, the second component of dynamic power dissipation is more significant component, results from the current that flows in NMOS and PMOS transistors when the CMOS inverter is loaded by load capacitance. Now if the CMOS inverter is switching by periodic input voltage pluses with negligible rise and fall times, the average dynamic power dissipation in CMOS inverter will be:

$$P_D = fC_l V_{DD}^2 \quad (8)$$

Now, it is clear that the average dynamic power dissipation of the CMOS inverter is proportional to the switching frequency (f). Hence, the low-power advantage of CMOS circuits at the higher switching frequency becomes prominent. Also, the maximal operation frequency of the CMOS inverter is related to the propagation delay. The average switching power dissipation estimate by expression (8) will hold for the CMOS inverter, when the leakage power is neglected.

Under the realistic conditions, when the input voltage pulses (deviates from ideal step pulses) have nonzero rise and fall times, both MOSFET (NMOS and PMOS) transistors will simultaneously conduct (or both transistors temporarily form a conducting path between V_{DD} and the ground, when input voltage is near the threshold voltage of the CMOS inverter) a certain amount of current (the short-circuit current), which gives rise to dynamic power dissipation in the CMOS inverter. For this reason the dynamic power expression (8) it has to add the additional dynamic power dissipation, which is due to the short-circuits current. But, when the load capacitance has higher values, the dynamic power dissipation term which is due to the short-circuit current become negligible in comparison the dynamic power dissipation term which is due the loaded a load capacitance [11], [12].

The inverter propagation delay time can be used to estimate a fundamental parameter for measuring the quality and the performance of the CMOS process. This fundamental parameter is called the delay-power product (DP), and it can write as:

$$DP = P_D t_p \quad (9)$$

The lower the of DP product the more effective is the technology, which is used for fabrication device.

III. Results and Discussion

The dependence of the CMOS propagation delay time t_{PLH} on the NMOS transistor transconductance parameter (k_n) for two different (parametric) values of the NMOS transistor threshold voltage ($V_{t0,n}$) and other values remains constant. This is shown in Fig. 5.

The results presented through curves in Fig. 5 indicate the following: for higher values of the NMOS transconductance parameter (k_n) in CMOS inverter, the propagation delay time t_{PHL} (the propagation delay time during output voltage transition from high-to-low level) will be lower. Also, the smaller value of the NMOS threshold voltage ($V_{t0,n}$) will result in lower values of the propagation delay time t_{PHL}, with a more significant impact for the lower values of the NMOS transconductance parameter (k_n).

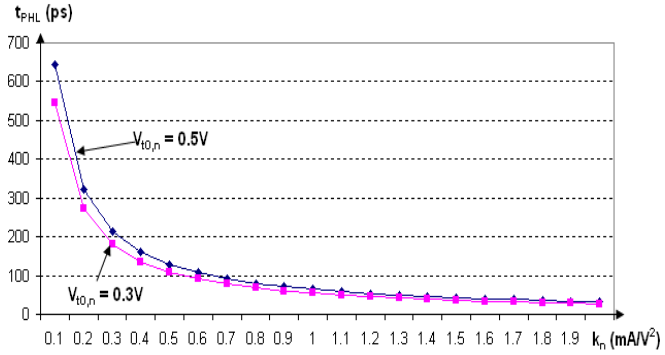

Fig. 5 The dependence of propagation delay time t_{PHL} in the CMOS inverter on the NMOS transconductance parameter (k_n) for two different values of NMOS threshold voltage ($V_{t0,n}$), when C_l = 0.1 pF and V_{DD} = 2.5 V.

The dependence of the CMOS propagation delay time t_{PLH} (the propagation delay time during output voltage transition from low-to-high level) on the transconductance parameter of the PMOS transistor (k_p), for two parametric values of the PMOS threshold voltage (by absolute value of the PMOS threshold voltage $V_{t0,p}$), and other values remains constant and it is same as the dependence of propagation delay time t_{PLH} in Fig. 5.

For the same dimensions of NMOS and PMOS transistors (complementary MOS transistors) propagation delay time in the CMOS inverter are asymmetrical $t_{PLH} > t_{PHL}$ (because $k_n > k_p$). While, for symmetrical (matching) conditions ($k_n = k_p$), the propagation delay times in the CMOS inverter are equal ($t_{PHL} = t_{PLH}$). In usual cases the maximal operation frequency in CMOS inverter circuits is determined by maximal value of propagation delay times.

The time response waveforms of the output voltage during low-to-high transition and high-to-low transition for three different cases of the complementary MOS transistors transconductance parameters ratio (k_n/k_p), when the CMOS inverter is driven by the ideal pulse (with zero rise and fall times) and with equivalent load capacitance C_l =1pF, is shown in Fig 6.

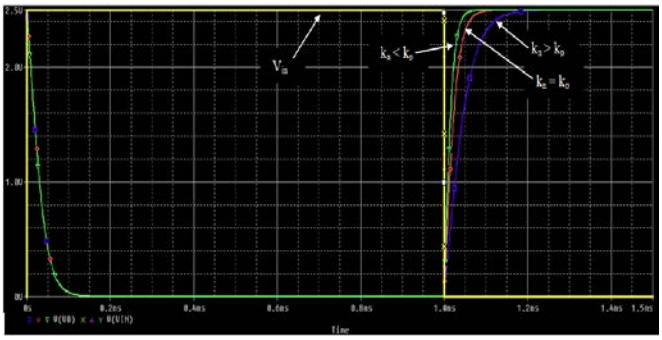

Fig. 6 The waveforms of output voltage for there different cases of the complementary MOS transconductance parameters ratio (k_n/k_p), when the CMOS inverter drives by the ideal pulse and equivalent load capacitance C_l = 1pF, as well the NMOS transconductance parameter (k_n) holds same.

From the time waveforms presented in Fig. 6, it is indicated that for symmetric cases ($k_n = k_p$), the propagation delay times during low-to-high and high-to-high transition of the output voltage in CMOS inverter are equal ($t_{PLH} = t_{PHL}$), whereas in other cases of the transconductance parameters ratio (k_n/k_p) the propagation delay times are asymmetrical. When $k_n > k_p$ the propagation delay time t_{PHL} is lower than propagation delay time t_{PLH} ($t_{PHL} < t_{PLH}$), and for $k_n < k_p$ the propagation delay time t_{PHL} is higher than the propagation delay time t_{PLH} ($t_{PHL} > t_{PLH}$).

Significant impact on propagation delay times has the load capacitance connected at the output of the CMOS inverter (when load capacitance (fan-out effect) connected at the output of the CMOS inverter is dominant term in the equivalent load capacitance, or extrinsic terms are dominant). The role of the output load capacitance (fan-out) in delay times is shown in Fig. 7 by the waveforms of the time response of the output voltage at the output of the symmetric CMOS inverter for three different values of equivalent load capacitance, when the CMOS inverter is driven ideal pulse. Form the waveforms of the time response in Fig. 7, it is indicated that the higher values of the equivalent load capacitance will result in higher values of the propagation delays during the transition of the output voltage in the CMOS inverter. Since the speed of the operation of the CMOS inverter depends of its propagation delay time, then the higher values of the propagation delay time will result in low speed of the CMOS inverter operation. When the combined output load capacitance is mainly dominated by its extrinsic components (which are not very sensitive to the NMOS and PMOS device dimensions), the directive to increase the operation speed (decrease the propagation delay time) of the CMOS inverter is by designing the NMOS and PMOS transistors with higher values of the transconductance parameters. But, the intrinsic components of the combined load capacitance are increasing functions of the NMOS and PMOS transistor dimensions, W_n (the channel width of NMOS transistor) and W_n (the channel width of PMOS transistor) [12], [13].

$$C_l = f(W_n, W_p) = C_{gd,n}(W_n) + C_{gd,p}(W_p) + C_{db,n}(W_n) + C_{db,p}(W_p) + C_{\text{int}} + C_g \quad (10)$$

The channel lengths of the NMOS and PMOS transistors in the CMOS inverters are usually equal and fixed to each other, determined by fabrication process, and then the channel width of MOS transistor is more significant determining parameter of the MOS transistor transconductance parameter [14], [15]. Then, any effort to increase the channel width of NMOS and PMOS transistors in order to reduce propagation delay time in the CMOS inverter will inevitably increase the intrinsic components of combined load capacitance at the output of the CMOS inverter. Then increasing channel width of the complementary MOS transistors to reduce propagation delay time, where the intrinsic capacitance terms will have significant impact in equivalent load capacitance, the influence on the propagation delay time will diminish and will asymptotically approach a limit value for larger values of the channel width of complementary MOS transistor (the propagation delay time cannot be reduced beyond the limit value). In these conditions the propagation delay times are independent of the extrinsic capacitance components, C_{int} and C_g.

When the intrinsic capacitance components are dominant on combined load capacitance in the CMOS inverter (parasitic capacitance components of NMOS and PMOS transistors), the combined load capacitance will reduce by reducing the channel width of NMOS and PMOS transistors, and propagation delay time limit is reached for smaller values of the NMOS and PMOS transistor channel width.

The influence of complementary MOSFET transistors dimensions upon the propagation delay of CMOS inverter are inherently limited by parasitic capacitances, and overall occupied area by CMOS inverter should also be considered. In fact, the occupied area of CMOS device is proportional to W_n and W_p, since the other MOSFET dimensions are simply kept constant. The significant factor which used as practical measure for quantifying design quality is the (area x propagation delay time) that takes into account for delay time reduction [6], [15].

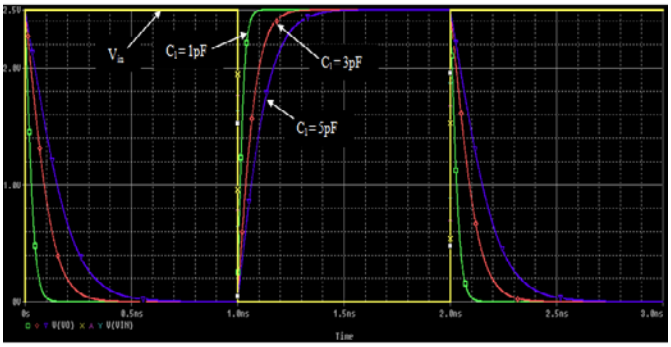

Fig. 7 The waveforms of time response of the symmetric CMOS inverter output voltage during switching conductions, when the equivalent load capacitance (C_l) has three different values.

All of the propagation delay times are derived under simplified assumption that the input driven signal is an ideal pulse, but in realistic cases the waveform of the driven input signal is not an ideal pulse. The real driven pulse at the input of the CMOS inverter has finite rise time (t_r) and fall time (t_f). The exact calculation of the output voltage propagation delay time is more complicated, because under these conditions both the NMOS transistor and PMOS transistor conduct during the charge-up and charge-down events. The estimation of the propagation delays of the CMOS inverter, when the driven input signal has finite rise and fall time, can utilize the propagation delay time calculated by ideal pulse (step-input) assumption and using the rise and fall time of the driven input signal, by using the empirical expressions [4]:

$$t_{PHL}(reale) = \sqrt{t_{PHL}^2(ideal\ pulse) + \left(\frac{t_r}{2}\right)^2} \quad (11)$$

$$t_{PLH}(reale) = \sqrt{t_{PLH}^2(ideal\ pulse) + \left(\frac{t_f}{2}\right)^2} \quad (12)$$

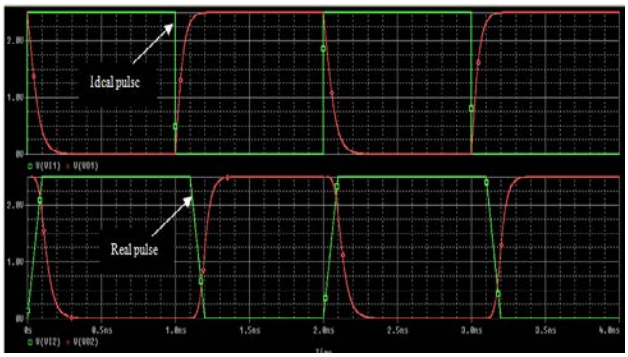

Fig. 8 The waveforms of the CMOS output voltage during switching conditions for ideal driver input signal and real driver input signal at the input of the CMOS inverter, when the equivalent load capacitance has fixed value C_l = 2pF.

The impact of the rise and fall time of the driven input signal on the waveform and propagation delay times of the output voltage during the switching conditions in the symmetric CMOS inverter, when the driven input signal is an ideal pulse and when the driven input signal has a finite rise and fall time, as well the equivalent load capacitance has a fixed value is shown in Fig. 8.

During switching conditions in CMOS inverter, there will be created the conduct path between the power source and the ground under realistic conditions (the input driven signal deviates from the ideal step pulse), through NMOS and PMOS transistor when the input voltage is larger than $V_{tn,0}$ and smaller than (V_{DD} -|$V_{tp,0}$|). Under these conditions the NMOS and the PMOS transistors will simultaneously conduct a nonzero current (drain current) during low-to-high and high-to-low transitions, and the current reaches its peak value when the input voltage is equal to the CMOS threshold voltage V_{in}= V_{th}. Otherwise, the short-circuit current of CMOS invertor is called the power supply current. Both the NMOS and PMOS

transistors operate in the saturation mode of operation when the current reaches its maximum (peak value) [8], [15].

$$I_{DD} = \frac{k_n}{2}(V_{in} - V_{t0,n})^2, \quad (V_{t0,n} \le V_{in} \le \frac{V_{DD}}{2}) \tag{13}$$

$$I_{DD} = \frac{k_p}{2}(V_{DD} - V_{in} - |V_{t0,p}|)^2, (\frac{V_{DD}}{2} \le V_{in} \le V_{DD} - |V_{t0,p}|) \tag{14}$$

The CMOS inverter does not draw any significant current from the power source, when the input voltage is smaller than V_{tn} or larger than (V_{DD} - $|V_{t0,p}|$), except some small leakage and subthreshold currents. From the expression above, it is concluded that the transconductance parameters of the NMOS and PMOS transistors and the threshold voltage of the NMOS and PMOS transistors have impact in the current peak value. The dependence of the drain current peak value from the transconductance parameters of the NMOS and PMOS transistors in the symmetric CMOS inverters is shown in Fig. 9. The achieved results indicate that when the transconductance parameters of the both NMOS and PMOS transistor increase the short-circuit current peak value of the symmetric CMOS inverter during output voltage transition will increase. Thus, the higher values of the transconductance parameters will result to the higher value of short-circuit current and the higher value of dynamic power dissipation term.

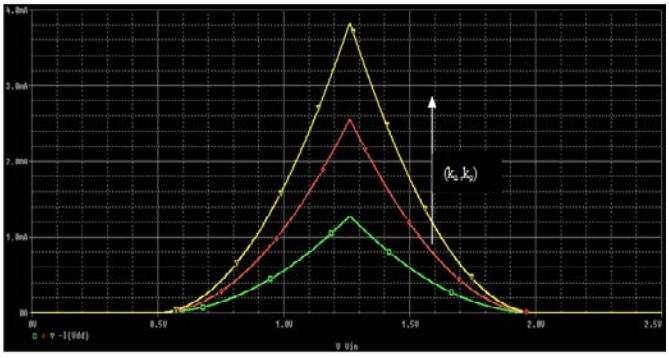

Fig. 9 The short-circuit current in the symmetric CMOS inverter during switching operation when the transconductance parameters of the NMOS and PMOS transistors increase proportionally.

The impact of the threshold voltages of the NMOS and PMOS transistors on short-circuit current peak of the symmetric CMOS inverter, when the transconductance parameters of both MOS transistors are fixed, is shown in Fig. 10. The achieved results indicate that when the value of the threshold voltage of the NMOS transistor and the absolute value of the threshold voltage of the PMOS transistor are smaller, the short-circuit current (drain current or power supply current) peak value of the CMOS inverter will be larger by values during the transition operation.

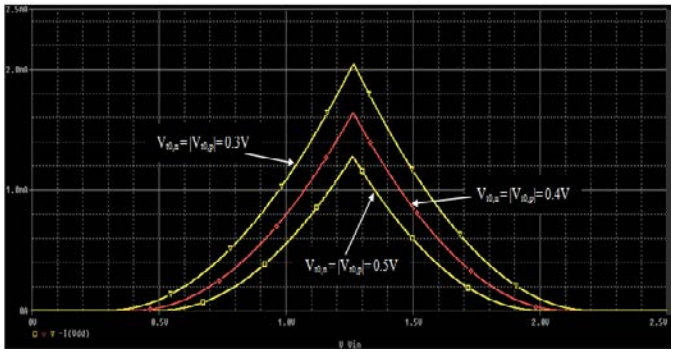

Fig. 10 The waveforms of the power supply current (short-circuit current) in the symmetric CMOS inverter, for some different values of the threshold voltages of the NMOS and PMOS transistor during transition operation, when the transconductance parameters are fixed.

The impact of the channel- length modulation effect (λ) in the power supply current (short- circuit current) of the CMOS inverter during transition operation is shown in Fig. 11. By waveforms presented, the larger values of the channel length modulation constant (λ) will result in larger peak values of the power supply current of CMOS inverter, but does not have any significant impact compared to the transconductance parameters and threshold voltages of complementary MOS transistors.

The power supply current of the CMOS inverter during transition operation will contribute in the overall power dissipation of the CMOS inverter under non ideal conditions, with significant role when output load capacitance has a lower value. The waveforms of short-circuit current (power supply current) and its peak value on same different values of equivalent load capacitance are shown in Fig. 12.

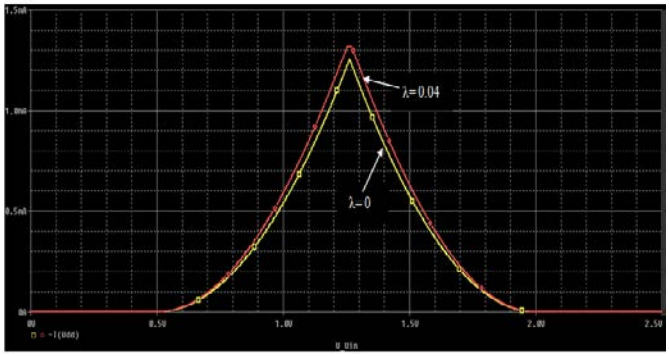

Fig. 11 The waveforms of the power supply current of the CMOS inverter for two parametric values of the channel length modulation constant (λ) during transition operation, when the transconductance parameters of the NMOS and PMOS transistors and their threshold voltages are fixed.

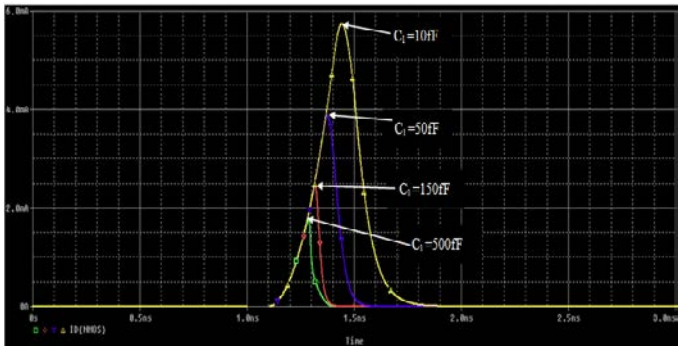

Fig. 12 The dependence of the power supply current peak value in the CMOS inverter on equivalent load capacitance (combined load capacitance).

In general, the larger supply voltage V_{DD} results in lower a lower value of propagation time delay t_p. But, the dynamic power dissipation of CMOS inverter will rise by expression (8), the short-circuit current will be higher, thus the overall dynamic power dissipation will rise. However, the supply voltage V_{DD} is determined by process technology and thus it is not under the control of the designer. Moreover, modern process technologies in which device size are reduced continually require lower value of V_{DD}.

An important issue is the fact that propagation delay time for sub-micron MOSFETs cannot estimate by expressions (3) and (4), but have to modify. In sub-micron transistors (or a small-geometry transistor) the current driving capability reduced as ea result of channel velocity saturation. By using the saturation current of a deep-sub-micron MOSFETs, and the average current method for estimate the propagation delay times, the expression of the propagation delay time is [16], [17]:

$$t_{PHL} = \frac{C_l (V_{DD}/2)}{\kappa W_n (W_{DD} - V_{t0,n})} \tag{15}$$

The propagation delay time for sub-micron transistors has a weak dependence on the power supply voltage compared on the propagation delay times estimate by expressions (3) and (4). The obtained results by this expression have an accurate about 90%, but to achieve the better results must use the another MOSFET model for sub-micron transistors.

The obtained results for switching characteristics of the CMOS inverter on specific parameters discussed until now, also can apply to all general CMOS circuits. The CMOS circuit consists of two blocks of MOSFETs, a block of the NMOS transistors and a block of the PMOS transistors, which can be simplified to one equivalent CMOS inverter with equivalent parameters [6].

IV. Conclusion

If during the design phase of the CMOS inverter, the transconductance parameters of the complementary MOS transistors, i.e. the transconductance parameter of the NMOS transistor (k_n) and the transconductance parameter of the PMOS transistor (k_p), and the threshold voltage values of complementary MOS transistors, i.e the threshold voltage of the NMOS transistor ($V_{t0,n}$) and the threshold voltage of the PMOS transistor ($V_{t0,p}$), are controlled, or matched, the CMOS inverter can be designed with high performance in the dynamic conditions of operations, depending on the designer requirements and operating conditions.

For the higher values of complementary MOS transistors' transconductance parameters (k_n and k_p), the propagation delay times during low-to-high (t_{PLH}) and high-to-low (t_{PHL}) transition of the CMOS inverter output voltage will have lower values, when in equivalent lumped load capacitance dominate the extrinsic components. But increasing the transconductance parameters beyond certain values, the influence on propagation delay time will diminish, and the propagation delay time will asymptotically approach the limit values. When in the equivalent lumped capacitance dominate the intrinsic components, the limit values of the propagation delay time are reached for smaller values of the complementary MOS transistors' transconductance parameters. The increasing of the transconductance parameters of complementary MOS transistors in CMOS inverter are reached by increasing the channel width of the complementary MOS transistors. But the increasing of the channel widths will inevitably increase the intrinsic components of the equivalent lumped load capacitance. If transconductance parameters of complementary MOS transistors are equal or matching ($k_n = k_p$), the propagation delay times are equal (symmetric), and for other cases the propagation delay times will be asymmetric. The MOSFETs transconductance parameters ratio is determined parameter of the propagation delay times ratio in the CMOS inverter.

For the lower value of the NMOS transistor threshold voltage ($V_{t0,n}$) and higher value (or lower absolute value) of the PMOS transistor threshold voltage ($V_{t0,p}$), the propagation delay times during output voltage transitions in CMOS inverter will decrease and vice versa.

The nonzero rise and fall time of the driver signal at the input of CMOS inverter will have significant influence to the propagation delay time during output voltage transition, and the higher value of rise and fall time of driven input signal (input pulse) at the input of CMOS inverter will lead in increasing the propagation delay times.

The nonzero rise and fall time of input driver signal (input pulse) and the complementary MOS transistors transconductance parameters in CMOS inverter will have influence in short- circuit current (power supply current) during output voltage transition, and the higher values of rise and fall time of the input driver signal, as well the higher values of complementary MOS transistor transconductance parameter, will result in higher values of the short- circuit current, as well in higher value of the overall dynamic power dissipation of the CMOS inverter.

Another parameter called the channel length modulation coefficient (process-technology parameter), that has to be taken into account especially when MOSFET is defined as a short-channel device, then for higher value of the channel length modulation coefficient (λ) will have a small increase in

the value of the short- circuit current peak during the output voltage transition of the CMOS inverter.

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