An FPGA-based pulse integration system to improve the SNR of radar echo

Chengchang Zhang, Sa Yu, Lihong Zhang, Yuwen Gong

***Abstract*—**An efficient pulse integration scheme based on FPGA to improve the signal to noise ratio (SNR) of received radar echo is presented. Radar echo is mixed with noise, due to noise interference, useful radar signals may be completely submerged in noise, it is difficult for radar receiver to detect useful target signals. With the benefit of FPGA high speed and parallel computing features, it is developed by sampling multiple cycles received radar echo, storing and accumulating the sampled data in FPGA. Useful radar pulse in radar echo mixed with noise is coherent in different cycles, the process of accumulation makes the value of radar pulse increase, whereas the noise is random, the change of noise is not obvious. So, radar pulse is strengthened, otherwise noise is suppressed. In ideal case, the integration for M cycles of radar echo can increase SNR by M times. This method provides a valuable method for radar design, especially, it is valuable for the digitization and miniaturization of radar receiver.

***Keywords*—**Detection, FPGA, Integration, Radar, Signal to Noise Ratio.

I. Introduction

THE pulse radar transmits and receives pulse sequence by setting a certain threshold to detect echo signal [1]-[2]. If radar echo's SNR is high enough, it can be detected easily. However, the difficult is that the pulse echo is always mixed with a large number of random noises, or that the useful pulse signal is completely submerged in the noises, which result in a low SNR and make it cannot correctly detect the echo pulse [3], [4]. How to improve the SNR of the echo signal is the key to improve radar detection capability. Pulse integration is an effective method to solve this problem [5]-[9], it is employed in radar receivers to combine the signals received in multiple pulses from the target within one scan in order to increase the SNR. Increased SNR results in increased probability of detection and reduced probability of false alarm.

Pulse integration in early radar system [1] was to rely on the accumulation of the afterglow of the display screen combined with integration function of the operator's eyes and brain, or design mainly based on complex analog circuits and devices, which could not meet the needs of development.

Based on analog to digital conversion technology and Field Programmable Gate Array (FPGA) [10]-[12], this paper proposes an efficient pulse integration scheme to improve the quality of received radar echo in aerospace exploration, which can provide a new technique to realize the miniaturization, digitization and power efficient of radar system design.

The mainly work are as below:

1) We propose a new FPGA-based radar pulse integration technique.

2) We derive mathematical expressions for pulse integration.

3) We develop a prototype system to verify the performance of FPGA-based integrator.

The remainder of the paper is organized as follows. In the next section, we introduce the principle and threshold detection of pulse radar. In section III, we analyze the radar pulse integration performances, deduce the mathematical expression of pulse integration, and give the simulation result of the pulse integration. Section IV describes the scheme of FPGA-based pulse integrator, the function of each part, and a detailed description of the working process of the integrator. Experimental results are given in Section V. Finally, section VI concludes the present paper and makes some comments.

II. Range-measuring Principle of Pulse Radar

A. Principle of Pulse Radar

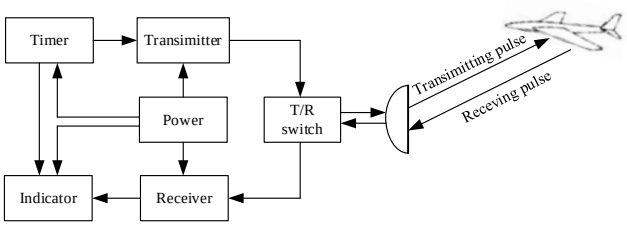

Fig.1 Pulse radar systems

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Measuring the distance of the target is one of the basic tasks of pulse radar. The simple systems block diagram of pulse radar is as shown in Fig.1.

Pulse radar systems mainly include timer, transmitter, receiver, power, indicator, T/R(Transmitter/Receiver) switch and antenna. Radar transmits signal outward, and receives echo signal from target. According to the echo signal, radar judges whether the target is and calculates the distance of the target.

Radar ranging principle is shown as Fig.2.

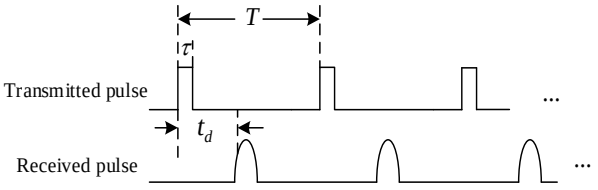

Fig.2 Radar ranging schematic

Radar transmits a narrow pulse sequence, which pulse width is , pulse circle is *T*. The distance *l* of the target is directly related to the time delay between transmitted pulse and received one, which can be expressed as

$$l = \frac{ct_d}{2} \tag{1}$$

where *c* is the velocity of electromagnetic wave. It is a fixed value in homogeneous medium (c=3×10^{8}m/s). The distance between the target and the radar can be obtained by measuring the delay time.

B. Threshold Detection

The block diagram of the radar receiver with the envelope detector is shown in Fig.3. The input signal of the receiver is composed of the radar echo signal and additive white gaussian noise(AWGN).

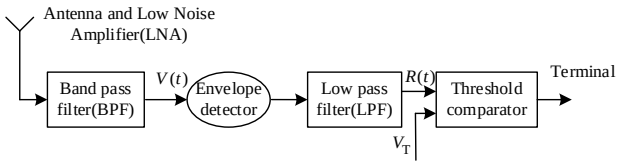

Fig. 3 The diagram for Radar receiver

The noise in receiver is Gauss noise with wide frequency band, and the ability to detect weak signal of receiver will be limited by the noise energy of the same frequency band as the signal energy spectrum.

Because of the fluctuation of the noise, it becomes a statistical problem to detect the signal, which must be judged according to some statistical standard. Neyman-Pearson criterion is usually used in radar signal detection. The implementation of this criterion is to compare the received echo signal pulse with a preset threshold voltage, if the envelope amplitude exceeds the threshold voltage, the target is considered to exist, otherwise, the target does not exist, which is as shown in Fig.4.

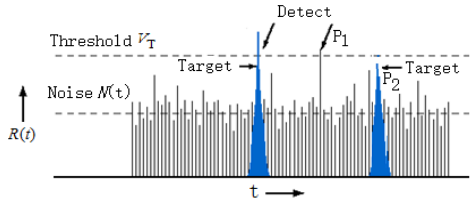

Fig.4 Threshold detection

If the echo signal is clear enough, receiver can easily detect it, however, useful signals may be disturbed by noise, even completely submerged in noise, thus, false detection and missed detection are often occurred. False detection is that the instantaneous value of noise is greater than the threshold voltage, receiver detects the noise as target signal mistakenly, which is indicated as P_1 in Fig.4, missed detection is that although the target appears, but the receiver does not detect useful signal, which is indicated as P_2 in Fig.4.

So, the key to accurately determine the target is to improve SNR and avoid false detection and missed detection. In this paper, we propose a scheme of pulse radar integration based on FPGA, which can improve the signal to noise ratio and improve the quality of radar detection.

III. Integration Performance Analysis

A. Mathematical model

Assuming a cycle of target echo *R(t)* is a combination of the ideal echo radar pulse *S(t)* and zero-mean Gauss white noise *N(t)*, which is expressed as

$$R(t) = S(t) + N(t) \quad (0 < t < T) \tag{2}$$

where *S(t)* is a known signal, each cycle is identical. *T* is the echo signal period. *N(t)* is a random signal that every cycle is independent from each other. The SNR of *R(t)* can be expressed as

$$\left(\frac{S}{N}\right)_1 = \frac{[S(t)]^2}{E\{[N(t)]^2\}} \tag{3}$$

where *E{*}* is the calculation of mathematical expectation. Simple integration of *M* cycles of target echo signals can be expressed as

$$\begin{aligned} \sum_{i=1}^{M} R_i(t) &= \sum_{i=1}^{M} [S_i(t)+N_i(t)] \\ &= M \cdot S(t) + \sum_{i=1}^{M} N_i(t) \end{aligned} \tag{4}$$

The integrated signals' SNR is:

$$\left(\frac{S}{N}\right)_M = \frac{[M\cdot S(t)]^2}{E\{[\sum_{i=1}^{M} N_i(t)]^2\}} = \frac{M^2[S(t)]^2}{E\{\sum_{i=1}^{M}[N_i(t)]^2\}+E[\sum_{i\neq j} N_i(t)N_j(t)]} \quad (5)$$

Since the noise of each cycle meet the statistical independence conditions:

$$E[\sum_{i\neq j} N_i(t)N_j(t)] = 0 \quad (6)$$

So:

$$\left(\frac{S}{N}\right)_M = \frac{M^2[S(t)]^2}{E\{\sum_{i=1}^{M}[N_i(t)]^2\}} = \frac{M^2[S(t)]^2}{M\cdot E\{[N(t)]^2\}} = M\cdot\left(\frac{S}{N}\right)_1 \quad (7)$$

So far, it can be seen that the pulse integration can effectively improve the quality of the received signals. In ideal case, the integration of *M* cycles of echo signal can increase the SNR by *M* time.

B. Simulation

The simulation result of pulse integration is shown as Fig.5.

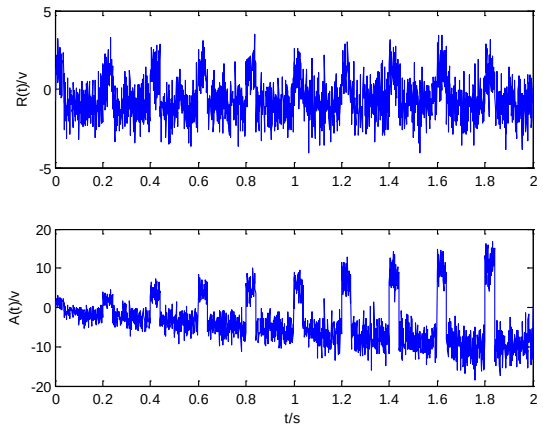

Fig.5 The simulation of pulse integration

where *R(t)* represents target echo radar pulse, which is composed of the ideal radar pulse with 20% duty cycle and random noise. The SNR of *R(t)* is 0dB. *A(t)* is the result of simple superposition of *M* (*M*=1, 2, …, 9) cycles of target echo signals.

It can be seen from the simulation result of integration, with the number of integration increasing, the amplitude of the useful signal is increasing, while the amplitude of the noise is basically unchanged, the quality of the echo radar pulse has obtained significantly improved.

IV. Design of FPGA-Based Pulse Radar Integrator

A. The system composition

We develop a prototype system to verify the performance of FPGA-based integrator, which mainly includes three parts, as shown in Fig.6, they are analog to digital converter (ADC), Field Programmable Gate Array (FPGA), and digital to analog converter (DAC), separately.

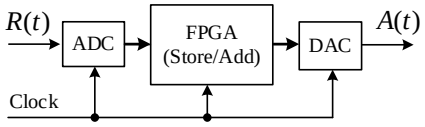

Fig.6 Block diagram of pulse integration system

The analogue echo signal *R(t)* is first converted into digital signal by ADC, and inputted to FPGA to store and integration, in the end, the integrated digital signal is inputted to DAC to reproduce the radar pulse whose SNR is improved.

B. Working flow of radar pulse integration

The process of radar pulse integration is shown in Fig.7.

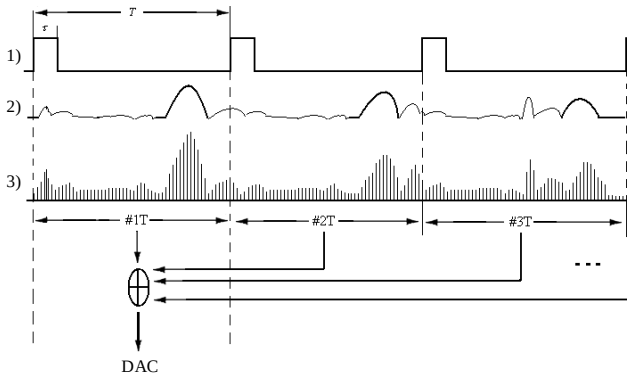

Fig.7 The working flow of pulse integration

1) Transimitted pulse

2) Echo pulse

3) Sampling pulse

First, the sampling data of the first cycle (#1*T*) are stored in memory with *N* FPGA cells, the value of *N* depends on the ratio of sampling frequency to the radar pulse one.

From the second cycle (#2*T*), while sampling a new value, it reads out the former period value corresponding to the same time from memory, and adds the two periods data, then saves the result back to the original cell. After the second cycle, the memory will be stored for the integration value of the first two

cycles, and so on, the memory has stored the value of *M* cycles target echo integration after #*MT* cycles later, the process of storing and adding is completed.

In the #(*M* +1) cycle, the integration value of *M* cycles is read out and inputted to the DAC for analog to digital conversion. While the data reading out from the memory, the memory is cleared to prepare for the next process of integration.

C. FPGA-Based pulse integrator

The scheme of FPGA-Based pulse integrator is shown in Fig.8, which mainly consists of several functional modules, which are Code conversion and Sign extension, Integration times control, Add and Reset, Read and Write Addresses generation, Dual-port RAM and Adder.

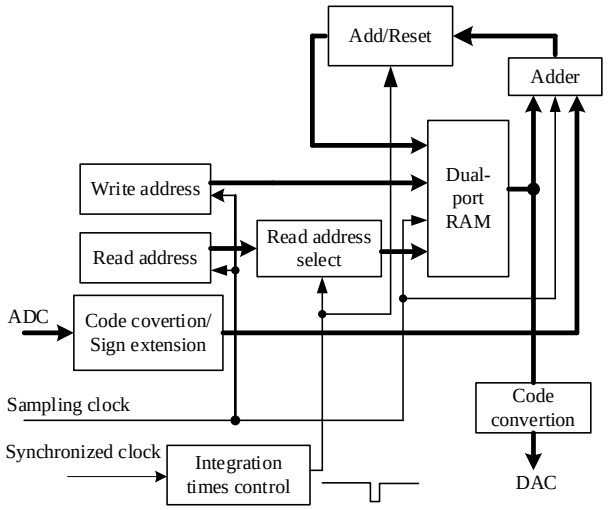

Fig.8 The scheme of integrator in FPGA

1) Code conversion/Sign extension

Usually, the format of output data of ADC is offset binary code, however, the data format of FPGA is two's complement, therefore, the output data of ADC need to be performed code conversion, and then input to the FPGA to complete the accumulating process. Meanwhile, the data should also need sign bit extension in consideration of the overflow. And the output data of FPGA should also need corresponding code conversion before it is sent to the DAC.

2) Integration times control

A counter is used to count up for synchronizing clock to control accumulation times. When the counter's carry bit is high level, it illustrates that the system is in accumulating period, and when it's low, it means that the calculation is completed and the counter is reset for the next integration cycle.

3) Add/Reset

Add/Reset module is used to control the input data of dual-port RAM. It reads the adder's data when the system in the accumulation cycles, and is cleared for the next accumulation cycle when the process of accumulation is completed.

4) Read/Write Address

It is designed to generate the RAM read and write addresses. In the accumulation cycle, the write address of the RAM should lag read address three clock cycles in order to ensure that the read and write address are consistent because the dual-port RAM needs reading, adding and writing in one accumulation period and thus consuming three clock cycles. While in the dual-port RAM cleared cycle, as long as the write addresses lags the read address one clock cycle, all of the memory cell data can be sequentially read out and cleared. The conversion of read address is completed in Read address select module.

5) Adder

The operation of accumulation is completed in the adder.

6) Dual-port RAM

The dual-port RAM is able to read and write at the same time, however, it does not mean that it can simultaneously read and write the same address unit, but it can read and write different address unit, such as read *n1* unit while write *n2* unit, which $n2 \neq n1$. This function of storage and accumulation simultaneously is completed based on the way of pipelining. And there are two methods can be selected to output the data from the dual-port RAM to the DAC, one is that the result of integration is outputted after *M* times adding operation is completed, the other is that the result of integration is outputted while each adding is going on. In order to observe output process of the DAC clearly, this paper adopts the latter.

In addition, it also needs two clocks to ensure normal operation of FPGA, one is used for modules of read/write address survival, dual-port RAM and adder, which is the same clock with the ADC, that is also the sampling clock; the other is synchronized clock whose frequency is the same as the radar pulse.

V. Experimental Verification

In order to verify the function of the FPGA-Based pulse integrator, an experimental circuit board is designed, which primary devices, such as ADC, FPGA and DAC are respectively AD9057, EP1K30TC144 and THS5671A. The resolution of AD9057 is 8 bit and THS5671A is 14 bit. The main parameters of experiment are shown in Table I.

Table I The parameters of experiment

Description	Value
Radar pulse frequency	10KHz
Sampling frequency	5.12MHz
Duty cycle	20%
Input pulse SNR	-6dB
Integration times	15
Synchronized clock frequency	10KHz

The frequency of input radar pulse is 10 kHz, which is generated by the arbitrary waveform generator in the experiment. In order to simulate the actual received pulse, we can add up random noise thereon, and the superposition signal's SNR is -6dB. The sampling clock frequency is 5.12 MHz, so during each pulse cycle the ADC samples 512 points. Since the conversion resolution of ADC is 8bit, and the conversion resolution of DAC is 14 bit, so the number of accumulation time in FPGA cannot exceed 63 (2^{14-8}-1). In order to reduce the complexity of design, at the same time not affect observing the

effect of integration, the time of integration for radar pulse in this article is selected as 15. The synchronized clock frequency is 10KHz. Adding every point sampling data from #2*T* to #15*T* cycles onto the #1*T* cycle, and during each cycle the corresponding (like the first point of the #1*T* cycle and the first point of #2*T* cycle) points adding simply, and so on. At the end of each cycle, the data in the RAM is read out and sent to the DAC for analog to digital conversion, while at the #16*T* cycle the RAM is cleared to prepare for the next 15 cycles calculation.

We verified the pulse integrator ability in the experimental circuit board, Fig.9 shows the testing waveforms, where channel 1 (Ch.1) is the input signal, and channel 2 (Ch.2) is the output pulse. Since the analog input range of AD9057 is 1Vp-p, in order to make the phenomenon of test more obvious, the amplitude of input signal is close to 1V. From the output radar pulse in Ch.2, it can be seen that the useful radar pulse amplitude increases gradually, however, the amplitude of noise did not change significantly with the increasing of accumulation time. Thus, the SNR of output radar pulse is improved effectively.

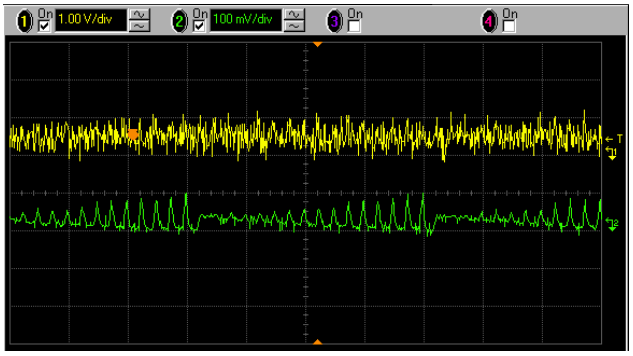

Fig.9 The testing waveforms

Ch.1 The input pulse

Ch.2 The output pulse

In order to observe the pulse accumulation process, the result of integration is outputted to complete the digital to analogue conversion while every time accumulation is going on in experiment. While in actual radar system, it can only output the last result, as this design, it can only output the result after 15 times accumulation for radar detection.

VI. Conclusion

A new pulse integration technique based on FPGA to improve radar detection performance is proposed. Firstly, we analyze the performance of radar pulse integration, deduce the mathematics expression of integration, and give the simulation results. Secondly, the scheme of FPGA-based integrator is designed, the internal modules are introduced and a detailed description of the working process of the integrator is given. In the end, the pulse integrator ability is verified in the experimental circuit board. It can be seen that the integrator can effectively improve the SNR of the received pulse. Pulse integration can be realized in real time based on high speed and parallelization of FPGA. It has engineering value for pulse radar miniaturization and digitization.

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