Cognitive Adaptive Travelling Window Filter Technology Implementation On Heterogeneous Multi-core Architecture

V.Jean Shilpa , Dr.P.K.Jawahar

Abstract**—**Low frequency signals are corrupted mainly by high frequency noise signals. In the last few decades many efficient algorithms have been proposed to design FIR filters for noise suppression in digital signal processing systems. Majority of these algorithms focus on static noise suppression techniques for noisy signals of different frequency. To overcome this major drawback, this paper proposes and designs Cognitive adaptive travelling (CAT) window algorithm for adaptive noise suppression, with flexible architectural changes to FIR filter structure based on the frequency and amplitude of the noise signal. CAT algorithm for FIR filters is designed using windowing technique which is hybrid of different traditional existing windowing techniques. This adaptive filter achieves 17% fall off, of the first side lobe noise to suppress the noise contents with 47% fall of rate of maximum side lobe noise levels achieving a side lobe role-off factor from -13 dB to -16.9 dB compared to static FIR filters. With the above achieved improvements, the hybrid CAT window is 23% efficient compared to static FIR filter. With Zynq processor being an implementation platform, CAT window FIR filter is efficiently mapped to an efficient heterogenous multicore architecture.

Keywords: FIR filters, Hanning window, Hamming window, Heterogenous-multicore, Zynq.

I.INTRODUCTION

Heterogenous multicore design have become very easily feasible with the evolution of embedded processor FPGA boards [1]. The move towards heterogenous-multicore systems is due to their wide applications in image processing, internet of things, multimedia services and all portable low power consuming devices[2]. The data intensive applications demand low power and energy constrained platform. Pertaining to this Zynq processor is identified as a right platform for portable, reconfigurable, low power and low cost device designs [3]. Most of the applications and design are getting shifted towards multicore architectures, in order to grab maximum advantage of different cores to boast their over all performance [4]. The field of signal processing having a strong wealthy background, craves for a implementation platform that gives maximum throughput [5].

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Filtering is the process of improvising the quality of the signal by extracting the information of the signal [6], with suitable removal of noise factors. Signal separation and restoration are the two main features of filtering in Digital Signal Processing. This field of study is dominated by the most stable and highly performing Finite impulse response filters because of their linear phase, non-recursive nature and feed forward implementations [7,8]. The inputs to the digital filters are the fixed filter co-efficients being multiplied with the input noisy signal [9]. Filter coefficient values are predetermined in digital signal processing applications and remain constant, hence making FIR filter are easily realizable. But fixed filter co-efficient do not aid in removal of artifacts and interferences in non stationary noise signals[10].

The design of FIR filter in this paper is carried out using the newly proposed cognitive adaptive travelling window algorithm. The algorithm focuses on the design of a new window function methodology to generate co-efficients for FIR filter that are made adaptive with the input high frequency noise signals to suppress accordingly. The architecture is well planned for hardware and software partitioning, accomplished by heterogeneous mapping and fitting on Zynq system on chip board. The partitioning is optimized by fitting CAT window FIR filter in the reconfigurable FPGA part of the chip as a user designed IP and the master controller unit is ported to hardware unit of the chip(dual cortex A9 ARM processor) forming a heterogenous multicore architecture.

The remainder section of the window is organized as follows. Section 2 introduces FIR filter design with traditional windowing technique and the proposed CAT window is elaborated in section3. Section4 discusses the experimental results and section 5 finally concludes the advantages of implementing he designs on heterogenous multicore processors.

II.FIR FILTER DESIGN BY WINDOWING TECHNIQUE

The weighting, tapering and apodization functions for an FIR filter are well known as window function. They are simple mathematical functions whose value is zero-valued outside a specified interval. Choosing an appropriate window function for filtering the signals in the right application decides the quality of the filtered signals [11]. FIR filter design is carried out in two phases, the approximation phase and the realization phase. The transfer function is obtained

from the approximation phase. The second phase of the algorithm is to develop a structure for implementing the obtained transfer function through programming or a circuit level structure.

Design of Finite impulse response filters are carried out by three major processes. Windowing method, the frequency sampling technique and optimal filter design methods. But the simple and efficient methodology being the windowing technique, designed to exactly truncate the impulse response based on the shape of the window. But this process leads to Gibbs phenomenon effect, giving a constant value of overshoot and a discontinuity in the frequency response due to the presence of ripple leading to non-uniform convergence of the fourier series resulting in discontinuity. The ripple factor was very high due to sudden truncation. The other side effects being the width of the transition bandwidth depends on the width of the main lobe of frequency response of the window function, secondly since the signals are characterized in frequency response the multiplication process is changed to convolution process which makes the filter always non optimal and as the length of the filter increases, the transition bandwidth reduces and the ripples increases.

To over come the disadvantages of the rectangular window function, the window functions are designed using complicated cosine functions well known as hamming, hanning and blackmann window techniques that provides better truncation which is smoother and the frequency response better comparatively.

A.Existing windowing Techniques

The window functions aids in the process of truncation. When an infinitely ranged continuous time signal is multiplied with a rectangular window function in continuous time domain given in equation

$$f(t) = \begin{cases} 1, \\ 0 \end{cases} |t| \leq \tau \quad (1)$$

the side effects that occur after the process of truncation is that the frequency is not localized to one particular value instead it has a series of spurious peaks called side lobes fig 1. They give raise to a number of frequency components instead of the desired value. To overcome this effect different window functions are applied to give a lower side lobes. Also when the fundamental input frequency of the input signal is not an integer multiple of the sample length, it gives rise to side lobes and this effect is termed as frequency leakage effect. Considering all the effects, the two possible ways to reduce the side lobes is, one is to limit the frequency component of the input signal to integer multiple of the fundamental frequency or choose an appropriate window function to have lower side lobe amplitudes in the frequency domain representations.

To thoroughly elaborate the windowing method used for FIR filter design, the following relation explains the relationship between the unit sample response $h_d(n)$ and desired frequency response $H_d(w)$ shown in (2) and (3)

$$hd(n) = \frac{1}{2\pi}\int_{-\pi}^{\pi} Hd(w)\ e^{jwn}\ dw \quad (2)$$

$$Hd(w) = \sum_{n=-\infty}^{\infty} hd(n)e^{-jwn} \quad (3)$$

$h_d(n)$ the unit sample response is infinite in the duration specified in the equation above. For the design of FIR filter the equation is being truncated to the length N-1 for the length of the filter N. The process of truncation is derived by multiplying the input noisy sample of the filter with the window [13,14].

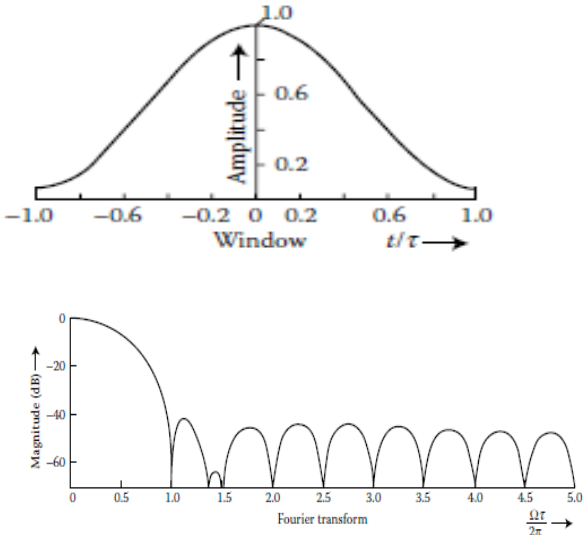
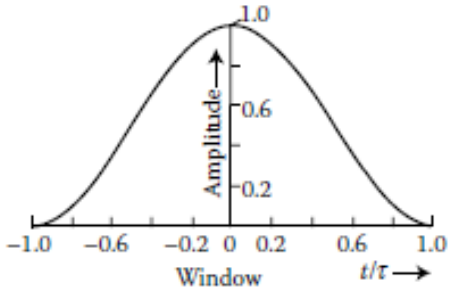


Fig 1 : Magnitude in dB representation of the discrete time rectangular function.

Further more to reduce the transition width of the main lobe the hanning window is a refined form of the truncated taylor series window shown in fig 2, the fourier transform of the window is represented as

$$f(x) = \begin{cases} 0.5 + 0.5\cos(\frac{\pi t}{\tau}), & t \leq \tau \\ 0, & elsewhere \end{cases} \quad (4)$$



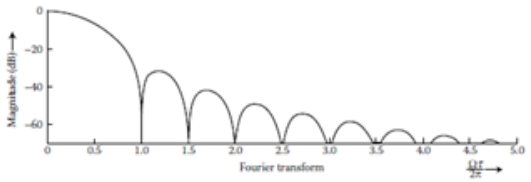


Fig 2 : Magnitude in dB representation of the discrete time hanning window function

An optimal form of hann window is the hamming window shown in fig 3, the coefficients generated are such that the first side lobe level have a reduced value, with this advantage hamming window has wide applications in optics for apodization , smoothens the input intensity of input signals etc. The fourier tranform of hamming window is

$$f(x) = \begin{cases} 0.54 + 0.46\cos(\frac{\pi t}{\tau}), & t \le \tau \\ 0, & elsewhere \end{cases}$$

(5)

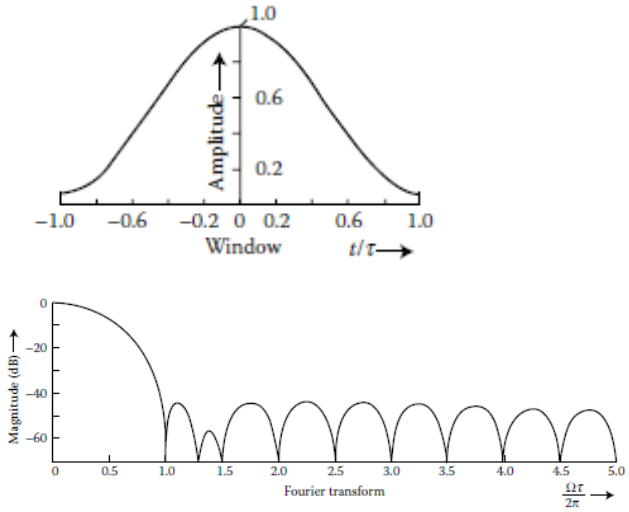


Fig 3 : Magnitude in dB representation of the discrete time hamming window function

III.THE COGNITIVE ADAPTIVE TRAVELLING WINDOW DESIGN.

The combined advantages of Hann and Hamming window are employed to give a reduced main lobe width, where maximum energy is concentrated and to achieve faster side lobe roll off. To design the hybrid window is to take a product function of both the window functions and maintain the α value adaptive between 0.5 to 0.9 [12]. The derived hybrid window functions is given by (6)

$$c_0 = \frac{(\alpha + \alpha^2)}{2};$$
$$c_1 = \alpha;$$
$$c_2 = \frac{(\alpha - \alpha^2)}{2};$$
$$f(x) = \begin{cases} c_0 - c_1\cos\frac{2\pi t}{\tau - 1} + c_2\cos\frac{4\pi t}{\tau - 1} & t \le \tau \\ 0, \ eleswhere \end{cases} \quad (6)$$

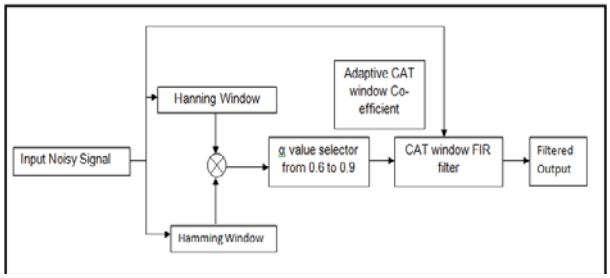


Fig 4: Block diagram representation of Cognitive adaptive travelling window.

As the value of α increases between 0.6 to 0.8 the first side lobe level and the maximum side lobe level reduces by 15 dB. Table 1 describes the various window parameters obtained for the traditional hanning, hamming and the proposed CAT window for α = 0.5, Hybrid_Hanning_Hamming1 for α = 0.6, Hybrid_Hanning_ Hamming2 for α = 0.7, Hybrid_Hanning_Hamming3 for α = 0.8, Hybrid_Hanning_Hamming4 for α = 0.9. Signals intended to reduce the noise exactly at the main lobe can choose α value between 0.6 to 0.8 shown in fig 4. The side lobe roll off falls at a rate of 23% for increase in α value from 0.6 to 0.8.

Table 1: Comparative analysis of CAT window with Hanning and Hamming window functions.

Window	Normalized Half Main Lobe Width NHMLW	First Side Lobe Level (dB)	Maximum Side Lobe Level (dB)	Side lobe roll off dB/decade	Equivalent Noise Band width
Hanning	42	-31.48	-31.48	-13	1.5300
Hamming	43	-47.65	-42.53	-0.3	1.3823
Hybrid_Hanning_Hamming	61.35	-46.74	-46.74	-16.9	1.9833
Hybrid_Hanning_Hamming1	69.5	-56.52	-56.52	-16.2	1.8487
Hybrid_Hanning_Hamming2	89.69	-55.24	-56.52	-16.2	1.7418
Hybrid_Hanning_Hamming3	-69.17	-48.04	-47.63	-15.24	1.6559
Hybrid_Hanning_Hamming4	55.17	-37.13	-37.1	-16.4	1.5865

The window co-efficient are adaptive to the property of the signal. The property of the signal mainly depends on the amplitude and frequency of the input noisy signal. From the table 2 the signal-to- noise ratio for the filtered signal clearly displays that the SNR value increases linearly as the frequency of the noise signal increases ten times.

Table2: Analysis of SNR value for different types of High frequency noise signal

Window	SNR 1	SNR 2	SNR 3	SNR 4	SNR 5	SNR 6
Hanning	31.97 25	32.12 87	32.31 56	31.80 38	31.79 03	31.78 40
Hamming	31.45 23	31.66 29	31.90 88	31.21 54	31.19 56	31.18 62
Hybrid_Hanning_Hamming	31.66 64	31.75 24	31.86 07	31.58 23	31.57 64	31.57 37
Hybrid_Hanning_Hamming1	33.30 67	33.40 60	33.52 94	33.20 69	33.19 97	33.19 63
Hybrid_Hanning_Hamming2	34.70 48	34.81 77	34.95 66	34.58 86	34.57 98	34.57 58
Hybrid_Hanning_Hamming3	35.92 59	36.05 30	36.20 76	35.79 28	35.78 25	35.77 77
Hybrid_Hanning_Hamming4	37.01 24	37.15 39	37.32 46	36.86 18	36.84 99	36.84 44

V.IMPLEMENTATION OF CAT WINDOW FILTER ON HETEROGENEOUS MULTI CORE PLATFORM.

The developed CAT window is implemented on a heterogenous multicore platform to achieve high performance. To design a flexible heterogenous multicore architecture an FPGA(Field programmable gate array) [17] and an General purpose processor are interfaced to share the tasks. In the architecture, FPGA acts a softcore processor, flexible to any changes and dual cortex A9 processor acts as hardcore processor. The hard and the soft core processors are interfaced with an advanced bus structure, popularly known as AXI(Advanced extensible interconnect bus) extensible bus. Zed Board which belongs to zynq series of FPGA boards is particularly used for the applications where programmable logic as well as programmable software enhances the output performance.

In this design the CAT algorithm is implemented as an IP(Intellectual Property) and he ARM dual cortex A9 processor resides in the processing system portion of FPGA, which acts as a master and control's the slave IP the residing in the processing system part of FPGA unit. Fig 5 clearly shows the IP name my_hanning_hamming hybrid window IP developed and integrated with the ARM cortex A9 processor through the AXI interface generated by Vivado.

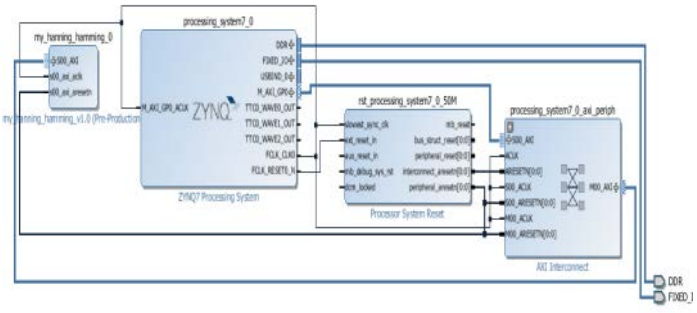


Fig 5 : Multicore Architecture of FIR filter with CAT algorithm

Now the various IP's that are added to form the heterogenous multicore are the zynq processing system, now the AXI4lite interface is selected to connect the programmable logic portion of FPGA[16]. The clock and the reset signals being common to all the blocks.

V.EXPERIMENTAL RESULTS

Table 2 shows he experimental results of the comparison of the signal-to-noise ratio of standard windows such as hann and hamming window with alpha values varying from 0.5 to 0.9 for CAT window. The SNR value [15], increase at the rate of 3.4% with the increase in alpha value indicating the improvement in the quality of the signal. By applying the standard window functions along with the proposed CAT window function [20] with variable alpha value the frequency response curve is shown from fig 6. The curve has maximum energy concentration in the main lobe as the curve becomes narrower the more energy is conserved. The desired cut off frequency is at 50Hz. Observing from the graph the standard window gives cut-off nearing 60hz for hanning and hamming window. Whereas the cut off value of frequency for CAT windows is at 46 to 49 from alpha values ranging from 0.5 to 0.9.

The CAT window designed to be reconfigurable shows the following advantages from fig 7 to 11. To understand the curve the variable assignments are α1 = hanning, α2 = hamming, α3 = 0.5 for CAT window, α4 = 0.6 for CAT window, α5 = 0.7 for CAT window, α6 = 0.8 for CAT window, α7 = 0.9 for CAT window.

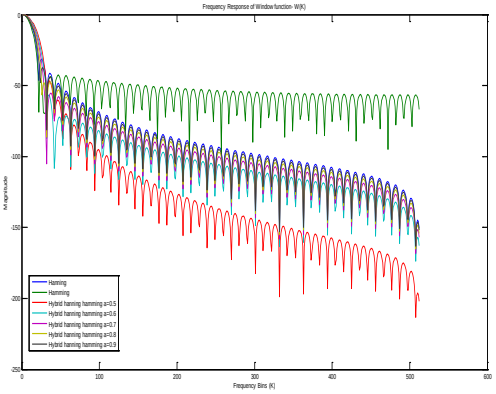


Fig 6: Window functions for CAT window.

The figure 7 shows that, the maximum side lobes are at α1, α2 & α7. For signal filtering which requires less noise value in the side lobes the best suitable α value is from 3 to 6.

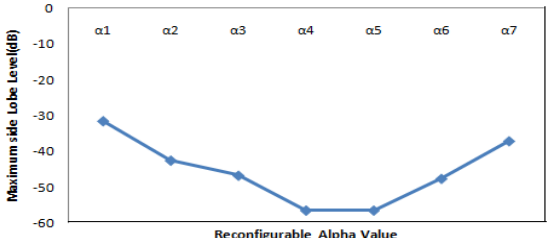


Fig 7:Maximum side lobe level(dB) for α1 to α7.

Figure 8 gives the best values of α suited to adapted for maximum roll off, of noise signals with best suited α values from 2.

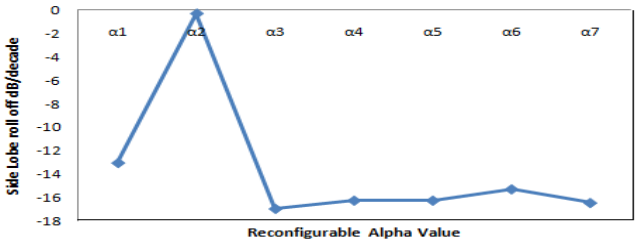


Fig 8: Side lobe roll off dB/decade(dB) for α1 to α7.

Figure 9 depicts that the maximum noise bandwidth decreases from α3 to α7.

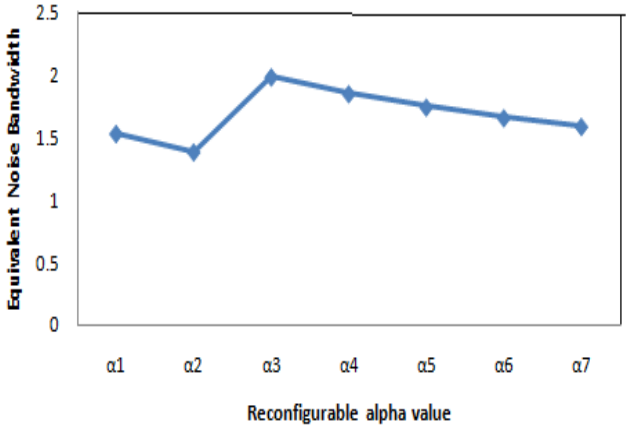


Fig 9: Equivalent noise bandwidth(dB) for α1 to α7.

To avoid signals which do not desire the first noise side lobe the desirable value of α is 1 and 7 shown in fig 10.

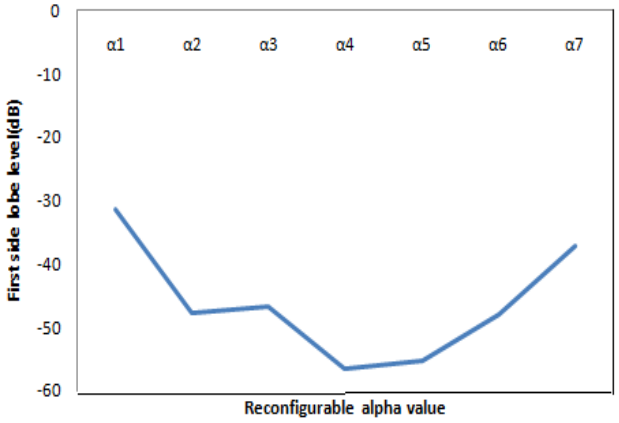


Fig 10: First side lobe level(dB) for α1 to α7.

Fig11: Normalized half main lobe width(dB) for α1 to α7.

For signals deserving maximum energy the desirable value of α is 5 to 6 from fig 11. The device used in the experiment is the ZC702 Zynq [16], all purpose platform. This board is a solution for connecting hard processor core with a dedicated silicon area mounted on the board along with the softcore programmable logic core on FPGA [17]. The purpose of this setup is that, the hardcore processor is stringent in adapting to new changes in the application, nor it allows adding a new processor core to FPGA for providing more processing capabilities. The main advantage of a soft core processor is, its implemented in the programmable logic portion of FPGA. The entire design setup is a developed flexible heterogenous multicore processor for CAT window. The clock, reset inputs are synchronous to the blocks. The device is controlled by the FPGA clock running at 100Mhz.

Table3: Utilization summary of Multi processor Vs Softcore processor.

Type of the core	Softcore Processor(FPGA)	Multicore_Processor (ARM with FPGA)
LUT	1110	671
Slice Registers	987	796
BoundedIO pads	164	130
No.of DSP blocks	1	1

Table3 shows experimental results of the CAT separately running only on FPGA and Parallelly running on the developed multicore processor. LUT (loot up tables) utilized by the multicore processor is reduced by 39.5%.

Hence when any kind of applications is ported on the enveloped multicore processor structure sharing of hardware resources is done between hardcore and softcore processor. This process reduces the burden on the single processor. This platform is best suited for task sharing. Also it shows slice registers are 19.3% less than softcore processor. Bounded input and output pad are reduced by 20.7% compared to softcore processor. From source to destination the clock signal shows that they are timed and false. This clearly indicates the clocks operate without any false paths or partial false paths.

By implementing the CAT window in the heterogenous multicore the area report from fig16 and table 4 shows that very minimal area of the multicore is utilized for the implementation purpose. Also the left over area can be utilized to form different designs. Approximately only 2% of the LUT's is being utilized for design implementation. Hence performance of any complicated designs can be easily carried out in FPGA with no restriction on the area utilization.

Table4: Hardware resource utilization of CAT window on Zynq

Resources	Available	Utilized
LUT	53200	671
Slice Registers	106400	796
Bounded IO pads	130	130
Buffers	32	1
DSP Blocks	220	1

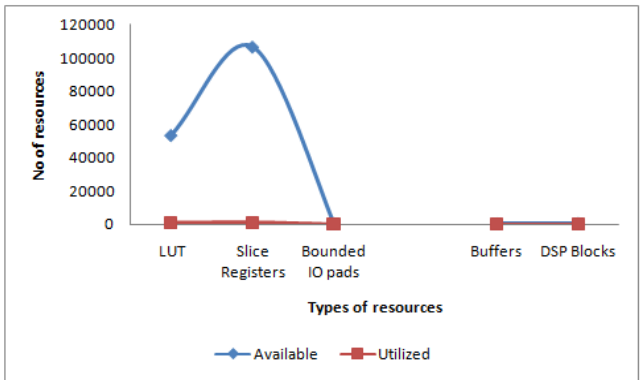


Fig12: Area report

The ARM processor the soft core are connected using AXI lite 32 bit bus and a minimum of 4 registers are used to reserved both as source and destination[18].

Table5: Core wise hardware utilization area report

Resources	Core1(ARM Processor)	Core2(FPGA)
LUT	452	56
Slice Registers	607	137
Bounded IO pads	96	34
Buffers	1	0
DSP Blocks	1	0

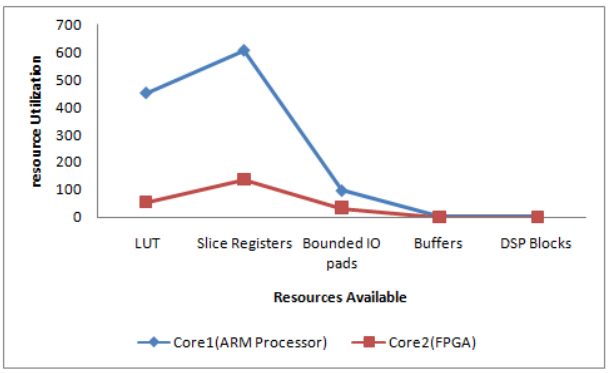


Fig13: Comparative graph of core wise hardware utilization area report.

Table 5 and fig 12 clearly indicates that the hardcore utilizes more percentage of the hardware resources like LUT's, slice registers and BIO(Bounded input output) pads.

The total dynamic power consumed by the design comes to 91% and 9% of the power is the device static power. This shows that only when the inputs change the power consumed is maximum and only a small amount of 9% power is consumed in static condition. The total power consumed in dynamic condition is 1.542W and the device static power is 0.158W. This clearly indicates that when the inputs change the power is consumed and the system goes to sleep mode in static conditions to save power.

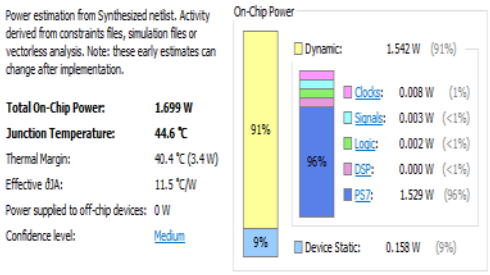


Fig 14 :Power reports

IV.CONCLUSION.

Implementing the CAT window on the heterogenous multicore processor, the various advantages achieved are, dynamically the α value can be reconfigured the get the maximum benefits of signal filtering properties which include maximum reduced side lobe width, maximum energy concentrated signals and faster noise factor fall off ration. Upon implementing the design in developed heterogeneous multicore processor, there is fast reduction in the static and dynamic power consumption as well as the flexibility of adding new designs in the soft core processor.

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