Design of 3.1-10.6 GHz CMOS UWB LNA Using Current Reuse Technique

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Abstract— A wideband Low Noise Amplifier (LNA) for Ultra-Wide Band (UWB) applications based on current reuse technique is proposed. The noise from the matching device is greatly suppressed over the desired UWB band by using the proposed circuit and design methodology. The wideband input matching is achieved by the combination of degenerative parallel LC circuit and resistive feedback in shunt-shunt connection. The cascaded LC technique is used to achieve the output matching. Simulated in 90 nm BSIM3 CMOS process, the LNA achieves peak power gain (S_{21}) of 18.621 dB at 4 GHz and high-flat gain of 18.0 \pm 0.5 dB in 3.1 to 10.6 GHz frequency range. The flat-low noise figure of 2.6 \pm 0.2 dB is attained in UWB frequency of interest. The input return loss (S₁₁) is less than -13 dB at 8 GHz and less than -10 dB in (5-11) GHz. The output return loss (S_{22}) is less than -6 dB in the band of interest. The reverse isolation (S_{12}) is lower than -25 dB. The IIP3 is obtained as -7 dBm. The Gain ripple of 1.57 dB is achieved through the entire band. The proposed LNA draws 11 mW power from 1.0 V supply.

Keywords— Cascaded LC technique, Current reuse, Low Noise Amplifier (LNA), Resistive feedback, Ultra-Wideband (UWB).

I. INTRODUCTION

FICs design makes use of CMOS technology and is Reference with its cost the second se management and integrating on Silicon on Chip (SoC) design. For Ultra-Wideband (UWB) applications, the frequency spectrum lies between 3.1GHz to 10.6 GHz which is declared by Federal Communications Commission (FCC). UWB systems include wireless sensor networks, medical imaging along with monitoring devices and ground penetrating radars. The integral part of the Radio Frequency (RF) receiver front-end block is the Low Noise Amplifier (LNA). It has a considerable significance as it gets the poor radio signals from the entire UWB range of frequencies and strengthen them with a good SNR. Of late, various UWB LNAs such as Common Source (CS), Common Gate (CG), cascade, cascode etc., have been represented [1]-[18]. For low dc power (P_{DC}) consumption and broad gain, Current Reuse (CR) technique is preferred [7], [9]-[12], [18], [19]. Broad band input matching which is a desired requirement is achieved in dual RLC branch [6], [16], which also performs low Noise Figure (NF).

To limit output matching and wideband, cascode [1], [3], [13], [14] and cascade [15] techniques are preferred. CG presented in [17] and CG-CR are preferred for low P_{DC} [8]. Narendra Nath Ghosh *et al.*, [18] presented differential LNA for radio applications between 0.2-3.2 GHz band.

Wei-Wei Chen *et al.*, [19] proposed CR negative shunt feedback method to provide additional design freedom to lower the P_{DC} of the trans-conductance (g_m) -boost CG LNA. However, some drawbacks are present among these UWB LNAs, for example, conventional distributed LNAs suffer from high P_{DC} . Wideband of LNA circuitry is achieved by adopting Resistive Feedback (RFB) at the cost of moderate gain and noise requirements. The noise performance of low power shunt-feedback LNA, degrades due to the low intrinsic g_m of MOS transistors. The LNAs with the above mentioned frequency range is expected to have better gain, less input return loss, favourable linearity and impedance matching at the circuit output [4]. Besides, an acceptable linearity of LNA is required in UWB RF systems to preserve the state of the pulse [5].

The UWB LNAs with CR technology are thoroughly examined due to their less P_{DC} , flat and high power gain, enhanced SNR, good reverse isolation and satisfactory output impedance matching [6]. In this present work, the authors propose a design model for low power consumption, less noise and an amplifier operating in wideband is achieved by integrating a narrowband LNA along with the shunt-shunt resistive feedback of conventional type of degenerative parallel LC circuit. The UWB LNA circuit description along with its short analysis of gain and NF is presented in section II. Section III describes the Advanced Design System (ADS) simulation results. Section IV highlights the presented work is a nutshell as conclusion of the report.

II. CIRCUIT DESIGN OF WIDEBAND LNA

The typical narrowband LNA in cascode topology is shown in Fig. 1(a). In Fig. 1(a), source inductor (L_s) is used to minimize the noise and the impedance matching between input of LNA and source resistance (R_s) is accomplished by the gate inductor (L_G) [2]. The Fig. 1(b) shows the small signal equivalent model for the input stage of the overall LNA presented. The input transistor M_1 has gate to source capacitance, C_{gs} . The reactive elements are combined in series shown in Fig. 1(b) to resonate at the frequencies of interest such that a real value with $\omega_T L_s$ being equal to R_s . The transistor M_1 has a cut-off frequency ω_T . The series resonating input circuit quality factor's mathematical expression is shown in equation (1) [21].

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$$Q_{NB} = \frac{1}{(R_s + \omega_T L_S).\omega_0.C_{gs}} \tag{1}$$

Where ω_0 defines the resonant frequency. The quality factor as in equation (1) is required to be more for large gain with low noise figure and less P_{DC}. The 3 dB bandwidth of an ideal series RLC circuit is inversely proportional to its Q-factor (BW-3 dB = ω_0/Q_{NB}) which is unacceptable for wideband applications, shown in Fig. 1(a).



Fig. 1 LNA topology for narrowband. (a) Circuit schematic (b) Input stage small-signal equivalent model.

Fig. 2 represents the wideband LNA that is designed in this paper. The shunt feedback resistor R_{FB} is used at the output of first stage [6] and shunt inductor (peaking) L_{D2} is used at the output [20]. The cascode configuration with CR is adopted for designing a two stage CS-LNA. The broadband input matching is the main benefit by using resistive-shunt feedback and the LC parallel load provides the input network equivalent to two branches in parallel, which means a second order band-pass filter for wideband applications. The bandwidth extension is achieved by using series inductive and shunt peaking technique. The cascode architecture provides low NF and flat high power gain. The power dissipation is the major drawback in cascode topology which is addressed by use of CR technique in the present UWB LNA design.



Fig. 2 Proposed UWB LNA

The designed architecture with current reuse technique is used to resolve various issues such as small gain, reverse isolation and excessive power consumption. The technique stands on reducing the driving current sources by using dc current between output to input stage. The various architectures with CR technique are available as in [9]-[12].

RFB technique is used in the first stage of CS, which provides better input matching and low noise by tuning L_{S1} , L_{G1} , and parameters of the M_1 transistor, which are shown in equations (2), (3) & (4).

$$S_{11} = \frac{Z_{in} - R_s}{Z_{in} + R_s}$$
(2)

Where
$$(Z_{in} = \left(\frac{(L_{G1} + L_{S1})R_{FB}}{L_{D1}g_{m1}}\right) + S\frac{(L_{G1} + L_{S1})}{g_{m1}} + \frac{1}{S}\left(\frac{(L_{G1} + L_{S1})}{g_{m1}L_{D1}C_{1}} + \frac{1}{g_{m1}C_{gs1}} + \frac{L_{s1}R_{FB}}{C_{gs1}L_{D1}}\right)$$

(3)
 $F \approx 1 + \frac{R_{FB}\left(\gamma g_{m1} + \frac{1}{R_{LD1}} + \frac{SL_{D1}}{R_{FB}}\right)}{SL_{D1}g_{m1}^{2}(R_{FB} + S^{2} + L_{D1}^{2})} \cdot \frac{1}{\left(\frac{1}{R_{S}} + \frac{1}{R_{FB}} + \frac{1}{R_{LG1}} + \frac{1}{R_{LS1}}\right)Z_{in}^{2}}$

(4)

Where R_{LD1} , R_{LG1} and R_{LS1} are resistance of drain, gate, and source inductances and γ is the coefficient of thermal noise.

The second stage of CS LNA improves gain flatness, amplifies the first stage signal with appropriate impedance matching at output terminal by tuning circuit parameters of second stage such as L_{D2} , R_{D2} , L_{G2} and transistor parameters of M₂. Cascaded LC (L_{OUT} and C_{OUT}) output network provides good output matching. The gain expression for the proposed UWB LNA is represented in equation (5).

An ac-coupling path for the transistors M_1 and M_2 is accomplished by the capacitors (C_1 and C_2). The capacitor C_3 is connected to the source side of M_2 which helps ac current flowing to the ground path and hence to avoid interference coupling back to M_1 [6]. PTM 90 nm BSIM3 model [22] is used to design the UWB LNA.

$$A_{\nu} = g_{m1}g_{m2} \cdot \frac{SL_{D1}(SL_{D2}+R_{D2})}{S^2 c_{gs2}L_{G2} + \left(\frac{c_{gs2}}{c_2} + \frac{c_{gs2}}{c_0}\right)}$$
(5)

III. RESULTS DISCUSSION

The small-signal *S*-parameters analysis in the UWB-band is discussed in this section. The BSIM3 90 nm model parameters are imported into ADS environment and simulated for the proposed LNA. The simulated gain and NF of the proposed LNA are shown in Fig. 3. The reverse isolation and input-output reflection coefficients are presented in Fig. 4.



Fig. 3 Gain and Noise Figure of the proposed LNA





The maximum gain for the LNA is obtained as 18.62 dB at 4 GHz and minimum gain as 16.84 at 10 GHz. The maximum variation 1.77 dB is reported in the entire UWB band. The maximum NF is 2.71 dB at 3 GHz and 2.59 dB of minimum NF is at 9.5 GHz. The difference is 0.12 dB in the total UWB frequency range. S₁₁ is less than -13 dB at 8 GHz and less than -10 dB in the frequency band of (5-11) GHz. S₂₂ is less than -2.89 dB between 3 GHz to 5 GHz. S₂₂ is lower than -3.89 dB between 5.1 GHz to 7 GHz and below -5.07 dB for (7.1-10) GHz. The reverse isolation (S_{12}) is less than -25 dB in the entire UWB band. Stability factor is one of the parameter used to evaluate the amplifier performance. The amplifier should be unconditionally stable means at any possible impedance the circuit should be stable [18]. The stability factor of the LNA circuit is as shown in Fig. 5. Clearly, the LNA was unconditionally stable over the UWB band of interest.

In an amplifier design, flatness is highly desired and it can be achieved by controlling the ripple. The less difference between maximum and minimum of the amplitude will provide more flat band. Fig. 6 gives the gain ripple of the proposed LNA. The Gain ripple is 1.57 dB between 3.1 GHz to 10.6 GHz. Figure of Merit (FoM) is a decisive parameter to reveal the overall performance of the LNAs. FoM considers gain, 3 dB bandwidth, NF_{min} and P_{DC} of the LNA defined in equation (6) [11]. The FoM of proposed LNA is 18.

$$FoM = \frac{Gain \ X \ BW_{3-dB} \ [GHz]}{(F-1)X \ P_{DC} \ [mW]}$$
(6)



Fig. 5 Stability Factor K of the of the proposed LNA



Fig. 6 Gain ripple of the proposed LNA

Fig. 7 and Fig. 8 show the 1-dB compression point (P1dB) of -22 dBm and the third-order intercept point (IIP3) of -7 dBm respectively.



Fig. 7 P1dB of proposed UWB LNA



Fig. 8 IIP3 of proposed UWB LNA

The implemented CMOS UWB LNA and state of the art UWB LNA's reported recently are summarized in Table I. The standard 90 nm CMOS process is adopted by considering BSIM3 of PTM model. The proposed LNA exhibits high and flat, better linearity and low NF when compared to previously published LNAs. The simulation results indicate that the gain is improved by a factor of 15.36 %, noise figure is improved by a factor of 24.72%.

IV. CONCLUSION

The two stage CS LNA based on the current-reuse cascode configuration is designed by considering 90 nm CMOS process. The present paper is focused on low power, high-flat gain, low NF and good input-output matching with better linearity. The high-flat gain and less power are

achieved by taking the advantages of CR technique. Controlling the resistive feedback and input LC network at M_1 transistor, degraded NF and input matching of 50 Ohm are obtained. Good output matching is accomplished by adding cascaded LC (L_{OUT} and C_{OUT}) output network and controlling R_{D2} , and L_{D2} at M_2 transistor. The proposed LNA achieves a gain of 18.621 dB. The input return loss, S_{11} is less than -10 dB and S_{22} is below -6 dB in frequency band of interest. NF is less than 2.71 dB in the frequency range of

3.1 GHz to 10.6 GHz with excellent linearity, stability and FoM. The results show that the proposed LNA is applicable for high gain, low power UWB wireless sensor network applications.

Parameters	[7]	[9]	[10]	[16]	This Work
Technology	90 nm	130 nm	180 nm	130 nm	90 nm
BW (GHz)	2.6-10.2	3.1-4.8	3-11	3-12	3.1-10.6
V _{dd} (V)	1.20	1	1.20	1.20	1
Gain (dB)	12.50	13	15.76	13.50	18.62
NF _{min} (dB)	3-7	3.50	3.38	4.30	2.71
S ₁₁ (dB)	-9	<-8	<-10.60	< -11.00	< -10
S ₁₂ (dB)	-45	<-40			<-25
P1dB (dBm)	-12	-15.40			-22
IIP3 (dBm)		-6.10		-7.00	-7
P _{DC} (mW)	7.20	3.40	8.65	8.50	11
FoM			33.90	3.41	18

Table L Comparison chart of the various LNAS for UWB App	plications
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REFERENCES

- Bevilacqua and A. M. Niknejad, "An Ultrawideband CMOS lownoise amplifier for 3.1–10.6-GHz wireless receivers," *IEEE J. Solid State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.
- [2] Trung-Kien Nguyen, Nam-Jin Oh, Hyung-Chul Choi, Kuk-Ju Ihm, and Sang-Gug Lee, "CMOS low noise amplifier design optimization techniques," *IEEE Trans. on Microwave Theory and Techniques*, vol. 52, no. 5, pp. 1433–1442, May 2004.
- [3] Chang-Wan Kim, Min-Suk Kang, Phan Tuan Anh, Hoon-Tae Kim, and Sang-Gug Lee, "An Ultra-Wideband CMOS low noise amplifier for 3–5-GHz UWB system," *IEEE J. of Solid-State Circuits*, vol. 40, no. 2, pp. 544-547, Feb. 2005.
- [4] Chang-Zhi Chen, Jen-How Lee, Chi-Chen Chen, and Yo-Sheng Lin, "An excellent phase-linearity 3.1-10.6 GHz CMOS UWB LNA using standard 0.18 µm CMOS technology," in *Proc. of Asia-Pacific Microwave Conference*, 2007, pp. 1-4.
- Yi-Ting Chiu, Yo-Sheng Lin, and Jin-Fa Chang, "A 18.85 mW 20-29 GHz wideband CMOS LNA with 3.85±0.25 dB NF and 18.1±1.9 dB gain," in *IEEE MTTS International Microwave Symposium*, 2010, pp.381-384.
- [6] Yo-Sheng Lin et al., "Analysis and design of a CMOS UWB LNA with dual-branch wideband input matching network," *IEEE Tran. On Microwave Theory and Techniques*, vol. 58, no. 2, pp. 287-296, Feb. 2010.
- [7] Giuseppina Sapone and Giuseppe Palmisano, "A 3–10 GHz low-power CMOS low-noise amplifier for Ultra-Wideband communication," *IEEE Trans. on Microwave Theory and Techniques*, vol. 59, no. 3, pp.678-686, 2011.
- [8] Alireza Dehqan, Ehsan Kargaran, Khalil Mafinezhad, and Hooman Nabovati, "An ultra-low voltage ultra-low power CMOS UWB LNA using forward body biasing," in *IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012, pp 266-269.
- [9] Muhammad Khurram and S. M. Rezaul Hasan, "A 3–5 GHz Current-Reuse g_m-boosted CG LNA for ltrawideband in 130 nm CMOS," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 3, pp. 400-408, Mar. 2012.
- [10] A. N. Ragheb, G. A. Fahmy, I. Ashour, and A. Ammar, "A 3.1-10.6 GHz low power high gain UWB LNA using current reuse

technique," in 2012 4th International Conference on Intelligent and Advanced Systems (ICIAS2012), vol. 2, 2012, pp. 741-744.

- [11] Meng-Ting Hsu, Yu-Hua Lin, and Jing-Cheng Yang, "Design of UWB CMOS LNA based on current-reused topology and forward body-bias for high figure of merit," in *Proceedings of Asia-Pacific Microwave Conference*, 2013, pp. 772-774.
- [12] K. Yousef et al., "A 0.18 μm CMOS current reuse ultra-wideband low noise amplifier (UWB-LNA) with minimized group delay variations," in proc. of the 9th European Microwave Integrated Circuits Conference, 2014, pp. 1392-1395.
- [13] Meng-Ting Hsu, Jing-Cheng Yang, and Jyun-Ren Jhan, "Design of UWB LNA using RC feedback technology," in proc. of Asia-Pecific Microwave Conference, 2014, pp. 1169-1171.
- [14] Jihai Duan et al., "Design of an incoherent IR-UWB receiver frontend in 180-nm CMOS technology," in *IEEE Sixteenth International* Symposium on Quality Electronic Design, 2015, pp. 186-190.
- [15] A. Slimane et al., "A 0.6 V, 2.1 mW CMOS UWB LNA for 3-5 GHz Wireless Receivers," in IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Oct. 2016, pp. 1-4.
- [16] Nan Li, Weiwei Feng, and Xiuping Li, "A CMOS 3–12-GHz ultrawideband low noise amplifier by dual-resonance network," *IEEE Microwave and Wireless Components Letters*, vol. 27, no 4. pp. 383-385, 2017.
- [17] Ahmed M. Saied, Mostafa M. Abutaleb, Ibrahim I. Ibrahim, and Hani Ragai, "Ultra-low-power design methodology for UWB lownoise amplifiers," in *IEEE 29th International Conference on Microelectronics (ICM)*, 2017, pp. 1-3.
- [18] Narendra Nath Ghosh, Prakash Kumar Lenka, SriHarsa Vardan G, and Ashudeb Dutta, "A 0.6 mW 1.6 dB noise figure inductorless shunt feedback wideband LNA with G_m enhancement and current reuse in 65 nm CMOS," in *IEEE 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID)*, Jan. 2018, pp. 335-340.
- [19] Wei-Wei Chen, Shang-De Yang, and Kuang-Wei Cheng, "A 1.2 V 490 μW sub-GHz UWB CMOS LNA with current reuse negative feedback," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1-4.
- [20] Sunderarajan S. Mohan, Maria del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee, "Bandwidth extension in CMOS with optimize on-chip inductors," *IEEE J. of Solid-State Circuits*, vol. 35, no. 3, pp. 346-354, Mar. 2000.

- [21] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 1998.
 [22] Predictive Technology Model, Latest Models. [Online]. Available: http://ptm.asu.edu/modelcard/90nm_bulk.txt.