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22nm FINFET Based High Gain Wide Band Differential Amplifier

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Abstract- Differential Amplifier is a primary building block of analog and mixed signal circuit for pre-processing and signal conditioning of analog signal. FINFET devices with high-k gate oxide at 22nm technology are predominantly used for high speed and low power complex VLSI circuits. FINFET based differential amplifiers are widely used in ADC's and signal Processing applications due to their advantages in terms of power dissipation. Analog front end of complex VLSI circuits need to offer high gain, higher stability and low noise figure. Designing of FINFET based VLSI sub-circuits requires proper design procedure that can provide designers flexibility in controlling the circuit performances. In this paper, differential amplifier is designed using model parameters of high-k FINFET in 22nm technology. The conventional procedures for designing MOSFET based differential amplifier are modified for designing FINFET based differential amplifier. Schematic capture is carried out in Cadence environment and simulations are obtained considering 22nm FINFET PDK. The performance metrics are evaluated and optimized considering multiple iterations. The designed differential amplifier has slew rate of 6V/µSec and settling time of 0.9 µSec which is a desired metric for ADCs. Power Supply Rejection Ratio (PSRR) is 83 dB and dynamic range is 1.6754 V. Open loop DC gain of DA is achieved to be 103 dB with phase margin of 63^0 that demonstrates the advantages of DA designed in this work suitable for analog front end.

Key Words – FINFET, Differential Amplifier (DA), CMRR, PSRR, High Gain, Wide Band

I. Introduction

Differential Amplifier (DA) is a fundamental building block of complex analog circuits. The DA circuits processes the input signal and amplifies the signal with high gain minimizing noise at the output. The operational amplifier module has the DA in the front end for this purpose. CMOS circuits have been predominantly used in design of complex analog circuits and in the last few years new devices such as FINFETs are used in place of MOS transistors. In the year 1987 Balestra et al. [1] proposed the Double Gate MOSFET (DG-MOSFET) that had advantages over MOSFET in terms of increased current and reduced short-channel effects. Using vertical silicon layer called as FIN with two lateral gates gave rise to one of the best transistor structures. FINFET based amplifier performs better when compared with MOSFET based amplifiers. Further to this another gate at the top resulted in trigate transistors with two lateral channels. It is also required to design circuits using FINFETs and hence it is required to understand the voltage and current relationship in FINFETs. There are two types of operational amplifiers such as two stage and folded cascode amplifiers. The two-stage amplifier comprises of differential amplifier and source follower or second stage amplifier circuit. For design of high gain operational amplifier with wide band width support the differential amplifier (DA) need to be designed appropriately setting standard design procedures for the transistor geometries. Design MOSFET based DA are based on well-known conventional methods, it is required to design DA based on FINFETs. In this paper, a detailed discussion on design of DA is presented considering FINFET VI characteristics. FINFET is one of the recent technologies used for low voltage analog and digital applications. Different features of FINFET created single stage Differential amplifier compared with Conventional CMOS Single-stage Differential amplifier. FINFET circuit offers best performance than the MOSFET and CNFET at the cost of power consumption. The low leakage, low power dissipation and high current driving capabilities of the FINFET are the basic building blocks of Differential amplifier. From the recent studies of Differential amplifier design using FINFET, Amir Baghi Rahin et al. [2] proposed a double gate transistor with independent gate using FINFET and simulated the same using a supply voltage of 1V. In the design a compensation capacitor of value 2.2PF was used. Vikhe et al. [3] in their work designed differential amplifier using FINFET and evaluated its performances. Power consumption of 58µW was observed in their work on FINFET based DA at 1 V power supply. DC gain of 52 dB with unity gain frequency of 6.4MHz and phase margin of 71° were obtained. The DA circuit designed is having limited operating frequency for high speed applications. S. Hsieh et al. [4] discuss design of 12-bit SAR ADC using adaptive time domain comparator and, they incorporated noise optimization method. The DA circuit designed has gain of less than 50 dB. Y. Chen et al. [5] designed a 9-bit, 1.46mW SAR ADC using 65nm technology. They used differential amplifier in their design to achieve an amplified output at the output stage. M. Yoshika et al. [6] proposed a 10-bit, 820µW SAR ADC with on-chip digital calibration method, the high power dissipation in the ADC is

contributed by power dissipation in DA circuit. H. Choi et al. [7] in their work used mid-code calibration technique for SHA based free dual channel nyquist ADC. DA circuit in their work is found to operate in MHz frequency range and is limited for high speed ADCs. Tai-ji et al. [8] designed a CMOS SAR ADC using asynchronous pipelined architecture and achieved a high-power dissipation 3.5 mW using 1.0 V supply voltage. DNL and INL achieved are 0.71 LSB and 0.70 LSB, respectively. Murmann [9] worked on transistor scaling and ADC architecture design using different sub circuits. Most of the DA circuits have been designed to achieve high gain but have limited operating frequency of less than 60 MHz. FINFET based DA circuit have demonstrated higher operating frequencies in ADC circuit design [10] and discussions on transistor scaling and its limitations are presented in [11]. Next section discusses the concept of FINFET and design procedure for DA circuit using FINFETs.

II. FINFET

Chenming HU, Tsu-Jae King-Liu and Jeffrey Bokor from University of California have developed the FINFET with Double Gate (DG) [13] to control the flow of current in the channel. The gate to channel coupling is improved due to double gates and with control mechanism on both sized channel size is reduced [13]. DG-FETs are operated at lower threshold voltages and reduce power dissipation [12]. Figure 1 shows the structure of FINFET with double gate (top and bottom) [14] placed on the insulator, the source and drain regions are conned through the channel. The circuit topology or the small signal model of the FINFET is shown in Figure 2. The intrinsic circuit comprises of parasitic capacitances C_{gd}, C_{gs} and C_{ds} along with the parasitic resistance R_{gd}, R_{gs}, R_{ds} and R_{sub}. The capacitances C_{pg} and C_{pd} are considered at low frequencies with pinch-off condition. The parameters Lg, Rg, Rs and Rd are computed considering Vgs above pinch-off.

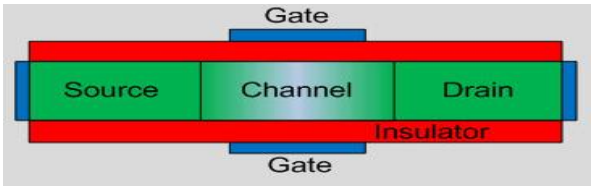

Fig. 1- Structure of FINFET (Double gate) [15]

The small signal model and model file of FINFET considered from Predictive Technology Model (PTM) is considered for design of ADC. The device parameters are presented in Table 1. The source doping and drain doping concentration based on Gaussian doping is considered at 1e+19/cm^{-3}, the dielectric constant of channel is 11.7 and the dielectric constant of insulator is 3.9.

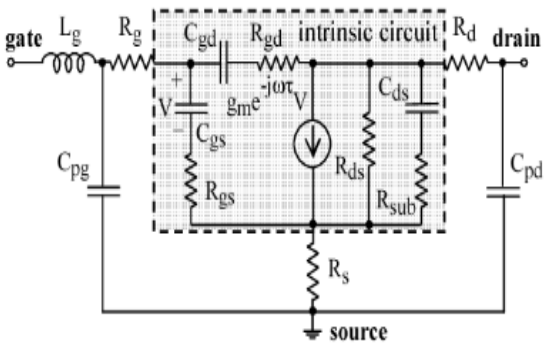

Fig. 2- Small signal equivalent circuit for FINFET [16]

The bandgap and affinity of channel material is considered at 1.12 eV and 4.05 eV with gate contact work function of 4.6 eV. Mobility of electrons and saturation velocity is considered at 1400 cm^2/Vs and 1.07e+07 cm/s. Considering these structural and electrical properties for FINFET the device model is simulated for its input and output characteristics.

Table 1- FINFET Device Parameters

Parameter	**Value (This Work)**	**Value [12]**
Channel length	22 nm	32 nm
Oxide thickness 1	2.5 nm	1.6 nm
Oxide thickness 2	2.5 nm	1.6 nm
Gate length	22 nm	-
Source/drain extension length	50 nm	32 nm
Gate to source/drain overlap	2 nm	-
Work function	4.6 eV	4.5 eV
Source/Drain doping	1 x 10^{19}cm^{-3}	2 x 10^{20} cm^{-3}

Figure 3(a) and 3(b) presents the input and output characteristics for the FINFET considered with the structural parameters as in Table 1. The parameters chosen in this work is compared with the parameters that have been considered in [12]. The technology selected in this work is 22 nm. The input is obtained by setting the drain voltage at 0.5 V and 1V. The output characteristic is obtained by setting the gate voltage between 0 V to 1 V with incremental step so 0.1 V.

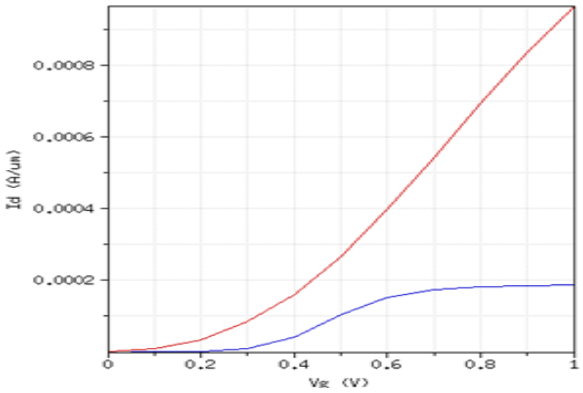

Fig 3(a)- Input Characteristics

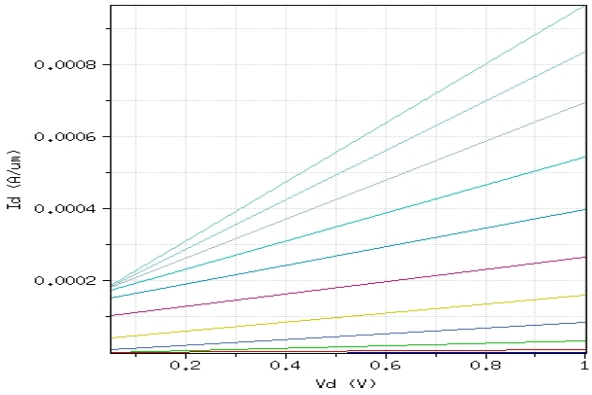

Fig 3(b)- Output characteristics

Figure 4(a) presents the power dissipation and transfer characteristics of inverter based on FINFET device. The maximum power dissipation is observed to be less than 800nW and transition width is less than 0.12 V.

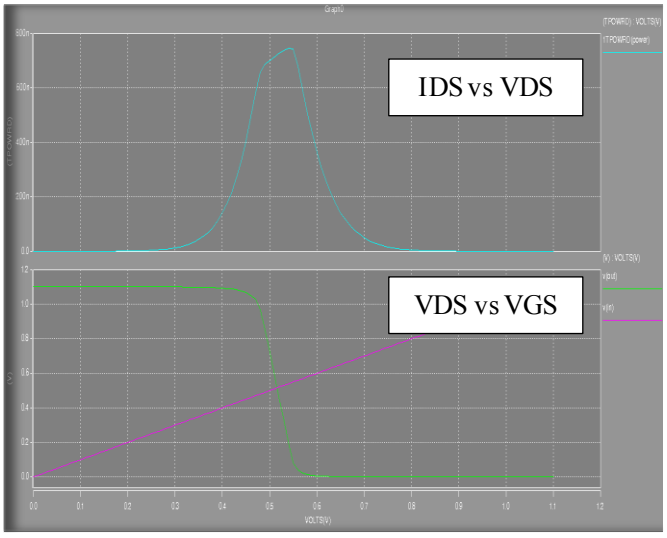

Fig. 4(a)- Power dissipation and transfer Characteristics of Inverter

Figure 4(b) presents the leakage current analysis for FINFET based inverter circuit. The leakage current during positive switching and negative switching current is observed to be less than 9µA.

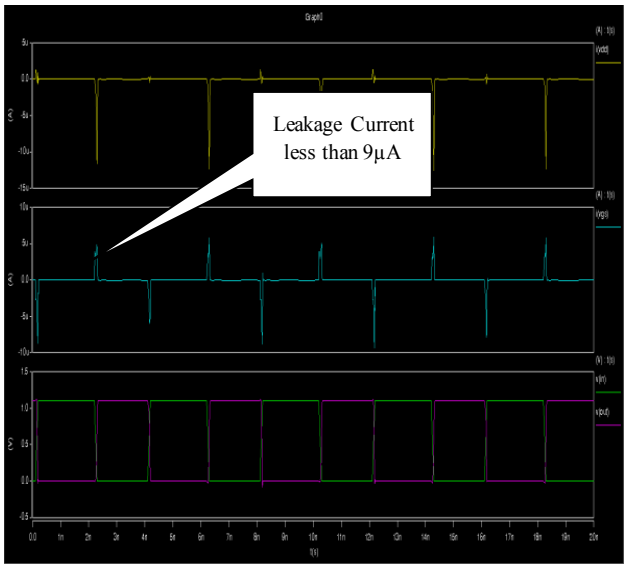

Fig 4(b)- Leakage Current analysis of Inverter characteristics for 22nm high-k FINFET

III. DIFFERENTIAL AMPLIFIER DESIGN

The Differential Amplifier (DA) at the input stage of the OPAMP achieves larger gain leading to improvement in noise performance and offset. Figure 5 presents the circuit schematic of differential amplifier using FINFET. The two gates of FINFET are shorted and are used as single gate transistor device. Transistors M1 and M2 are the common source amplifiers with P-channel FINFET (M3 and M4) used as current mirrors. Transistor M5 is the bias transistor that is required to set the maximum current that can flow in the two amplifiers. Transistor M8 is the N-channel FINFET current mirror used as current reference providing bias current for transistor M5. The load capacitance CL is set across which the output voltage is observed.

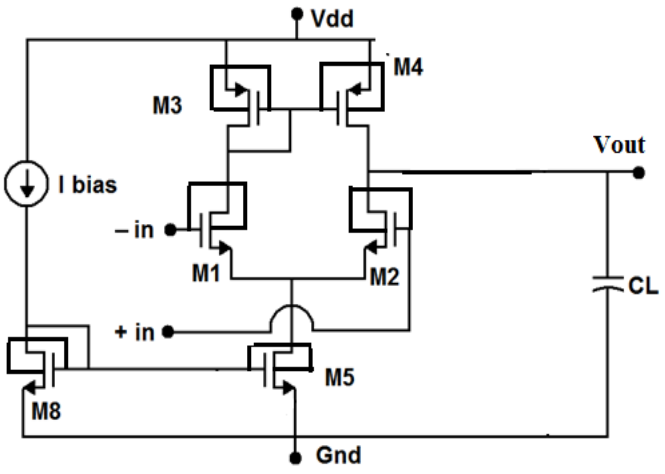

Fig. 5- FINFET based DA

In typical A/D converter applications, the DA which is also used as comparator must slew its output quickly and without oscillation once the input thresholds are crossed. The slew rate for the DA or comparator is measured by giving a step input

signal and measuring the time it takes for the DA to reach the final output value. The circuit schematic for the DA is captured in Cadence environment. The transistor geometries for the M1 and M2 are set to 100 nm and the transistor geometries for M3 and M4 are set to 200 nm, transistor geometries for M5 and M8 are set to 400 nm supporting maximum driving current of 100 µA.

IV. DESIGN OF DIFFERENTIAL AMPLIFIER TRANSISTOR GEOMETRIES

Table 2 presents the DA design specifications considered for the requirement of OPAMP design [11]. The slew rate is assumed to be greater than 6V/ µS and the power dissipation is set to be less than 50 µW as per the design specifications of high speed ADCs. The factors K'_p and K'_n are computed considering the mobility and parasitic capacitance parameters obtained from the model file.

Table 2- DA Design Specifications

Parameters	Value
Slew Rate = SR	> 6V/µS
V_{out} range	= ±2V
ICMR	= 0.15 to 0.8V
Phase margin	60^0 to 75^0
Open loop gain	>100 dB
Power Dissipation	≤ 50 µW
$V_{th} = \|V_{tp}\|$	= 0.25V to 0.45V
$K'_p = \mu_p C_{ox}/2$	= -455 µA/V²
$K'_n = \mu_n C_{ox}/2$	= 1085 µA/V²

Design procedure for MOSFET based DA is discussed in detail by Allen Hollberg [17]. In this work the design procedure is fine tuned to compute the transistor geometries of FINFETs for DA circuit schematic. Table 3 summarizes the design procedure for FINFET based DA Design.

Table 3-Transistor geometry

Transistor Number	W (MOSFET) nm	W (FINFET) nm
M1	200	100
M2	200	100
M3	1200	600
M4	1200	600
M5	800	400
M8	1600	800

Based on the identified transistor widths the schematic capture is modeled in Cadence and simulation results are obtained to identify the performances of DA amplifier.

V. RESULTS AND DISCUSSIONS

The performance parameters such as DC gain, open loop gain, output swing, CMRR, PSRR and transconductance are measured considering standard test models. The results obtained are discussed in detail for the DA circuits designed using FINFET. The DC gain of the DA is measured considering the test configuration shown in Figure 6 which provides provision for direct measurement of v_o/v_{in} at DC. A load capacitance of CL is included at the output side and the non-inverting input is swept with AC signal with V_{OS} (offset voltage) of 0.5 mV. Adjusting DC gain will help in improvising all other parameters. Variation in load capacitance impacts the wide band operation of DA circuit.

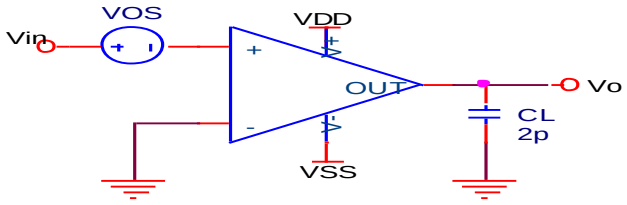

Figure 6- Configurations to find DC Gain

From the simulation results for measuring DC Gain as shown in Figure 7, the maximum gain is found to be 83 dB and the phase margin is 65^0 measured at 3 GHz operating frequency.

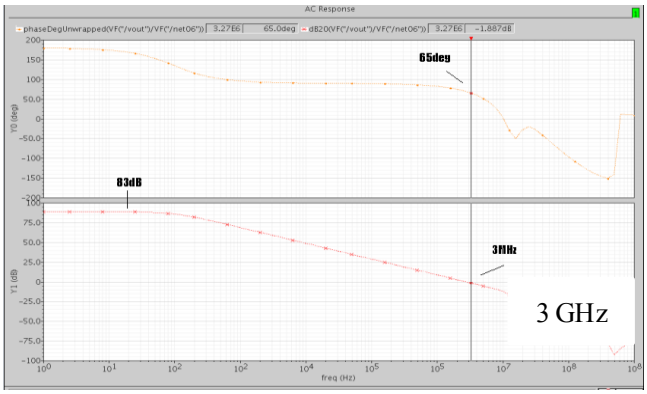

Figure 7-AC analysis of Differential Amplifier

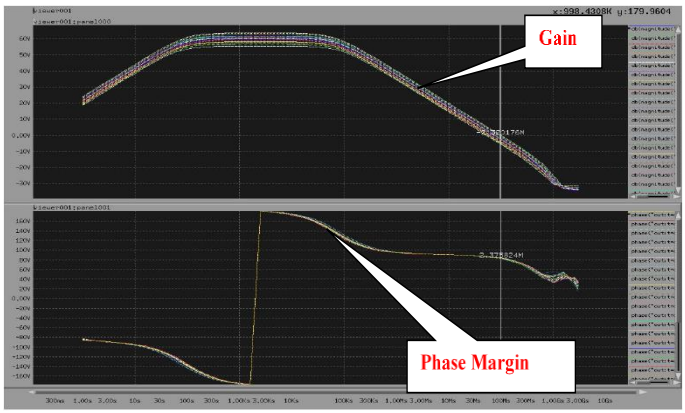

Fig. 8- Gain and phase-margin plots of DA with varying W_{eff}

The expected gain of Differential amplifier is around 100 to 120 dB. The achieved gain is around 107dB. The phase noise margin increases the stability of the Differential amplifier. The desired phase noise margin is around 55° to 75° and the achieved Phase noise margin is 63°.In order to measure the output voltage swing the test configuration in Figure 9 is considered. The input is applied at the inverting terminal with input resistance of 1 M Ohm and a feedback is introduced with resistance of 10 M Ohm. The inverting configuration is measured for its output voltage swing by setting the inputs to various voltage levels. The output is measured for its voltage swing and the test results are shown in Figure 10.

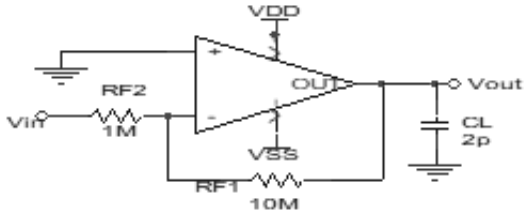

Figure 9- Configuration for the measurement of the output swing

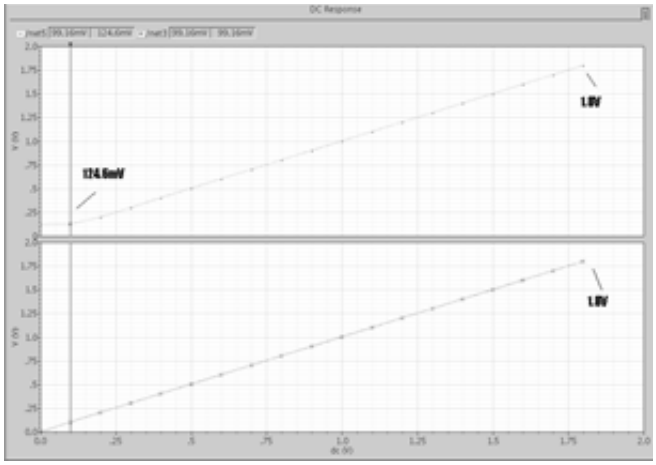

Figure 10- Output Swing of Differential Amplifier

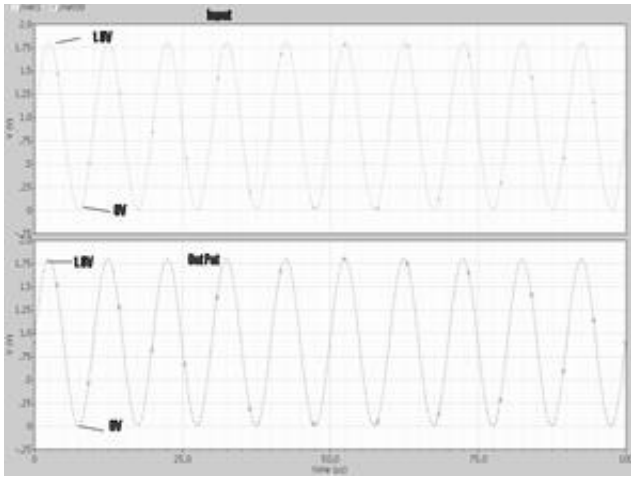

Figure 11- Rail to rail voltage swing considering sine wave input

Figure 11 presents the rail-to-rail voltage swing for a given sine wave input. The Vin is varied from 0 to 2 V and the output voltage swing is measured be between 124.6 mV to 1.8 V. The dynamic range of the designed differential amplifier is 1.6754 and the ratio of dynamic range is 83.77%. It is expected to be nearing 85%; the DA design achieves dynamic output voltage swing of 83.77%. Figure 12 shows the configuration used to find the DC open loop gain of the system and the DC gain is the important parameter in the design of DA circuit. The open loop gain results are presented in Figure 13 and the open loop DC gain is 103 dB which is higher than the desired requirement of 100 dB.

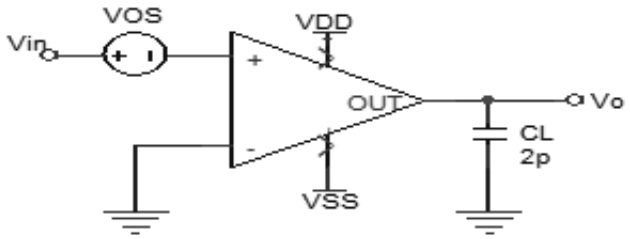

Figure 12-Configuration for DC open loop gain

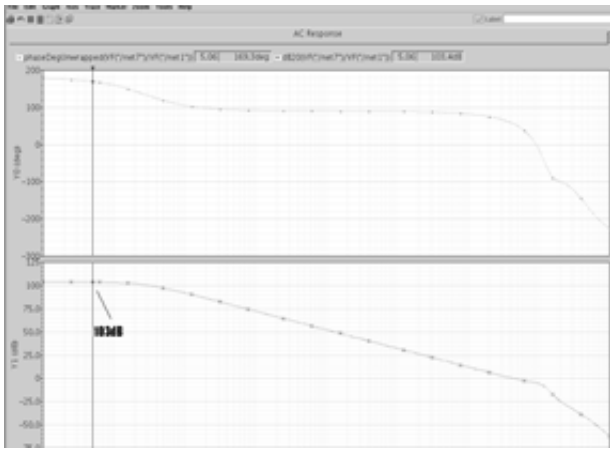

Figure 13-DC open loop gain

Common Mode Rejection Ratio (CMRR) is measured considering the circuit configuration shown in Figure 14. As CMRR was critical parameter, necessary steps are required to be considered in design of transistor geometries to ensure to meet the transistor matching criteria. In this work, transistor geometries are fine tuned to meet the CMRR requirements based on simulation results. The transistor geometries are varied by a factor of 8% as compared with theoretical calculations. Further it is required to consider transistor matching during layout design that will provide the actual CMRR computations after back annotations. Figure 15 is the simulation result of CMRR for the designed DA circuit.

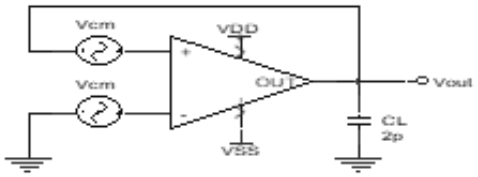

Figure 14- Configuration to measure CMRR

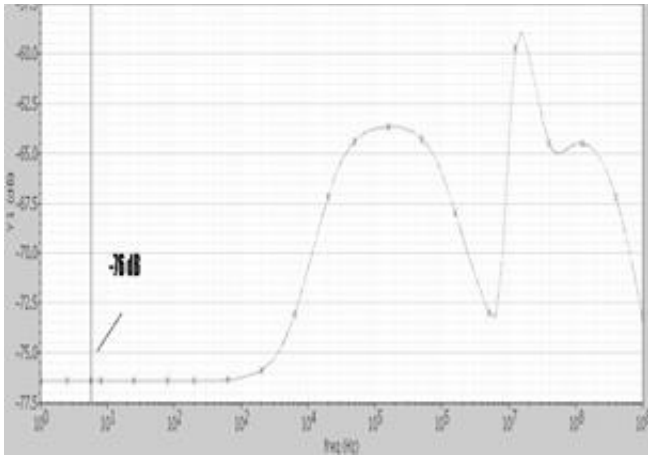

Figure 15- CMRR simulation results

The slew rate and settling time is measured for the DA circuit. The slew rate is found by connecting the DA in voltage follower configuration and input is set to a square wave. The slew rate is found to be 6V/µsec and settling time was 0.9 µsec as shown in Figure 16.

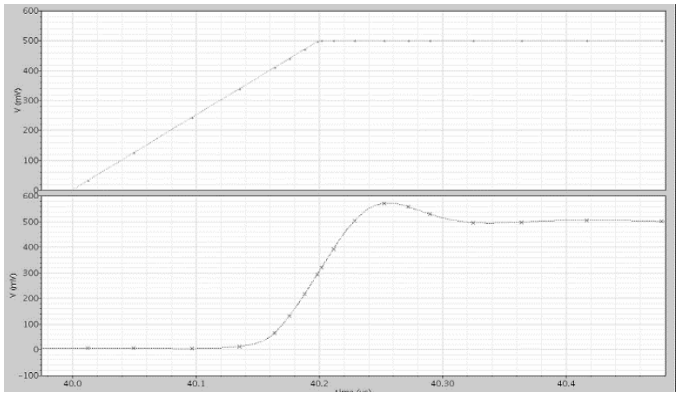

Figure 16-Slew rate results for DA

Power Supply Rejection Ratio (PSRR) is the capability for the DA to reject any noise being induced from the power supply. It is measured by connecting the DA as per the test configuration shown in Figure 17 and the corresponding simulation results are shown in Figure 18 from which the measured PSRR is 83 dB.

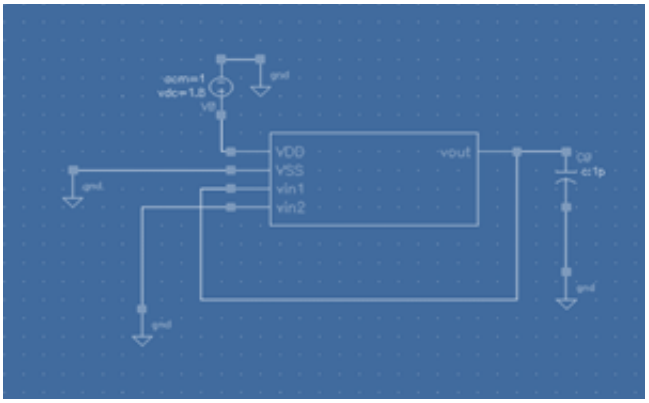

Figure 17- PSRR Configuration

Bin Wang et al. [18] have designed Asymmetric structure for power amplifiers and have discussed a thorough methodology for analysis. Sami Laifa et al. [19] have designed PID Controllers for MIMO Systems. For implementation of this module differential amplifier designed in this paper can be adopted.

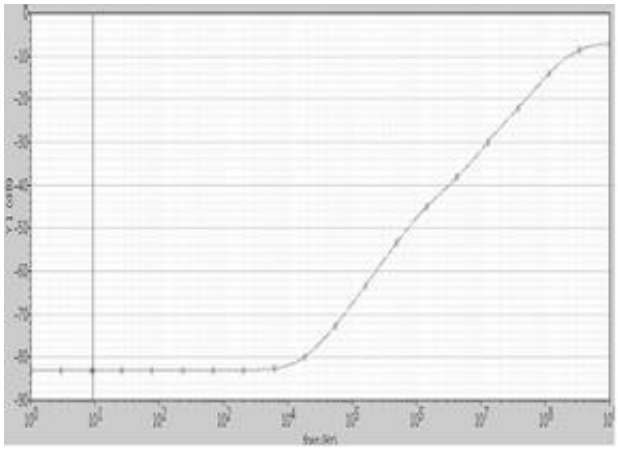

Figure 18- PSRR Simulation results

The power supply rejection of the DA is simulated using ELDO tool. An external script used to measure the quantities. 1V AC added in order to verify the power supply rejection of DA. All the analog input is forced low-to-high to get the full-scale output. Then the power supply rejection is measured on the DA analog output. The resulting output waveform which is simulated across corners is shown in Figure 19.

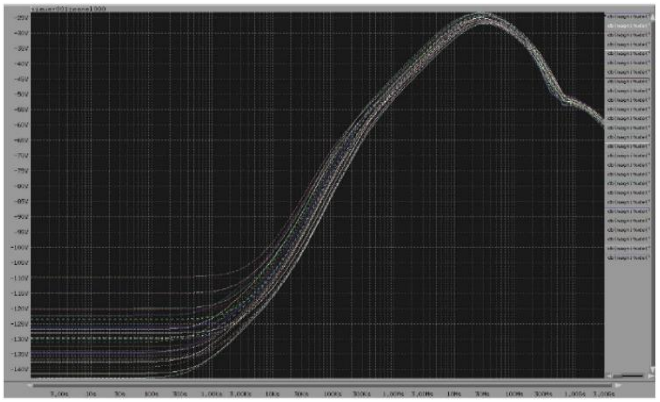

Fig. 19- Power supply rejection shown on DA output

The Power Supply Rejection Ratio (PSRR) is expected around 70 dB and it should not exceed 90 dB. The achieved PSRR is around 83 dB. The power dissipation is 120µW with operating frequency of 10 GHz. It is required to reduce power dissipation and limit it to less than 50 µW; this is achieved with proper design of transistor geometries. Figure 20 presents the Transconductance Vs common mode voltage (V_{CM}) variation for the designed DA. Input is varied and transconductance is calculated and corresponding graphs generated. The variation in the transconductance is less than 0.71% demonstrating stability in the performances of DA circuit.

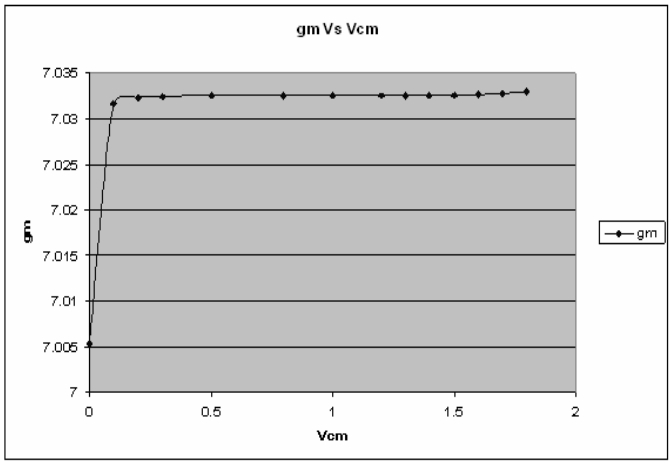

Figure 20-Constant Transconductance

The DA circuit is evaluated as comparator circuit. The simulation of the DA is carried out with a test case where a PWL signal is provided as the analog input to the DA. Power supply is set to 1.8V and the input data is set at 80 MHz is given as the clock. A delay (0.3ns) is added to the input to compensate the layout parasitic capacitance which will cause the input delay. The simulation results for the comparator operation are shown in the Figure 21.

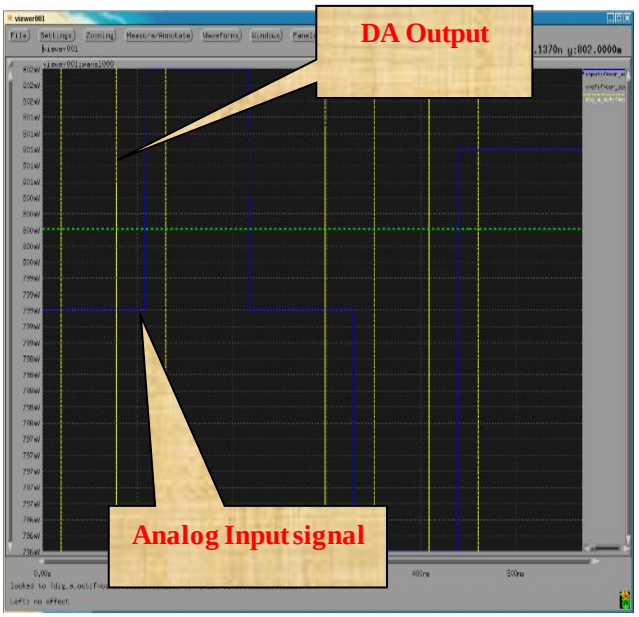

Fig. 21 Simulation results of DA

In this work Differential Amplifier Design Parameters are considered as VDD, DC Gain, Power Supply Rejection Ratio (PSRR) Slew Rate, Power Dissipation and Common Mode Rejection Ratio (CMRR). The results obtained are tabulated in table 4 and the Percentage Improvement is calculated for all the parameters mentioned and compared.

Table 4-Comparison of DA Circuits

Differential Amplifier design parameters	Existing literature using 32nm FINFET technology [3]	Present work using 22nm FINFET technology	Percentage improvement
VDD	1.8 V	1 V	80%
DC Gain	103 dB	107 dB	3.88%
PSRR	32.4dB	83dB	60.96%
Slew Rate	5V/µS	6V/µS	16.67%
Power dissipation	58µW	120µW	51.66%
CMRR	11.34dB	76 dB	85.07%

The DA Circuit designed in this work has a gain improvement of 3.88%. This is the most significant for improving SNR. The PSRR has been improved by a factor of 50Decibels and is suitable for low voltage ADC's. The power dissipation of 120µW can be reduced further by reducing slew rate.

VI. CONCLUSION

In this work a Differential amplifier circuit is designed that could be used for design high speed, low power ADC based on SAR logic using model parameters of high-k FINFET in 22nm technology. The FINFET device parameters are considered from Predictive Technology Model (PTM). The VI Characteristics of FINFET is plotted considered at 22nm

technology with high-K dielectric. Output characteristics for varying width of 22nm technology HIGH-k FINFET based inverter is evaluated. The gain and phase-margin of Differential Amplifier are identified to be greater than 107dB and 63° respectively. In this work a 1 V Supply is used as an input voltage, the Power dissipation is 50 µW and the overall performance of Differential Amplifier circuit was improved by 4%. The Power Supply Rejection Ratio (PSRR) is estimated to be around 83 dB. Slew rate is 6V/µs and the ratio of dynamic range is 83.77%. Also, the dynamic range of the differential amplifier is found to be 1.6754. The designed DA sub circuit is suitable for high speed ADC design operating at 100 MHz.

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