Static NP Domino Carry gates for Ultra Low Voltage and High Speed Full Adders

Sohail Musa Mahmood and Yngvar Berg

***Abstract*— In this paper we present different configurations of static ULV NP domino carry gates using precharge and pass transistor logic. The proposed ULV domino carry gates are aimed for high speed serial adders in ultra low-voltage applications. In terms of frequency, speed, PDP and EDP, the ULV carry gates offers significant improvement compared to conventional CMOS carry gate. At Minimum Energy Point at $250mV$, the proposed carry gates have less than 5% of the delay than the conventional CMOS Carry gate. Furthermore, the Power and Energy Delay Product is less than 23% and 1% respectively relative to conventional CMOS Carry gate at the same supply voltage. The simulated data presented is obtained using a $90nm$ $TSMC$ CMOS process.**

***Index Terms*— Low-Voltage, High-Speed, Carry gate, NP Domino Logic, Precharge, CMOS, Digital, Pass Transistor Logic.**

I. INTRODUCTION

In recent years, the power problem has emerged as one of the fundamental limits facing the future of CMOS integrated circuit design. The aggressive scaling of device dimensions to achieve greater transistor density and circuit speed results in substantial sub-threshold and gate oxide tunnelling leakage currents. Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits.

Depending upon the application, there are numerous methods that can be used to reduce the power consumption of VLSI circuits, these can range from low-level measures based upon fundamental physics, such as using a lower power supply voltage or using high threshold voltage transistors; to high-level measures such as clock-gating or power-down modes. The power consumption in digital circuits, which mostly use complementary metal-oxide semiconductor (CMOS) devices, is proportional to the square of the power supply voltage[1]; therefore, voltage scaling is one of the important methods used to reduce power consumption. To achieve a high transistor drive current and thereby improve the circuit performance, the transistor threshold voltage must be scaled down in proportion to the supply voltage. However, scaling down of the transistor threshold voltage Vt results in significant increase in the sub-threshold leakage current.

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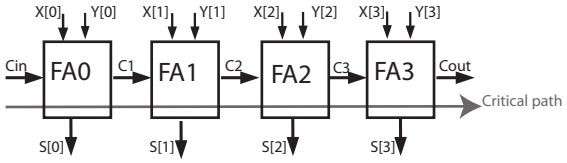
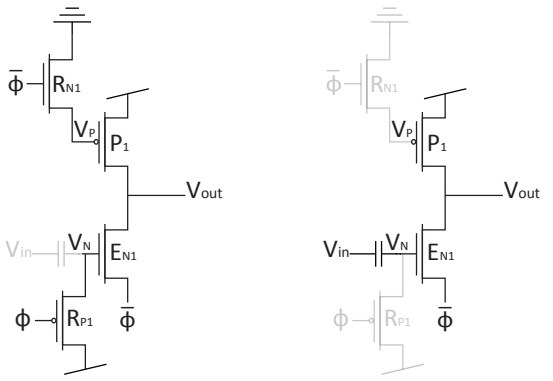


Fig. 1: *Four Bits Full Adder.*

Figure 1[2] shows a four bit full adder. Four full adders are cascaded in a chain, each of them has its C_{out} connected to C_{in} of the following one. The $Carry$ signal propagates through the whole chain. The Full adder performs in the propagation mode when the input signals $X \neq Y$ which makes $C_{\text{out}} = C_{\text{in}}$. The overall worst case delay is obtained when all the Full Adders operate in the propagation mode in a chain, and the $carry$ signal has to propagate from the first to the last full adder in the chain. Thus Carry propagation path is the most critical path when an addition of more than two bits is desired, which makes it a speed limiting factor for many high speed applications. By using complex carry look ahead techniques or applying parallel structures, the delay can be reduced compared to a simple serial adder shown in Figure 1 at the cost of increased complexity, power consumption and chip area.[3]

Floating-Gate (FG) gates have been proposed for Ultra-Low-Voltage (ULV) and Low-Power (LP) logic [4]. However, in modern CMOS technologies there are significant gate leakages which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances, either poly-poly, MOS or metal-metal, to the transistor gate terminals, the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [4]. There are several approaches for both analog and digital applications using FG CMOS logic proposed in [5], [6], [7], [8]. The gates proposed in this paper are influenced by ULV non-volatile FG circuits [9].

In this paper, we are focused on implementing Ultra-



(a) *Precharge Phase.* (b) *Evaluate Phase.*

Fig. 2: NP domino inverter in a) precharge phase and b) evaluate phase.

Low-Voltage (ULV) and high speed NP Domino carry gates. In Section II, an extended description of the NP Domino ULV inverter [10] is given. Conventional ULV carry gates are presented in Section III. In Section IV, different implementations of ULV carry gates are presented using pass transistor logic [13]. Simulation results are given in Section V and a conclusion is given in Section VI.

II. High speed and Ultra-low-voltage floating-gate NP domino Inverter

The ULV logic carry gates presented in this paper are related to the ULV domino logic style presented in [10], [11], [12]. The main purpose of the ULV logic style is to increase the current level for low supply voltages without increasing the transistor widths. We may increase the current level compared to complementary CMOS using different initialization voltages to the gates and applying capacitive inputs. The extra load represented by the floating capacitors are less than extra load given by increased transistor widths. The capacitive inputs lower the delay through increased transconductance while increased transistor widths only reduce parasitic delay. The proposed logic style may be used in critical high speed and low voltage sub circuits together with conventional CMOS logic.

The High speed and ULV N domino inverter represented in [10] is shown in Figure 2. The clock signals ϕ and $\overline{\phi}$ are used both as control signals for the recharge transistors R_{P1} and R_{N1}, and as reference signals for nMOS evaluation transistor E_{N1}. The recharge and the evaluation phase of the proposed logic style is characterized below:

A. *Precharge/Recharge phase*

When ϕ switches from 1 to 0, the circuit is in precharge/recharge phase. During this phase, R_{P1} turns on and recharges the gate of E_{N1} to 1. Meanwhile $\overline{\phi}$ switches from 0 to 1 which turns on R_{N1} and recharges the gate of pMOS transistor P_1 to 0. Thus both E_{N1} and P_1 turn on in the precharge phase and precharge the output node V_{out} to V_{dd}. Figure 2a shows the precharge mode of this circuit. The gray shaded lines indicate the components which are not operating in the precharge mode.

B. *Evaluation phase*

In the evaluation phase, clock signals ϕ and $\overline{\phi}$ switch from 0 to 1 and 1 to 0 respectively. Both recharge transistors R_{P1} and R_{N1} switch off which make the charge on nodes V_{p} and V_{n} to be floating as indicated by the gray shadow lines shown in Figure 2b. The output node V_{out} floats as well until an input transition occurs. The input signal V_{in} must be *monotonically rising* to ensure the correct operation for the N domino inverter. This can only be satisfied if

- input signal *Vin* is low at the beginning of the evaluation phase, and
- *Vin* only makes a single transition from 0 to 1 in the evaluation phase.

As V_{in} makes a positive transition, the capacitance at the gate of E_{N1} charges and discharges. The charge at node V_{N} can be estimated by using Equation (1). We assume that the initial charge at the node is V_{dd}, V_{in} is charged upto V_{dd} as well. The capacitive division will be $\frac{1}{2}$ if C_{in} and $C_{\mathrm{parasitic}}$ assume to be equal. This makes the voltage at the gate terminal V_{N} 1.5 $\times$ higher than the voltage supplied by the supply voltage V_{dd}[4]. Thus evaluation transistor E_{N1} strongly biased which increases the current level of the transistor. Thus Pull Down Network (PDN) becomes much stronger than PUN and discharges the output node V_{out} to 0.

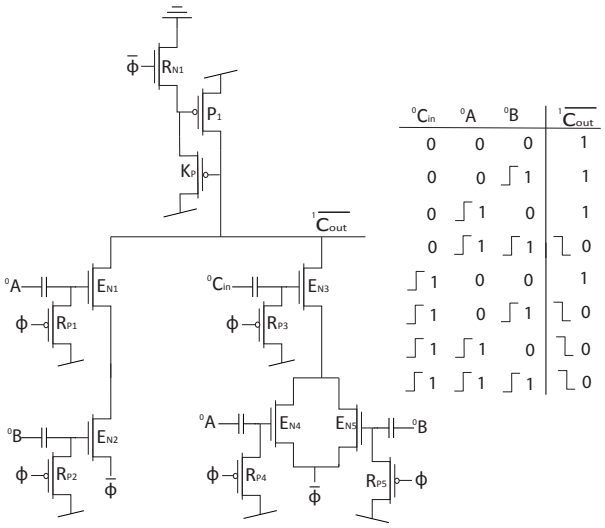
$$V_{\mathrm{N}} = V_{\mathrm{init}} + \Delta V_{\mathrm{in}} * \frac{C_{\mathrm{in}}}{C_{\mathrm{in}} + C_{\mathrm{parasitic}}} \tag{1}$$

III. Ultra-low-voltage and semi-floating-gate NP domino Carry circuit

Different NP domino logical gates are presented in [11] which operate in the sub-threshold regime and result in a really fast switching speed. The CARRY circuit can be implemented using the same logic style which can increase the propagation speed of the *carry bit* in a serial chain of cascaded full adders shown in Figure 1. C_{out} logic function of a Full Adder is shown in Equation 2 which concludes that C_{out} generates an *AND* functionality for the adding bits A and B as far as C_{in} is 0. With the arrive of C_{in} bit, C_{out} generates an *OR* functionality for A and B.

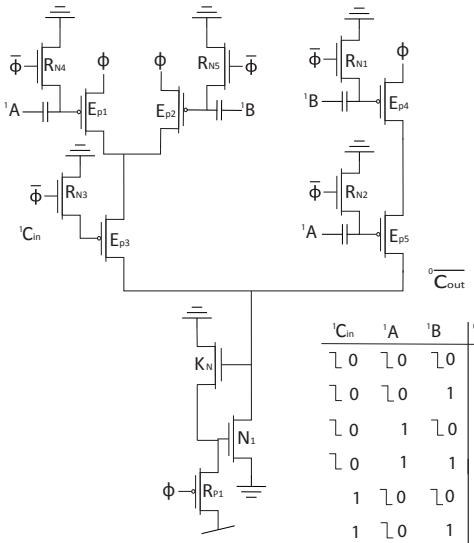
$$C_{\mathrm{out}} = A \cdot B + C_{\mathrm{in}} \cdot (A + B) \tag{2}$$

Two ULV domino Carry gates are shown in Figure 3. The output node $\overline{C_{\mathrm{out}}}$ in Figure 3a and 3b is precharged to 1 and 0 respectively. The CARRY gate has been implemented by combining ULV domino $Nand$ and Nor gates implemented in [11] together with a control signal C_{in}. C_{in}



$^0C_{in}$	^0A	^0B	$^1\overline{C_{out}}$
0	0	0	1
0	0	⌈1	1
0	⌈1	0	1
0	⌈1	⌈1	⌊0
⌈1	0	0	1
⌈1	0	⌈1	⌊0
⌈1	⌈1	0	⌊0
⌈1	⌈1	⌈1	⌊0

(a) *Precharge to 1 (N type).*



$^1C_{in}$	^1A	^1B	$^0\overline{C_{out}}$
⌊0	⌊0	⌊0	⌈1
⌊0	⌊0	1	⌈1
⌊0	1	⌊0	⌈1
⌊0	1	1	0
1	⌊0	⌊0	⌈1
1	⌊0	1	0
1	1	⌊0	0
1	1	1	0

(b) *Precharge to 0 (P type).*

Fig. 3: ULV domino Carry Gates I (CARRY1).

ascertains whether the output node gives a $Nand$ or Nor functionality for the input bits A and B. A desired ULV domino inverter implemented in [10] should be connected at the output node of the implemented circuit to obtain C_{out}. This means that the output node $\overline{C_{\text{out}}}$ of a N type ULV domino carry gate should be connected to a P type ULV domino inverter to obtain a desired C_{out}.

In order to retain the precharged value for the implemented Carry gates until the desired input bits arrive, the evaluation transistors P_1 to V_{DD}, or N_1 to GND should be made stronger than the other evaluation transistors. By applying an additional pMOS transistor K_{P} and nMOS transistor K_{N} in Figure 3a and 3b respectively, the gate of the evaluation transistors P_1 and N_1 will be pulled to V_{DD} and GND respectively when the output node $\overline{C_{\text{out}}}$ gets a transition in the evaluation phase which turns on the keeper transistors. This partially turns off the evaluation transistors P_1 and N_1 and let the output node $\overline{C_{\text{out}}}$ swings fully to V_{DD} and GND respectively. This helps to reduce the static current which matches the OFF current I_{off} in the conventional CMOS inverter. The Noise Margin NM is defined in Equation 3.

$$NM = \frac{\text{I}_{\text{on}}}{\text{I}_{\text{off}}} \tag{3}$$

Thus, by adding keepers, improves both the noise margin and the power consumption of the proposed circuits.

IV. ULV NP DOMINO CARRY CIRCUIT USING PTL

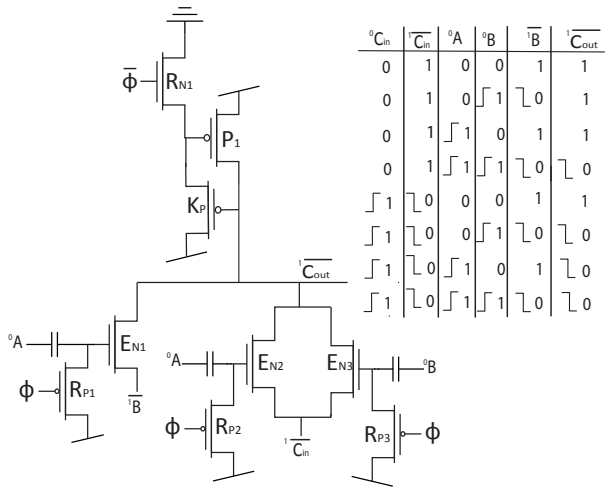
The same logic function can be obtained by using fewer number of transistors with the help of *Pass Transistor logic* (PTL) as compared to the conventional style, which reduces the overall delay of the system and saves the area on the chip. Circuits implemented in Figure 4 shows ULV NP domino Carry gates with the help of PTL. As compared to the carry gate implemented in Figure 3, the total number of evaluation transistors labelled E have been reduced from 5 to 3. The carry input bit needs only to pass through a single evaluation transistor before reaching the output node.

In Figure 4, the evaluation transistors labelled E can be described as pass transistors with an increased current level. If we consider the circuit in Figure 4a. As far as C_{in} is low, the output node $\overline{^1C_{\text{out}}}$ only switches from 1 to 0 when the evaluate transistor E_{N1} acts as a pass transistor for the input signal $\overline{^1B}$ when $\overline{^1B}$ switches from 1 to 0 and the other input ^0A switches from 0 to 1 in the evaluation phase. When C_{in} bit becomes high, only one of the two evaluation pass transistors E_{N2} or E_{N3} needs to turn on to pull the output node $\overline{^1C_{\text{out}}}$ from 1 to 0. This implies that E_{N2} or E_{N3} acts as pass transistor for input $\overline{^1C_{\text{in}}}$ when $\overline{^1C_{\text{in}}}$ switches from 1 to 0 and at least one of the two other inputs ^0A or ^0B switches from 0 to 1.

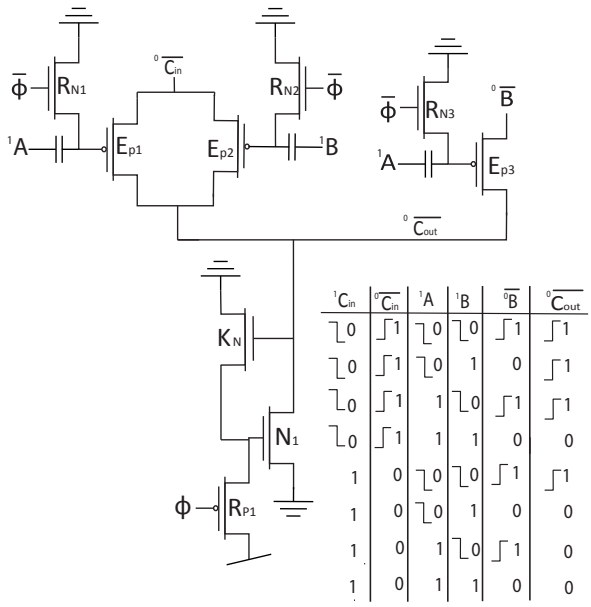
Another alternative solution of ULV domino NP Carry gate using PTL is implemented in Figure 5. N type Carry gate in Figure 5a resembles the Carry gate implemented in Figure 4a. Both circuits perform entirely in the same sense as far as $^0C_{\text{in}}$ is logically 0. When $^0C_{\text{in}}$ switches from 0 to 1 in the evaluation phase, both parallel connected evaluation transistors E_{N2} or E_{N3} turn on and act as pass transistors for the inputs $\overline{^1A}$ and $\overline{^1B}$. Under this instance, only one of the two inputs $\overline{^1A}$ or $\overline{^1B}$ requires to switch from 1 to 0 to pull the output node $\overline{^1C_{\text{out}}}$ to 0.

V. SIMULATED RESPONSE

The data simulated is based on a 90nm TSMC CMOS process. To avoid underestimation of the implemented circuits and to obtain more realistic waveforms, clock signals have been made by inserting two symmetric conventional CMOS inverters between the ideal voltage sources and the clock signals. In the same way, input signals have been

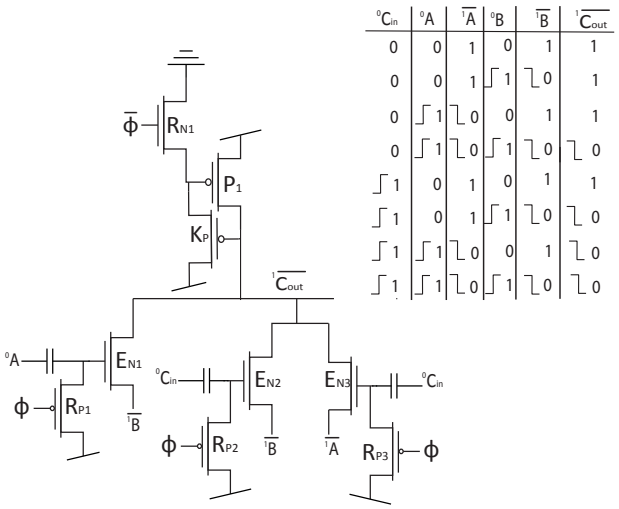


(a) *Precharge to 1 (N type).*

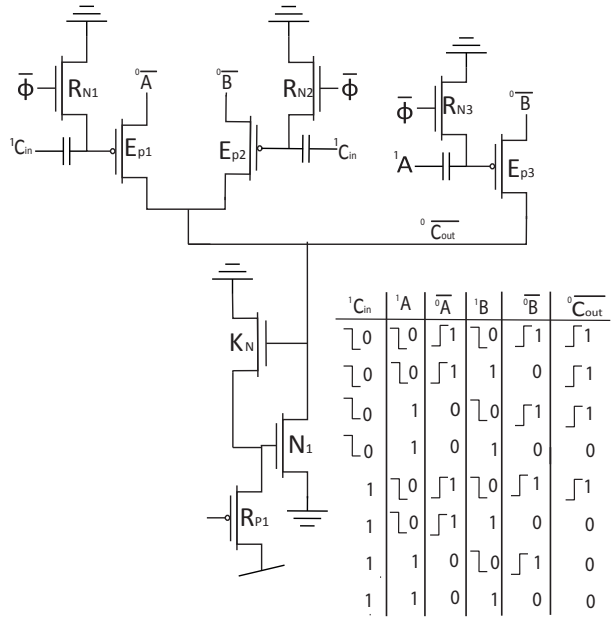


(b) *Precharge to 0 (P type).*

Fig. 4: ULV domino Carry Gates using PTL II (CARRY2).



(a) *Precharge to 1 (N type).*



(b) *Precharge to 0 (P type).*

Fig. 5: ULV domino Carry Gates using PTL III (CARRY3).

made by inserting ULV domino inverters implemented in [10] between the voltage sources and the input nodes. An identical gate for each logic style is applied as load at the output nodes of all circuits. The proposed ULV domino carry gates are simulated for the worst case scenario where only one of the two input bits are high and the and the $carry$ signal has to propagate through the full adder.

The performance of the proposed ULV domino carry gates implemented in Figure 3, 4 and 5 are shown in Table I. The implemented carry gates are directly target to operate in the sub-threshold regime. The presented gates are compared with the conventional CMOS carry gate[14] at the same supply voltages. Table I demonstrates speed performance, together with power consumption and other figure of merits (PDP and EDP) in order to optimize the *Minimum Energy Point* MEP for the proposed ULV domino Carry gates comparable with conventional CMOS carry gate.

The power consumed by the clock drivers are not included and must be taken into consideration for each specific application. Besides this, the Table also presents the operating limits of clock frequency which changes rapidly as the supply voltage varies. In Table I, the style labelled *N Carry* and *P Carry* represents the proposed N and P type domino carry gates respectively. Avg represents the average delay or power between the proposed N and P type domino carry gates.

The average propagation delay between N and P type

Style	Comment	100mV	150mV	200mV	250mV	300mV	350mV	400mV
CLK	f_{clk} (MHz)	0.83	2.5	8.3	16.67	66.67	83.3	125
Conventional Carry	Delay (ns)	328	101	25.4	10.4	2.56	1.55	0.782
	Power (nW)	0.008145	0.055	0.34	1.12	6.83	10.35	23
	PDP (10^{-18}j)	2.672	5.55	8.64	11.65	17.48	16.04	17.97
	EDP (10^{-27}js)	876.4	560.5	219.5	121	44.75	24.9	14.05
N Carry 1	Delay (ns)	53	18.74	2.49	0.318	0.162	0.05	0.022
P Carry 1	Delay (ns)	194	36.83	2.75	0.38	0.19	0.109	0.1086
Carry 1	Avg.Delay (ns)	123.5	27.785	2.62	0.349	0.176	0.0795	0.0653
	Relative delay (%)	37.65	27.52	10.31	3.36	6.88	5.11	8.36
	Avg.Power (nW)	0.0358	0.3078	1.907	7.55	41.1	100.8	265
	Avg.PDP (10^{-18}j)	4.423	8.552	4.996	2.635	7.234	8.014	17.305
	Relative PDP (%)	165	154	57.8	22.6	41.4	50	96.3
	Avg.EDP (10^{-27}js)	546.4	237.6	13.1	0.919	1.273	0.637	1.13
	Relative EDP (%)	62.35	42.4	5.97	0.76	2.84	2.56	8.04
N Carry 2	Delay (ns)	141.5	25.38	3.07	0.4127	0.183	0.0725	0.04516
P Carry 2	Delay (ns)	92.06	11.72	1.26	0.2976	0.166	0.1375	0.333
Carry 2	Avg.Delay (ns)	116.8	18.5	2.165	0.35	0.1745	0.105	0.189
	Relative delay (%)	35.61	18.32	8.52	3.36	6.82	6.77	24.18
	Avg.Power (nW)	0.01867	0.209	1.461	5.21	28.45	56.9	137
	Avg.PDP (10^{-18}j)	2.181	3.86	3.16	1.823	4.96	5.97	25.9
	Relative PDP (%)	81.6	69.55	36.57	15.65	28.37	37.22	144.13
	Avg.EDP (10^{-27}js)	254.7	71.41	6.84	0.638	0.865	0.627	4.897
	Relative EDP (%)	29.06	12.74	3.116	0.527	1.93	2.518	34.85
N Carry 3	Delay (ns)	141.5	22.5	3.35	0.475	0.22	0.092	0.0715
P Carry 3	Delay (ns)	265.7	31.1	2.75	0.504	0.248	0.182	0.883
Carry 3	Avg.Delay (ns)	203.6	26.8	3.05	0.489	0.234	0.137	0.477
	Relative delay (%)	62.07	26.53	12	4.7	9.14	8.84	61
	Avg.Power (nW)	0.01948	0.245	1.572	5.47	30.75	71.15	176.5
	Avg.PDP (10^{-18}j)	3.96	6.58	4.79	2.68	7.19	9.747	84.235
	Relative PDP (%)	148.4	117.35	55.1	23.01	41.15	60.57	468
	Avg.EDP (10^{-27}js)	807.5	176.4	14.63	1.312	1.684	1.335	40.2
	Relative EDP (%)	92.1	31.14	6.62	1.08	3.76	5.34	286

TABLE I: *Performance of ULV domino Carry gates compared to complementary CMOS Carry gate at different supply voltages.*

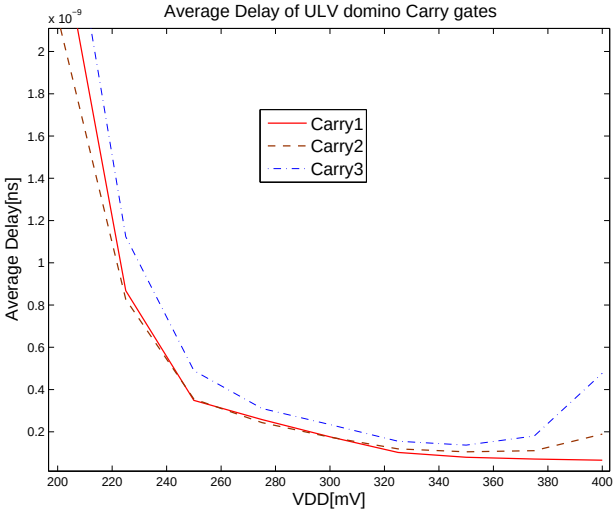


Fig. 6: *Average Delay of ULV domino carry gates for different supply voltages.*

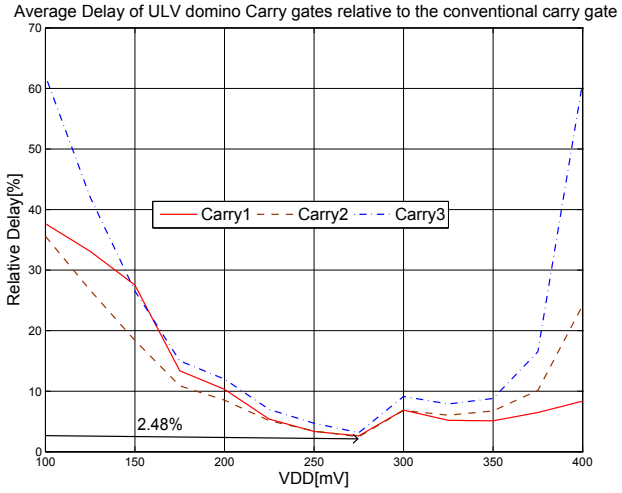


Fig. 7: *Delay of ULV carry gates relative to conventional CMOS carry gate for different supply voltages.*

Carry gates for the proposed ULV domino logic style is shown in Figure 6. The delay is in ns for the supply voltages under $225mV$ and decreases exponentially as the supply voltage increases. Beyond $300mV$, the propagation delay is only in the range of tens of ps. CARRY 1 and CARRY 2 contributes almost equal delay when the supply voltage is within $220mV$ and 320. Under $220mV$, CARRY 2 provides minimum propagation delay. On the other hand, CARRY 1 gives minimum delay when the supply voltage exceeds over $320mV$.

CARRY 3 is the slowest and less preferable in high speed applications due to low noise margin, as both parallel connected evaluation transistors E_{N2} or E_{N3} turn on in the worst case scenario, while only one of the two inputs $\overline{^1A}$ or $\overline{^1B}$ switches from 1 to 0. Thus both $\overline{^1A}$ and $\overline{^1B}$

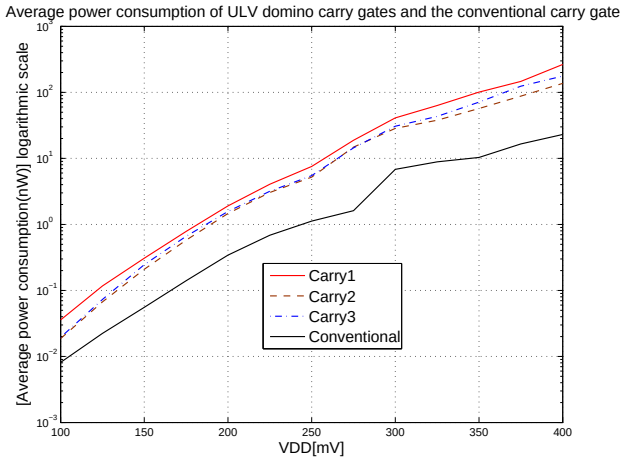


Fig. 8: *Average power consumption per ULV carry gate compared to conventional CMOS carry gate.*

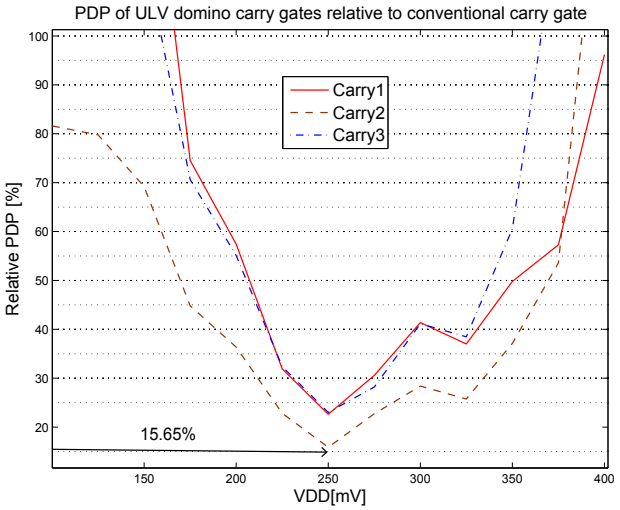


Fig. 9: *Average relative energy of ULV domino carry gates.*

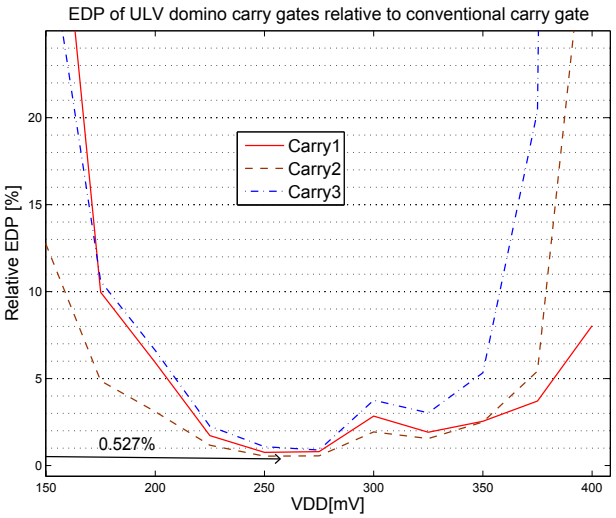


Fig. 10: *Average relative energy delay product of ULV domino carry gates.*

simultaneously contends at the output node, which makes the output transition slow and gives poor noise margin. However, it offers a more efficient solution in terms of area and power consumption as compared to CARRY 1.

The average delay between N and P type Carry gates for the proposed ULV domino logic style is compared with the conventional CMOS Carry gate in Figure 7. The relative delay is lesser than 20% for all the proposed domino carry gates when the supply voltage varies between $175mV$ and $375mV$. The overall best relative delay is achieved by using ULV domino carry gate proposed in Figure 4 which is obtained by using pass transistor logic. The reason is because the input carry bit only needs to propagate through a single evaluation transistor to reach the output node. Compared to conventional carry gate, the least average delay is achieved at the supply voltage of $275mV$, where CARRY2 only utilizes a delay of 2.48%.

The average power consumption per ULV domino carry gate is compared with conventional CMOS carry gate in Figure 8. The total power consumption per gate increases with supply voltage. As expected the power consumption for the ULV domino carry gates exceeds the power consumption of the conventional CMOS carry gate, giving the advantage of really fast speed. As shown in Figure 8, ULV domino carry gates using pass transistor logic (PTL) contributes minimum power consumption than the domino carry gate implemented in Figure 3. This happens as the total number of evaluation transistors reduces from 5 to 3 by using PTL which consumes less power in the evaluation phase.

The average energy of the ULV domino carry gates relative to conventional CMOS carry gate for different supply voltages is shown in Figure 9. The *Power Delay Product* PDP for the proposed ULV carry gates is lower than the conventional carry gate for the supply voltage between $175mV$ and $350mV$. This is mainly caused due to very reduced delay for the proposed carry gates relative to the conventional carry gate.

Comparing the graphs in Figure 7 and 9 concludes that minimum relative PDP corresponds to the maximum relative speed for the proposed carry gates. All three proposed ULV domino carry gates have the minimum relative PDP of lower than 25% at the supply voltage of $250mV$, which makes it the Minimum Energy Point. CARRY 2 is the most efficient solution as it only contributes 15.65% PDP relative to conventional Carry gate. As the supply voltage reduces below $175mV$, the relative PDP for CARRY 1 and CARRY 3 exceeds 100% while the relative PDP of CARRY 2 is still beyond the PDP of conventional Carry gate. However, the relative PDP of CARRY 2 becomes worse than CARRY 1 as the supply voltage exceeds $375mV$.

The relative Energy Delay Product EDP for the ULV domino carry gates for different supply voltages is shown in Figure 10. The relative EDP for all the proposed ULV domino carry gates is lesser than 30% for the supply voltage between $175mV$ and $375mV$ which directly corresponds to the same supply voltage range where the PDP is minimum

	CARRY1	CARRY2	CARRY3
Relative Delay(%)	3.36	3.36	4.7
Relative PDP(%)	22.6	15.65	23.01
Relative EDP(%)	0.76	0.527	1.08

TABLE II: *The delay, PDP and EDP of ULV domino carry gates at Minimum Energy Point ($250mV$) relative to conventional CMOS carry gate.*

as shown in Figure 9.

At Minimum Energy point ($250mV$), the EDP of of all proposed ULV carry gates is lower than 1.5% relative to a conventional carry gate. However, CARRY 2 is characterized by least relative EDP with a value closer to 0.527% at $275mV$. The relative EDP of CARRY 2 is far better than the other solutions at the supply voltage under $175mV$, but becomes worse than CARRY 1 as the supply voltage increases beyond $375mV$.

Table II is showing a summary of delay, PDP and EDP of proposed ULV domino carry gates relative to conventional CMOS carry gate at Minimum Energy Point with a supply voltage of $250mV$. CARRY 1 and CARRY 2 have the same relative delay of 3.36% thus both solutions are efficient for ultra low voltage and high speed applications. However for low power applications, CARRY 2 is the most efficient solution as it consumes less power than the other two ULV carry gates and results in lower PDP and EDP. CARRY 3 is the slowest and less preferable for high speed applications, but it offers a more efficient solution than CARRY 1 in terms of area and power.

VI. Conclusion

Different ultra low-voltage NP domino Carry gates have been presented in this paper. The ULV domino carry gates are high speed, i.e. the delay compared to conventional CMOS carry gate is less than 5% for a supply voltage equal to $250mV$. The power and energy delay product of the proposed ULV carry gates is less than 23% and 1% relative to conventional CMOS carry gate respectively at minimum energy point. Both power and area can be saved if we can avoid using parallel adders by applying ULV domino carry gates when ultra low voltage solutions are preferable. In this manner we may take the advantage of the speed improvement and the reduction of power and area.

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