

# A 20 Gb/s Fast Acquisition Clock and Data Recovery Circuit in 0.18 $\mu\text{m}$ CMOS

Naeeme Modir, Samad Sheikhaei, Behjat Foroozande, Elias Soleiman

**Abstract**— This paper presents a 20 Gb/s injection-locked clock and data recovery circuit for burst-mode applications. Using a new injection-locked LC oscillator as a half rate CDR, relaxes the speed requirements of VCO and re-timing flip flops. This allows us to design higher speed CDR with lower power consumption. Complementary clocks drive two flip flops in the decision circuit for re-timing the data. Simulated in 0.18  $\mu\text{m}$  CMOS, the circuit consumes 68.7 mW at 20 Gb/s, while the recovered clock rms jitter is 0.84 ps, rms in response to a  $2^7$ -1 PRBS.

**Keywords**— burst mode, clock and data recovery (CDR), fast acquisition CDR, injection locking, injection-locked LC oscillator

## I. INTRODUCTION

Clock and data recovery circuits (CDR) are widely used in modern high speed serial link communications where a data stream is transmitted without any additional timing reference. Therefore clock should be extracted from the data to reach synchronous data processing in the receiver. In high-speed optical multi-access network applications such as passive optical networks (PON), amplitude and phase of packets are not fixed and may vary from one packet to another [1]. Therefore, burst-mode receivers must realign clock phase at beginning of every packet and as a result they require fast response time to improve detection of short packets or burst data [2]. The clock and data recovery circuit in these receivers extracts a clock from the header area of the burst packets in a small fraction of a packet transmission time [3].

The clock and data recovery circuits can be implemented as open or closed loop circuits. Closed loop CDRs usually use PLL architecture to track the data phase. While closed loop CDRs offer a great performance in the presence of frequency offset and can also suppress the jitter, (Jitter suppression has been achieved by using low bandwidth loop filters in PLL-based CDRs) It leads to long lock time which disqualified them to be used in burst mode data recovery. Since open loop CDRs can achieve fast locking, they are attractive solutions for burst mode data communications. However, open loop CDRs suffer from limited frequency tracking and very weak jitter suppression [4]. Since no repeater is required in these

applications, jitter transfer is not a serious issue [5] and open loop CDRs are proper solution for such applications.

Open loop CDRs can be designed by Gated Voltage Control Oscillator (GVCO) or Injection-Locked LC oscillator (ILO). GVCO is used in [5]-[7] for burst mode applications. CDR circuits using GVCOs consume low power and have compact structures. However, ring structure of the GVCOs which is shown in Fig.1 will raise jitter in extracted clock. Also, the operating frequency of GVCOs is lower than ILO [8]. In injection locking method LC VCO is used instead of ring oscillator. It has better phase noise and higher speed in comparison to ring oscillator.

A CDR circuit based on injection locking technique is described in [8], in which rise and fall edges of received data has been detected with an edge detector and then injected to an LC oscillator, so it extracts a full rate clock from the input data. However, using injection-locked oscillator as a full rate CDR in the foregoing technique leads to design a high frequency VCOs. Another issue is design of edge detector which needs high speed CML XOR and delay cell circuits. In [9] a half rate injection-locked CDR is described. In this method the injection signal is applied to a super-harmonic ILO. In a super-harmonic structure the only block which operates at twice of the oscillator frequency is edge detector. Therefore, design of edge detector is serious bottleneck in high speed CDR design. Also, these blocks increase power consumption and area of the chip.

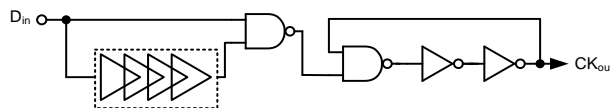


Fig. 1 Gated voltage control oscillator (GVCO)

In this paper, a high speed injection-locked CDR circuit has been proposed with a new injection technique. This new architecture improves the speed performance of injection-locked CDR circuit by eliminating edge detector and sampling data with a half rate clock. Since in this new injection technique the output frequency of the oscillator is half of the bit rate, the VCO and the decision circuit operation frequencies are reduced to half of the corresponding value in full rate techniques.

In [8] long runs cause fluctuations in  $\text{VCO}_1$  output amplitude due to steering unbalanced currents in oscillator

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outputs. So to purify the clock, output of VCO<sub>1</sub> is injected to another identical VCO. However, in our proposed CDR there is no steering current in long runs. Therefore, the output clock does not suffer from fluctuations.

II. THE PROPOSED CDR

Fig. 2 shows the proposed CDR architecture. This architecture incorporates an injection-locked oscillator, a reference PLL and a decision circuit which consists of two retiming flip-flops. The data is injected to the injection-locked LC oscillator to recover the clock. The oscillator output is fed to a clock buffer and the differential output signal of the clock buffer is used by two flip flops for sampling the data with the half-rate clock. As the injection locking technique has narrow locking range, the VCO may not lock to the frequency of the incoming data stream. Therefore, a PLL is used to generate a 10GHz clock from a reference clock which is 312MHz here. The VCO of the reference PLL is designed identical to the VCO in injection locking part; so the control voltage of this VCO can be used as an initial value or approximation to help the VCO lock easily to the incoming data. It also helps to compensate for the PVT variations [8]. The two oscillators may suffer from mismatches in fabrication, but it can be minimized with proper designing of layout. Since the data line can pull the VCO frequency through coupling between D and CLK ports of the flip flops, a clock buffer is used to isolate them [10].

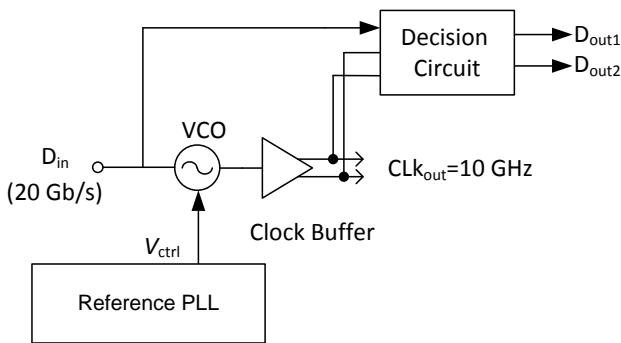


Fig. 2 The 20Gbps burst-mode CDR architecture

In the decision circuit, the midpoint of each bit should be sampled by one of the two flip-flops that are driven by clk<sub>p</sub> and clk<sub>n</sub>. In the proposed circuit the clock locks to the point other than midpoint of the data, therefore the delay of clock buffer should be carefully adjusted to set 90 degree phase difference between extracted clock and input data. Fig. 3 shows the proposed CDR circuit.

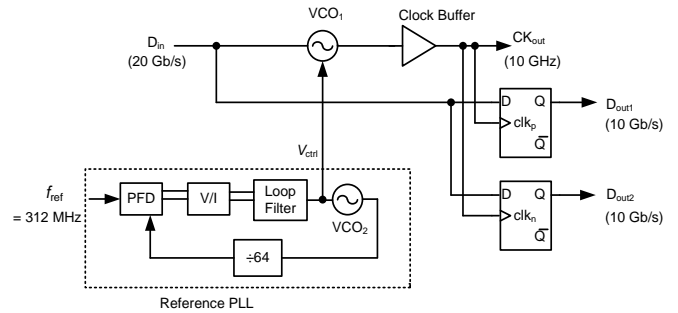


Fig. 3 Schematic of proposed CDR

Since the data rate is constant, the output frequency of the oscillator is constant as well. Nevertheless, VCO deviates from its locking conditions by the PVT variations and fail the correct data recovery. As stated before, a reference PLL is used to accommodate the variations and correct the free running frequency of the VCO.

III. BUILDING BLOCKS

A. Proposed Injected-Locked LC Oscillator

In full rate CDRs, output clock frequency must be equal to the data rate for sampling the random data. In [8] the data is applied to an edge detector circuit for creating a frequency component at the input data rate. To increase CDR speed, clock frequency can be half of the data rate and sample the data with two 180 degree phase difference signals.

There are several techniques to inject incident signal to differential LC oscillators. In the first technique, incident signal is injected to the gate of the tail transistor as is shown in Fig.4 (a) [11]. Here cross coupled transistors mix the output and incident signals to generate  $\omega_0 \pm \omega_{inj}$  component while the sum component ( $\omega_0 + \omega_{inj}$ ) filtered by the tank [12]. In this method, the tail node oscillates at twice the output frequency, so it is a good point for a second harmonic injection.

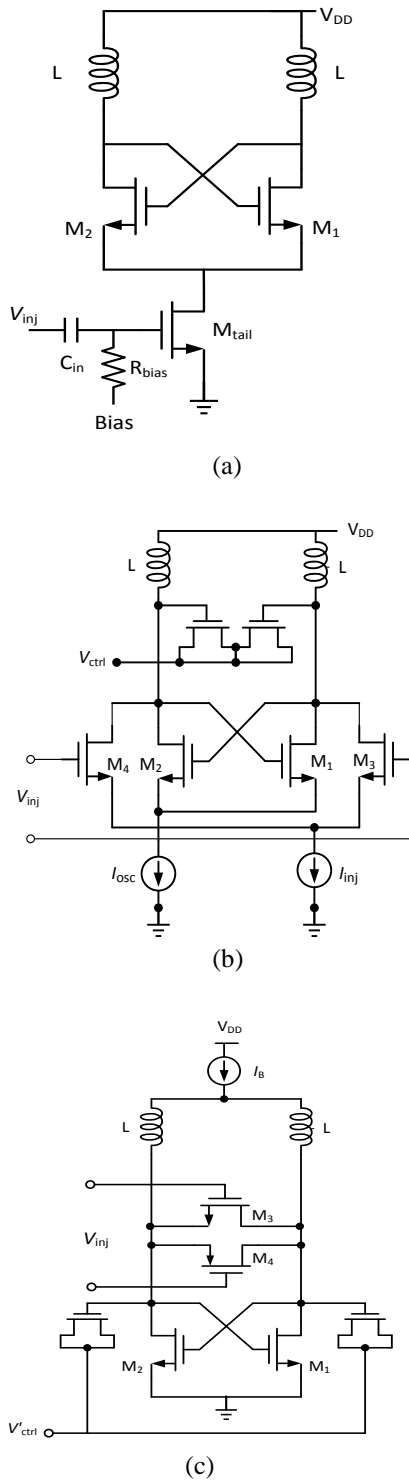


Fig. 4 Injection-Locked LC Oscillators architectures (a) Classical injection-locked oscillator (b) Direct injection-locked oscillator scheme (c) Another direct injection-locked oscillator scheme

In the other technique the incident signal directly injected to the LC tank of oscillator via MOS transistors [8], [13]. In [8] the coupling has been done with two NMOS transistors as shown in Fig. 4(b). And in [13] the switch transistors are located between two outputs as shown in Fig.4(c).

The drawback of the first topology is large input capacitor which reduces locking range and frequency operation of the oscillator [13]. Also, this structure has single-ended injection input and as a consequence the pervious stage sees non-symmetric load. The topology, shown in Fig. 4(b), has lower input capacitor and also differential inputs, but it cannot be used as a super harmonic structure. In addition this technique suffers from asymmetric loading on the oscillator outputs nodes in long runs. Therefore, long runs lead to distorted output signal in oscillator output [14]. For using third topology in a half-rate CDR structure, the input data cannot be directly injected to the injection switches because it shorts the VCO outputs in long runs. Therefore the data should be applied to an edge detector before injecting to VCO.

In proposed structure as is shown in Fig. 5(a) the data is injected to an ILO with a simple RC network directly instead of applying to an edge detector. M1 and M2 create an incident current in rise edge of the data. Thus, in every data transition the two outputs of the oscillator will be shorted. Therefore the oscillator output clock will lock to data edges. This structure is used as a half rate CDR in this paper. Its advantages are low power consumption and reducing maximum operational frequency by half in compare to the full rate structures. The foregoing technique can be used as full rate CDR as is shown in Fig 5(b).

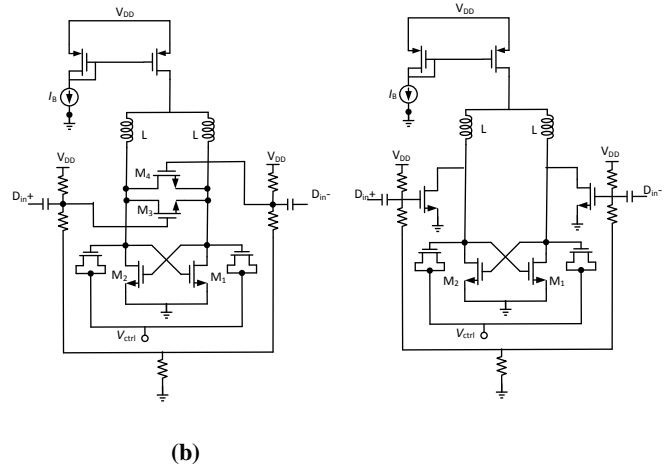


Fig. 5 Proposed injection-locked LC oscillator architectures (a) half rate, (b) full rate

Fig. 6 shows the circuit which has been used to inject the data to oscillator. For correct circuit operation, M1 and M2 must be on for a short time in every data triggers which needs sharp rising at the transistors gate. To generate required gate voltage at M1 and M2 gates, small RC time constant will be needed at the data input(C, R1) for correct AC operation. In addition, M1 and M2 DC bias should be adjust carefully. To have small RC time constant for AC operation and proper DC bias with low power dissipation, the network at fig.6 has been proposed. In this circuit, AC signal sees the resistor equal to  $2R_1$  while PMOS transistors DC currents see  $R_1+2R_2$ . So we can Choose  $R_1 \ll R_2$  to have small RC time constant. Fig. 7 shows the  $V_{g1}$  and  $V_{g2}$  for 20 Gb/s input data. In every fall

edge of the data, gate voltages go down from bias point so the transistors do not pass any current. Fig. 8 shows the current of M1 and M2 for a 20 Gb/s input data.

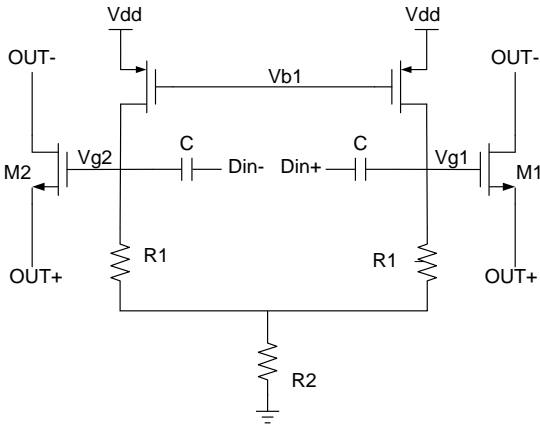


Fig. 6 Circuit for Direct Injection of Data

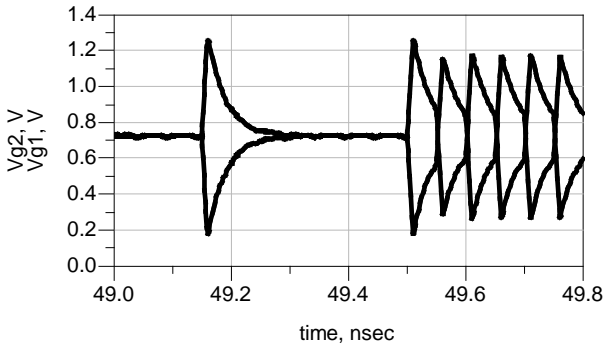


Fig. 7 Vg1 and Vg2

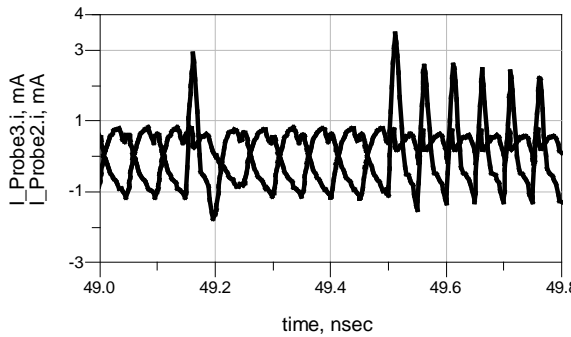


Fig. 8 The Injection Currents

In [12] locking range of an ILO is calculated using a phase-domain approach. Injection causes phase shift around feedback loop of the oscillator. To satisfy Barkhausen phase criterion the tank must oscillate in a new frequency  $\omega_{inj}$ . The obtained locking range is proportional to  $\omega_0/Q I_{inj}/I_{bias}$ , where  $I_{inj}$  is the injection current,  $I_{bias}$  is the bias current of the ILO,  $Q$  is the quality factor and  $\omega_0$  is the self-oscillation frequency of the LC tank. It can be seen from the above equation that the locking range is directly proportional to the  $I_{inj}/I_{bias}$  and

inversely proportional to the quality factor. For increasing locking range we can enhance the injection ratio or decrease the quality factor. To increase  $I_{inj}$  we can increase the size of the switch transistors but it increases the parasitic capacitances and reduces the operation frequency of the ILO [15].

*B. Flip Flop*

For designing high speed circuits, current mode logic (CML) circuits are used because of their high frequency operation. Fig. 9 shows the operation principle of this logic family. The CML gates are fully differential, so they reject any common-mode noise created by the power supply or the ambient noise.

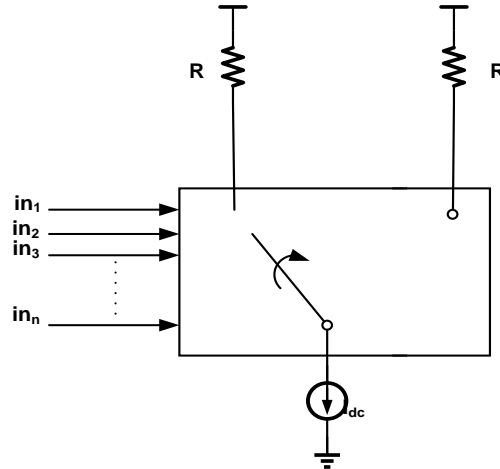


Fig.9 The CML circuit overview

There are some techniques to improve speed of CML circuits. In [16], [17], an inductor is added in series with the load resistor to extend the bandwidth. This inductor shunts the output capacitor and adds a zero to the frequency response. In fact, inductor steers the current to the capacitor and therefore reduces the rise time. This method is called inductive peaking.

Another way to increase the speed of CML circuits is to add an extra cross-coupled transistor pair to the outputs as shown in Fig. 10. The added cross-coupled transistors provide positive feedback which accelerates transition of output signals.

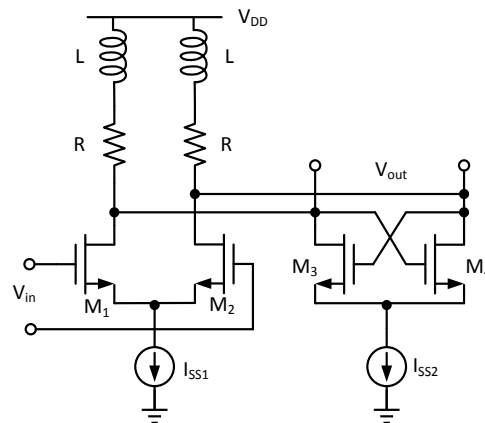


Fig.10 The two techniques for CML speed enhancement: shunt (inductive) peaking and cross coupled transistors

Figs. 11 shows latch circuit that is designed as a CML block and uses inductive peaking technique to enhance the speed.

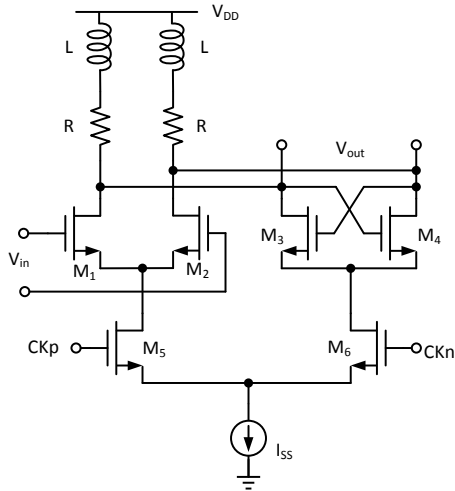


Fig.11 Implementation of latch

C. Reference PLL

As mentioned before, a reference PLL is used to provide a control voltage for the injection-locked main VCOs. The PLL circuit is depicted in Fig. 12. In this PLL a VCO that is identical to the main VCO is used to produce the required control voltage.

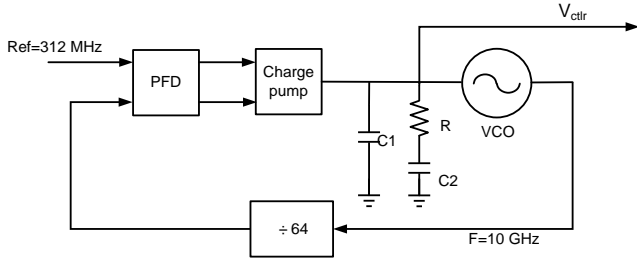


Fig.12 Reference PLL circuit

A 312MHz reference frequency is applied to a conventional PFD which compares its phase with the VCO output frequency and produces an up-down signal for the V/I converter that is followed by a second order loop filter. The V/I converter is shown in Fig. 13 [18]. The loop filter generates a proportional control voltage for tuning main VCO's frequency. A divider chain is placed in the feedback path that divides output of the VCO by a factor of 64.

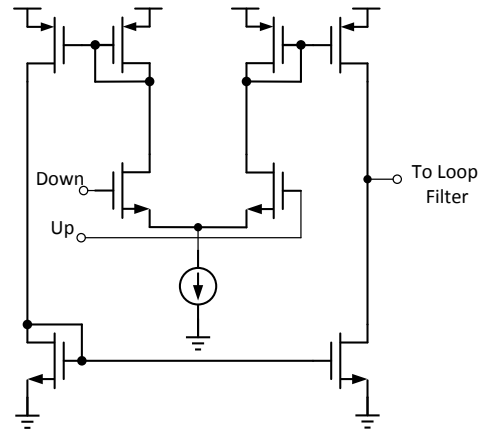


Fig.13 V/I converter

Since in this design, PLL must lock to a constant frequency, settling time and reference frequency magnitude is not of prime importance. By reducing the bandwidth of loop filter and choosing a relatively high reference frequency we can reduce VCO's control voltage ripples. A CML divider is used for the first two stages in the divider chain to work at high speed. For the next stages, dynamic dividers are designed as shown in Fig.14. This structure is a T flip flop that is made of two consecutive D flip flops (CML divide-by-two circuit is also made of two CML D latches combined to make a CML T flip flop). This divider consumes less power compared to CML circuits. These D flip flops are dynamic latches that sample the data in every rising edge of the clock. With the cross coupled PMOS configuration, the voltage of output nodes can change faster that enables the circuit operation at high speeds.

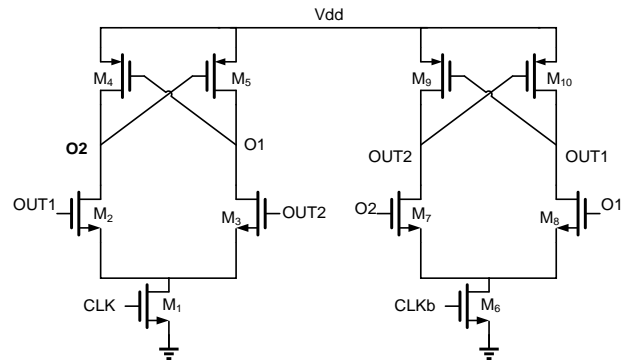


Fig.14 Dynamic frequency divider

IV. SIMULATION RESULT

The proposed circuit has been designed and simulated in a 0.18 μm CMOS technology. This circuit consumes 68.9 mW from a 1.8V supply voltage, where 38.6mW is consumed in the reference PLL and 30.3mW is consumed in the CDR core (including the two flip flops). As the performance (locking speed, etc) of the reference PLL does not have a large impact on the total system performance, the power consumption of

that PLL can be reduced to achieve an optimized design.

Fig. 15 depicts the reference PLL output clock spectrum and waveform. The spurs of the clock reference are approximately -60dBc. Also transient response of the VCO control voltage is represented in Fig. 16.

The input data is shown in Fig. 17(a) and the recovered data in response to a  $2^7-1$  continuous mode PRBS is shown in Fig. 17(b). The simulated jitter values for the recovered data are 4.8 ps, pp and 1.3 ps, rms. The recovered clock is shown in Fig. 18. The simulated peak-to-peak and rms jitters for the recovered clock are 2.4 ps,pp and 0.84 ps,rms, respectively. The VCO locking range for a fixed control voltage is achieved at 150 MHz. By using the reference PLL, the locking range of the CDR circuit is extended to 1 GHz. The CDR circuit recovers the data in less than 50 ps which is equal to 1 bit. Fig. 19 shows this fast locking time.

The circuit is simulated in different process corners, temperatures and supply voltages. Fig. 20 shows how the VCO frequency changes with PVT variations. In slow/slow process corner, 70° C and 1.65V, the rms and peak to peak jitter of the recovered clock are 1.07 ps and 3.2 ps, respectively. The consumed power in this situation is 60.7 mW and the circuit locks after 1 bits. In fast/fast corner, -20° C and 1.95 V, the rms and peak to peak jitter of the recovered clock are 0.86 ps and 2.43 ps, respectively. The consumed power is 83.8 mW and the circuit locks after 1 bits.

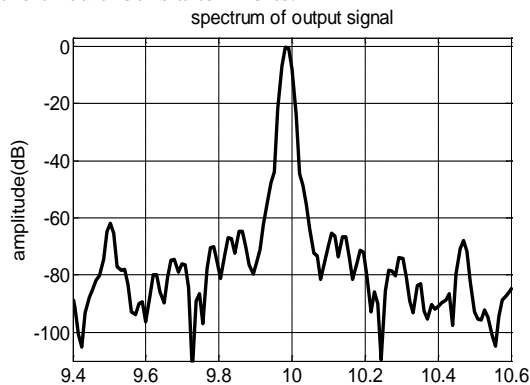


Fig.15 Spectrum of the reference PLL output

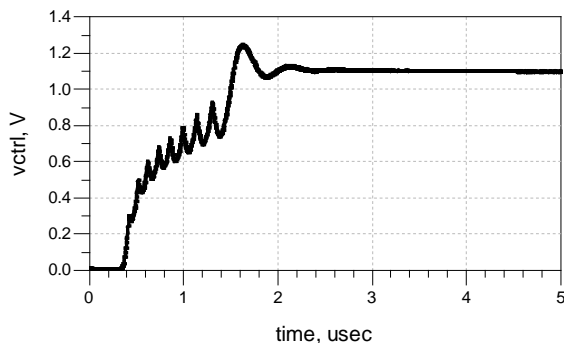


Fig.16 Control voltage of the VCO

design achieves a performance similar in speed to [8], while it uses a technology that is two nodes older than that of [8] and also consumes less power because of using half rate clock.

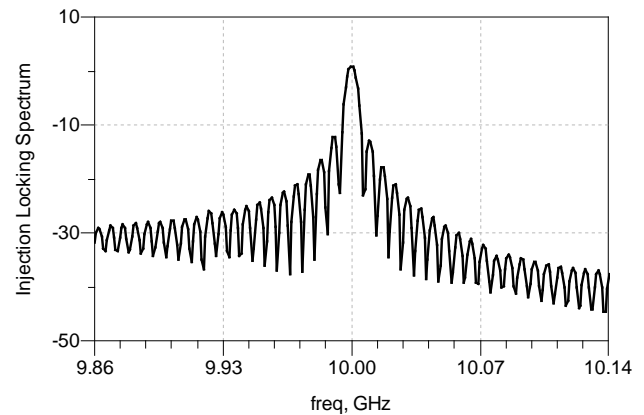
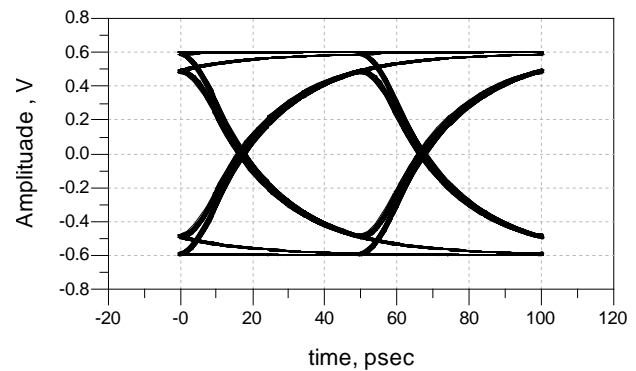
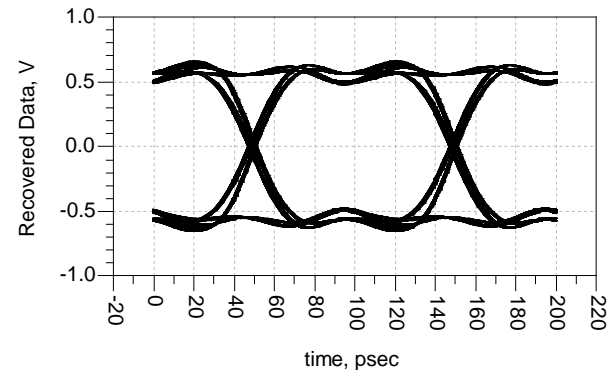


Fig. 17 Injection Locking Spectrum



(a)



(b)

Fig. 18 Data Eye diagram (a) at the CDR input (b) at the receiver output

Table 1 summarizes and compares the performance of this work and some other burst mode CDRs recently published in the literature. By using a super-harmonic ILO instead of first-harmonic ILO which can be seen from the table, the proposed

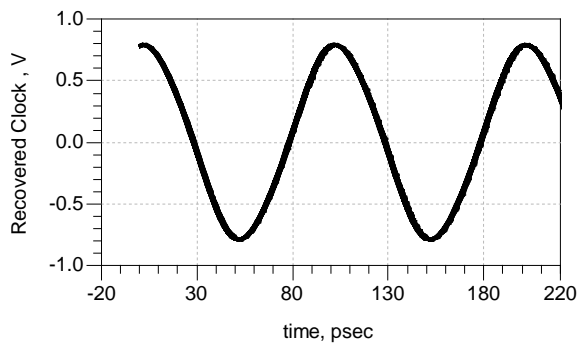
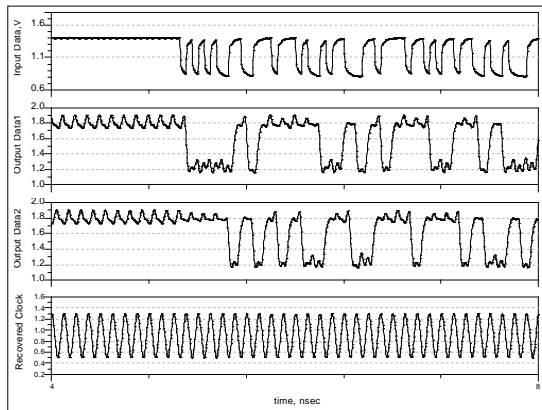
Fig. 19 Recovered clock with 20 Gb/s  $2^7$ -1 PRBS input data

Fig. 20 Simulated Input and Output Waveforms

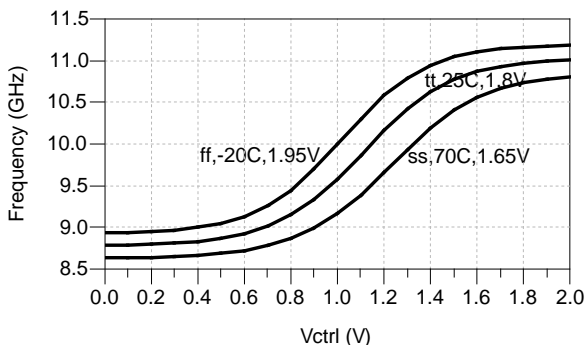


Fig. 21 VCO tuning curves for PVT variations

Table 1 The Measurement Results of similar works

	[7]	[19]
<b>Data Rate</b>	10 Gb/s	1.3-5.2 Gb/s
<b>Recovered Clock Jitter</b>	1.35 ps,rms (with $2^7$ -1 PRBS)	0.82 ps,rms (with $2^7$ -1 PRBS)
<b>Operation Range</b>	N/A	N/A
<b>Locking Time</b>	32UI	< 20UI
<b>Supply Voltage</b>	1.8 V	1.1 V
<b>Power Diss.</b>	200 mW	12.4 mW
<b>Technology</b>	0.18 $\mu$ m CMOS	40nm CMOS

Table 2 The Simulation Result of the proposed CDR compared with similar work

	[9]	This work
<b>Data Rate</b>	71 Gb/s	20 Gb/s
<b>Recovered Clock Jitter</b>	N/A	0.84ps,rms (with $2^7$ -1 PRBS)
<b>Operation Range</b>	N/A	1GHz
<b>Locking Time</b>	N/A	1UI
<b>Supply Voltage</b>	3.3 V	1.8 V
<b>Power Diss.</b>	0.5 W	68.9 mW
<b>Technology</b>	0.18 $\mu$ m SiGe	0.18 $\mu$ m CMOS

## V. CONCLUSION

A 20Gbps CDR circuit for burst mode applications is proposed and simulated in a 0.18 $\mu$ m CMOS process. Using super harmonic injection locking technique, frequency of the oscillator is reduced to the half of the bit rate, so two flip flops are needed for sampling the data with the half rate clock. To help CDR lock to the incoming data and track the frequency in the presence of PVT variations, a control voltage is made by a reference PLL and applied to the VCOs. Utilizing a new injection-locked oscillator as the VCO in this work allowed achieving the same high bit rate (20Gbps) in an older technology (i.e., 0.18  $\mu$ m CMOS) compared to the previously published work (in 90 nm CMOS).

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