Computationally Efficient Analytical Crosstalk Noise Model in RC Interconnects

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Abstract—This paper presents an accurate, fast and simple closed form solution to estimate crosstalk noise between two adjacent wires, using RC interconnect model in two situations: simple resistance as driver and short channel CMOS inverter as a driver. The salient features of our proposed models include minimization of computational overhead, elimination of adjustment step to predict the peak amplitude and pulse width of the noise waveform. Numerical calculations are compared with SPICE simulation and other metrics by plotting the noise voltage verses time. Based on our proposed models, we derive analytical delay models due to RC interconnect in each case. Finally we formulate energy dissipation of the RC coupled interconnects in both the cases using our proposed metrics. Experimental results indicate that our models are closely comparable by plotting the noise voltage verses time. Based on our proposed metrics, we derive analytical delay models due to RC interconnect in each case. Finally we formulate energy dissipation of the RC coupled interconnects in both the cases using our proposed metrics. Experimental results indicate that our models are closely comparable with SPICE simulation, with an average estimation error of 3.366%.

Keywords—Analytical Delay model, Crosstalk Noise, Energy Dissipation Estimation, Non-linear Driver, RC interconnects.

I. INTRODUCTION
In addition to the reduction in chip area, the scaling down of the feature size in deep submicron technology results in performance degradation of VLSI circuits such as logic failure, timing delay, unwanted coupling voltage between two adjacent wires. In the current technology, Crosstalk noise has become significant in the performance of VLSI circuits. Crosstalk noise exhibits a negative impact on the reliability of the VLSI circuits. Now it is time to VLSI designers to examine the crosstalk noise effects in their designs, so that they are free from noise. Cross talk noise modeling approaches are loosely classified into two categories based on their tradeoff between accuracy and efficiency [1]. They are analytical modeling and SPICE simulation. Analytical modeling is preferred because simulation using SPICE is always computationally expensive and time consuming, with the modern designs containing millions of transistors and wires. In addition, this estimation must be done at the early stage of the designs. Because detecting coupling induced problems at the late stage of the designs may implicate difficulties as most of the layout is completed and it may not be possible to modify floor planning, placement and routing at that stage [2]. Analytical modeling is developed based on two techniques, Elmore delay model and moment matching technique. Moment matching technique is quick to provide peak amplitude of noise voltage. However it has two drawbacks: Deriving solution is difficult, as it needs Laplace and inverse Laplace transform. Using Moment Matching method, it may take more than one day to complete the noise in a modern Micro Processor [3]. The summations of time constants is determined at each capacitor in the second technique, Elmore delay model. Devgan[4] & Heydari[5] proposed analytical models based on Elmore delay model. Analytical model of [4] is a simple mathematical expression to estimate the peak amplitude of the cross talk noise. However this model has several disadvantages: It is less accurate; it does not consider the parasitic parameters of aggressor net to compute crosstalk noise; it cannot provide complete time domain waveform. The model in [5] is a very effective mathematical model to estimate crosstalk noise voltage waveform in time domain. This metric considered the disadvantages of Devgan’s model. They computed time constant of RC interconnect model at each node by considering parasitic parameters of both aggressor and victim nets. Still this metric also has several drawbacks: They have adjusted the time constant of RC interconnect by multiplying with the time constant. Second, to compute noise voltage waveform in time domain, they considered Devgan’s result as the steady state value, which itself is highly inaccurate at an average error of 644%. Finally to compute crosstalk noise, it takes two iterations, i.e., One iteration to find time constant (τd) and another one to get steady state value by using Devgan’s metric. [6] proposed an accurate solution to crosstalk noise voltage waveform in time domain. This model addressed all the drawbacks of [5], namely adjustment of the time constant of RC interconnect by multiplying with the time constant; Passing two iterations to compute noise voltage and considering a highly inaccurate voltage as the steady state value. With reference to non-linear driver, the recent works are as follows: Huang [7] proposed a complete set of analytical models for signal delay, rise time and voltage overshoot for a non-linear driver based RC interconnect. But all their mathematical expressions are complex. Still their closed form expression for output voltage has considered only one region of operation for CMOS inverter. The main limitation of Huang’s metric is not considering: Coupling effects of adjacent wires and complete non-linear nature of CMOS inverter while deriving expressions for rise time and voltage waveform at the gate output. [8] presented a dual ramp driver model for RLC interconnect using piecewise approximation to the characteristics of CMOS inverter, which does not consider the complete range of operation of CMOS inverter. From above discussion, it is clear that the models of [7] & [8] do not provide complete non-linear nature of CMOS inverter. These models are likely to give large errors, while estimating crosstalk noise in a short channel CMOS inverter based RC interconnect. This paper presents two noise metrics: one is referred to linear driver as source and another one is based on non-linear driver, based on [6], which does not account for non-linear nature of the driver resistance. Our proposed models are closed form solutions to predict peak amplitude and pulse width of crosstalk noise voltage of an RC interconnect, which address all the drawbacks of previous metrics [4], [5], [7] & [8]. Our proposed noise metric, in the first case has a closed form expression, depends on circuit parameters of both aggressor and victim nets and rise (fall) time of the input signal. Our model presents a noise waveform in time domain which is further compared with SPICE simulation results. In the second
case, we propose a realistic mode, which accounts for non-linear driver and the time constant as in [6]. As our proposed mathematical expressions, to compute voltage at any node of aggressor victim net, need peak amplitude of its corresponding predecessor node of aggressor wire, it computes the voltage at that node with the same expression in the previous cycle and our results are closely matched with SPICE simulation results. This proposed second noise metric has a closed form expression, depends on circuit parameters of aggressor and victim nets, strength of the driver, rise time of aggressor and coupling capacitance between the two adjacent wires. As in the current technology, the interconnect effects like delay and energy dissipation due to crosstalk are significant, we subsequently investigate these effects elaborately. After obtaining analytical models for complete time domain noise voltage using those models, we develop analytical delay and energy dissipation estimation models due to RC interconnects.

Sections 2 reviews fundamentals of interconnects, Next Devgan’s metric & Heydari’s metric are discussed. Then we introduce our metric, referred to linear resistance as driver, then our non-linear driver based proposed metric is presented. Comparison between our models and SPICE simulations are explained. Our proposed analytical delay and energy dissipation estimation models are followed on each metric. Finally we present concluding remarks.

II. REVIEW OF INTERCONNECTS

In deep submicron technology, VLSI circuits usually consist of several parallel bus structures (collection of adjacent wires) result in significant parasitic coupling effects. These coupling effects produce interference, between signals is referred to as Crosstalk noise [9]. These effects may be capacitive or inductive. In this paper, we restrict our attention to only capacitive effects. Crosstalk effects can lead to logic failure, increased power dissipation and timing degradation in Digital system. Consider a two minimally separated adjacent wires as shown in Fig.1. A step input, with $t_r$, rise time is applied to aggressor net, which is propagated to the far end and is in the exponential shape due to the presence of $R_a$ and $C_a$. Though ‘0’ (GND) is applied to victim net, because of coupling capacitance $C_{cc}$, a cross talk noise voltage $V_V$ will be appeared at the far end of victim net, for a duration of ‘$t_p$’. The parasitic RC interconnect model of Fig.1 is given in Fig. 2.

Mathematically

$$V_V = V_{dd} \left(1 - e^{-t'/\tau}\right)u(t)$$

(1)

‘$\tau$’ is the time constant.

We first review Devgan’s & Heydari’s metrics and their drawbacks in estimating cross talk noise in RC circuits. Then we derive a new analytical expression to capacitive coupling model, which eliminates the drawbacks of Devgan’s & Heydari’s metrics.

A. Devgan’s Metric

To better understand this approach, consider a pair of capacitively coupled second order RC circuit, as shown in Fig.3. $R_{S1}$ & $R_{S2}$ represent the resistances of the input source, which are on resistances of line drivers.

Consider typical values of these parameters i.e., assume that
\[ C_1 = 60 \text{ fF}, \quad C_2 = 120 \text{ fF}, \quad R_2 = 100 \Omega, \quad R_1 = 20 \Omega, \quad C_c = 180 \text{ fF}, \quad R_{S1} = 100 \Omega, \quad R_{S2} = 150 \Omega, \quad t_r = 0.1 \text{ nsec}. \]

From the SPICE simulation, the reported value of voltage \( V_{22} \) is 0.3649 V.

Devgan’s metric for the same as follows

\[ V_{21,SS} = (2R_2 + R_{S2}) C_c (V_{DD}/t_r) \]  
\[ V_{22,SS} = (3R_2 + 2R_{S2}) C_c (V_{DD}/t_r) \]

Using (3) \( V_{22,SS} \) is 1.404V. The estimated error is 284.76 %. When the input signal rise time is small, the crosstalk waveform rolls down quickly and consequently error becomes unacceptably large.

**B. Heydari’s Metric**

The distributed RC model proposed by Heydari is shown in below Fig 4.

![Heydari’s Model of Distributed RC Interconnect.](image)

To compute the noise peak value, the capacitive crosstalk noise at every node of victim net is a rising exponential function during time interval of input.

\[ V_{2,MAX} = V_{2,SS} \left(1 - e^{-t_r/t_{dj}} \right) \]  
for \( j = 1, 2, \ldots, N \)

\( t_{dj} \) is the time constant of the \( j \)’th node voltage in the victim net and \( V_{2,SS} \), steady state crosstalk noise voltage measured using Devgan’s metric. The time constant at each node is equal to the summation of individual time constants due to each of the capacitances.

Considering \( 'z' \) as constant factor for the delay increase due to non-zero i.e., finite input value, which ranges in [1.00, 1.02], Payam has considered \( 'z' \) to be 1.09. Now time constant at node \( j \)

\[ t_{dj} = z [ R_{1,eq} C_{ij} + \sum_{k=1}^{j} (R_{1,eq} (C_{ck} + C_{1k}) + R_{2,eq} (C_{2k} + C_{ck})) ] \]

(5)

For \( j = 1, 2 \ldots, N \),

where \( R_{1,eq} = R_1(j) + R_{S1} \) & \( R_{2,eq} = R_2(j) + R_{S2} \)

As special case, consider two second order capacitively coupled RC network, as in Fig 4 and the same physical parameters.

Applying (4) & (5), the closed form expressions for peak value of the victim net are

\[ V_{21} = V_{21,SS} \left(1 - e^{-t_r/t_{d1}} \right) \]  
(6)

Where

\[ t_{d1} = z [ (R_1 + R_{S1}) (C_c + C_1) + (R_2 + R_{S2}) (C_c + C_2) ] \]

(7)

Applying the same physical parameters, considered for Devgan’s metric, \( V_{22} \) is computed to be 0.404 V. The estimated error is 10.71% compared SPICE simulation.

**C. New Metric for Crosstalk Estimation**

Careful investigation of these metrics and SPICE simulation shows that the computation of time constant is inaccurate. Mainly Heydari has done one adjustment by multiplying 1.09 (\( 'z' \)) to the calculated time constant. Another error in his metric is calculation of peak value of victim node is based on the steady state value, calculated using Devgan’s metric, which itself is 644% error, compared SPICE simulation. Further, to compute peak value of victim node, we must first find out steady state value using Devgan’s metric in first iteration, followed by computing peak value using (4), in the second iteration, which results in slow in computation. These three issues are mainly responsible for inaccuracy of Heydari’s metric to estimate cross talk noise.

In this paper, we propose a closed form solution to address all these issues and still more accurate solution than Heydari’s and Devgan’s metrics. Our contribution is mainly based on the following concept. The time constant due to each capacitance is obtained by calculating equivalent resistance seen across each capacitance, with all other capacitances open circuited. Consider the following equivalent circuit in Fig 5. The time constant at \( j \)’th node of aggressor net sees two capacitances \( C_1 \& C_c \), whereas \( j \)’th node of victim net sees two capacitances \( C_c \& C_2 \) and replace all other capacitances with open circuited. The circuit model is presented in Fig 5.

![Heydari’s Model of Distributed RC Interconnect.](image)

Hence the time constant of the \( j \)’th node of aggressor net, \( \tau_{aj} \) is given by

\[ \tau_{aj} = R_{1,j} C_{1,j} + C_{1,j} (R_1 + R_{2,eq}) \]

(8)

Where \( R_{1,j} \) is resistance of \( j \)’th node of aggressor net.

And the time constant of \( j \)’th node of victim net, \( \tau_{fj} \) is given by

\[ \tau_{fj} = R_{2,eq} (C_{1,j} + C_{2,j}) \]

(9)
Fig. 5. Equivalent Circuit Model to Compute Time-Constant of the j’th node of Aggressor and Victim nodes.

Where \( R_{2,jeq} \) is resistance of j’th node of victim net, which is equal to \((R_{2,j} + R_{5j})\).

By considering (8) & (9) and Fig 5, the voltages at the node of aggressor and victim nets are as follows

\[
V_{j,max} = V_{j-1,max}(1-e^{-t_{j}/\tau_{a}}) \quad (10)
\]

Where \( V_{j-1,max} \) is peak value of (j-1) node of aggressor net which is computed with same expression recursively considering \( \tau_{a} \) as in (8).

\[
V_{j,2max} = V_{1,max}(1-e^{-t_{j}/\tau_{v}}) \quad (11)
\]

The above expressions are much effective, simple and accurate to estimate peak values of voltages at aggressor and victim nets. To compute peak values of voltages at any node of aggressor & victim nets, these expressions need only the peak value at its predecessor node of aggressor net, unlike depends on steady state value using Devgan’s metric. These expressions eliminate the adjustment step also. Further this analytical model does not need steady state value using Devgan’s metric, to compute peak voltages at any node. Within one iteration, at all nodes of aggressor and victim nets can be computed using (10) & (11) recursively considering the respective time constants using (8) & (9). To verify the accuracy of our model to estimate voltages at aggressor and victim nets using (10) & (11), we consider second order RC network, with same parameters, as Devgan’s and Heydari’s metrics.

Our proposed second order RC model is presented in Fig. 6.

From (8) & (9), Time constant at first node of aggressor net is given by

\[
\tau_{a1} = (R_{1} + R_{S1})C_{1} + (R_{1} + R_{S1} + R_{2} + R_{S2})C_{C} \quad (12)
\]

Time constant at second node of aggressor net is given by

\[
\tau_{a2} = R_{1}C_{1} + (R_{1} + 2R_{2} + R_{S2})C_{C} + (2R_{1} + R_{S1})C_{01} \quad (13)
\]

Time constant at second node of victim net,

\[
\tau_{v} = (2R_{2} + R_{S2})(C_{C} + C_{2} + C_{02}) \quad (14)
\]

Finally from (11) & (12), the voltages at 1st and 2nd nodes of aggressor are given by

\[
V_{11} = V_{DD}(1-e^{-t_{f}/\tau_{a1}}) \quad (15)
\]

\[
V_{12} = V_{11}(1-e^{-t_{f}/\tau_{a2}}) \quad (16)
\]

Further the voltage at 2nd node of victim net is given by

\[
V_{22} = V_{12}(1-e^{-t_{f}/\tau_{v}}) \quad (17)
\]

The value of \( V_{22} \) computed to be = 0.379V. The estimation error of 3.86 % is reported, compared to SPICE simulation of \( V_{22} \).

To prove the consistency of our metric, we conduct an experiment on a multistage RC network, to compare Devgan, Heydari and our proposed models with SPICE simulation. We performed a number of experiments on a two line structure in a 130nm CMOS technology. The coupled length of adjacent interconnects are varied from 200µm to 5mm. The supply voltage is 1.3V. Results are reported for a range of rise time between 30 ps to 200 ps and victim and aggressor driver resistances vary between 20 Ω to 2.5 K Ω. Table I contains these comparisons. The mean and maximum error values are reported in Table I. Table I and II clearly show that high accuracy of our model compared to other approaches. Further, our proposed model results in an average estimation error of 3.36 %, compared to SPICE simulation. Our metric is reported to be better than Heydari’s metric, whose average estimation error is 51.28% and Devgan’s metric, whose average estimation error is 644%. It is evident that static CMOS logic circuit can sustain the signals, without any loss, in the presence of Crosstalk Noise. However, it tends to cause an increase in propagation delay on victim net.

The complete Noise Waveform can be as follows

\[
V_{2}(t) = V_{i}(1-e^{-t_{i}/\tau_{v}}) \quad 0 < t \leq t_{r}
\]

\[
V_{2}(t) = V_{2max}e^{(t-t_{i})/\tau_{v}} \quad t > t_{r} \quad (18)
\]

This expression gives complete picture about noise behavior. This closed form expression enables the designers to try alternative solutions to minimize noise. Fig.8. Compares our metric (18) with SPICE simulation and Heydari’s metric for capacitively coupled lines. Fig.7. shows the changes in crosstalk when the input rise time varies from 50 ps to 200 ps and all of geometric parameters are fixed. Fig.8 indicates that our plot is converging with the SPICE simulation at a particular instant of time. For long rise time Devgan’s metric predicts accurately the peak amplitude of noise. Heydari’s metric is best suited for lengthy interconnects. Finally, our metric is more accurate than the works done by Heydari & Devgan and is very close SPICE simulation.
Fig. 7. Crosstalk Noise waveform for two coupled transmission lines.

Fig. 8. Maximum Crosstalk Noise versus input rise-time

Table I
Results of simulation on the two capacitively Coupled transmission lines using T-SPICE and our Proposed metric

<table>
<thead>
<tr>
<th>$R_1$ KΩ/m</th>
<th>$Rs_1$ Ω</th>
<th>$R_2$ KΩ/m</th>
<th>$Rs_2$ Ω</th>
<th>$C_1$ pF/m</th>
<th>$C_2$ pF/m</th>
<th>$Cc$ pF/m</th>
<th>Spice volts</th>
<th>Ours volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.5</td>
<td>500</td>
<td>10.2</td>
<td>2500</td>
<td>60</td>
<td>64</td>
<td>100</td>
<td>0.094</td>
<td>0.096</td>
</tr>
<tr>
<td>9.3</td>
<td>75</td>
<td>10</td>
<td>150</td>
<td>92</td>
<td>80</td>
<td>170</td>
<td>0.356</td>
<td>0.325</td>
</tr>
<tr>
<td>17</td>
<td>325</td>
<td>17</td>
<td>335</td>
<td>140</td>
<td>100</td>
<td>200</td>
<td>0.245</td>
<td>0.241</td>
</tr>
<tr>
<td>12</td>
<td>190</td>
<td>8.5</td>
<td>100</td>
<td>85</td>
<td>75</td>
<td>140</td>
<td>0.183</td>
<td>0.159</td>
</tr>
<tr>
<td>9.55</td>
<td>527</td>
<td>9.6</td>
<td>400</td>
<td>72</td>
<td>72</td>
<td>150</td>
<td>0.191</td>
<td>0.186</td>
</tr>
<tr>
<td>8.2</td>
<td>270</td>
<td>7</td>
<td>240</td>
<td>83</td>
<td>90</td>
<td>160</td>
<td>0.188</td>
<td>0.183</td>
</tr>
<tr>
<td>10</td>
<td>625</td>
<td>10</td>
<td>750</td>
<td>120</td>
<td>120</td>
<td>132</td>
<td>0.197</td>
<td>0.2</td>
</tr>
<tr>
<td>15</td>
<td>800</td>
<td>15</td>
<td>550</td>
<td>108</td>
<td>108</td>
<td>200</td>
<td>0.163</td>
<td>0.166</td>
</tr>
<tr>
<td>13</td>
<td>270</td>
<td>20</td>
<td>250</td>
<td>130</td>
<td>100</td>
<td>220</td>
<td>0.201</td>
<td>0.204</td>
</tr>
<tr>
<td>9</td>
<td>26</td>
<td>15</td>
<td>550</td>
<td>97</td>
<td>30</td>
<td>120</td>
<td>0.433</td>
<td>0.425</td>
</tr>
<tr>
<td>7</td>
<td>37</td>
<td>16</td>
<td>500</td>
<td>100</td>
<td>14</td>
<td>100</td>
<td>0.379</td>
<td>0.399</td>
</tr>
<tr>
<td>11</td>
<td>160</td>
<td>11</td>
<td>140</td>
<td>90</td>
<td>90</td>
<td>120</td>
<td>0.17</td>
<td>0.164</td>
</tr>
<tr>
<td>17</td>
<td>20</td>
<td>17</td>
<td>150</td>
<td>140</td>
<td>100</td>
<td>200</td>
<td>0.414</td>
<td>0.407</td>
</tr>
<tr>
<td>8</td>
<td>1200</td>
<td>4</td>
<td>85</td>
<td>110</td>
<td>200</td>
<td>300</td>
<td>0.049</td>
<td>0.048</td>
</tr>
<tr>
<td>10</td>
<td>20</td>
<td>1.8</td>
<td>2000</td>
<td>70</td>
<td>20</td>
<td>95</td>
<td>0.484</td>
<td>0.487</td>
</tr>
</tbody>
</table>

Table II
Percentage Error Comparison of other metrics and Our Proposed Metric

<table>
<thead>
<tr>
<th>%Error Devgan</th>
<th>%Error Heydari</th>
<th>%Error Ours</th>
</tr>
</thead>
<tbody>
<tr>
<td>1283</td>
<td>427</td>
<td>2.12</td>
</tr>
<tr>
<td>335</td>
<td>1.4</td>
<td>8.71</td>
</tr>
<tr>
<td>536</td>
<td>2.04</td>
<td>1.6</td>
</tr>
<tr>
<td>555</td>
<td>19.12</td>
<td>13.1</td>
</tr>
<tr>
<td>623</td>
<td>22.51</td>
<td>2.6</td>
</tr>
<tr>
<td>644</td>
<td>18.61</td>
<td>2.65</td>
</tr>
<tr>
<td>625</td>
<td>48.73</td>
<td>1.5</td>
</tr>
<tr>
<td>679</td>
<td>57.66</td>
<td>1.84</td>
</tr>
<tr>
<td>593</td>
<td>8.9</td>
<td>1.49</td>
</tr>
<tr>
<td>248</td>
<td>23.32</td>
<td>1.8</td>
</tr>
<tr>
<td>259</td>
<td>79.15</td>
<td>5.27</td>
</tr>
<tr>
<td>693</td>
<td>2.94</td>
<td>3.5</td>
</tr>
<tr>
<td>267</td>
<td>5.07</td>
<td>1.69</td>
</tr>
<tr>
<td>2142</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>180</td>
<td>50.82</td>
<td>0.62</td>
</tr>
<tr>
<td>Average</td>
<td>644</td>
<td>51.28</td>
</tr>
<tr>
<td>Minimum</td>
<td>180</td>
<td>1.4</td>
</tr>
<tr>
<td>Maximum</td>
<td>2142</td>
<td>427</td>
</tr>
</tbody>
</table>
D. Our Proposed Metric for a Short Channel CMOS Inverter based RC Interconnect

In this section, we derive our model using short channel CMOS inverter as a driver. The RC interconnect model in this case is shown in Fig.9.

Consider Fig.9, aggressor inverter has \( L_{p1} : W_{p1} \) and \( L_{N1} : W_{N1} \) where as victim inverter has \( L_{p2} : W_{p2} \) and \( L_{N2} : W_{N2} \). \( V_{in} \) is applied input voltage with a \( t_f \) as fall time. \( R_a \) and \( R_f \) are wire resistances and \( C_a \) and \( C_f \) are corresponding ground capacitances of aggressor and victim nets respectively. \( C_c \) is coupling capacitance between aggressor and victim nets. Fig.10 illustrates the voltage waveforms at various nodes of aggressor & victim nets using SPICE simulation for Fig.9.

The Table III illustrates the complete behavior of CMOS inverter at different instants of time. In practice however, CMOS inverter undergoes five different operation regions, R1, R2, R3, R4 and R5 [10]. To predict noise voltage, \( t_1 \) is considered as the starting point. As CMOS inverter spends a short duration in R3 region, the third and fourth intervals are merged together [11]. Hence the regions of operation are confined to three. In Region ‘1’

\[
I_{dp} = \frac{W_p V_{sat} C_{ox} (V_{DD} - V_{in} - |V_{fp}|)^2}{(V_{DD} - V_{in} - |V_{fp}|) + E_{cp} L_p} \tag{20}
\]

\( V_g \) can be computed using (21)

\[
\frac{W_m \mu C_{ox}}{L_m} \left( \frac{V_{in} - V_{out}}{1 + \frac{V_{out}}{E_{cp} L_m}} \right) = \frac{W_m C_{ox}}{L_m} \left[ (V_{in} - V_{out}) \frac{V_{out}^2}{2} \right] = \frac{W_m V_{sat} C_{ox} (V_{DD} - V_{in} - |V_{fp}|)^2}{V_{DD} - V_{in} - |V_{fp}| + E_{cp} L_p} \tag{21}
\]

For a given \( V_{in} \), \( V_{out} \) can be computed, which is \( V_g \).
In Region ‘2’

\[ I_{dp} = \frac{W}{L} \frac{\mu}{E_{ox}} \left[ (V_{DD} - V_{in}) - V_{g} \right] \frac{V_{DD} - V_{sat}}{2} \]  \hspace{1cm} (22)

Now \( V_{g} \) can be computed, for a given \( V_{in}, V_{out} \) in (23), which is \( V_{g} \).

\[ \frac{W}{L} V_{sat} C_{ox} (V_{in} - V_{tn})^2 + E_{CN} L = I_{dp} \]  \hspace{1cm} (23)

\( I_{dp} \) is considered from (22) [9]

\[ t_1 = \frac{V_{DD} - |V_p|}{V_{DD}} t_f \]  \hspace{1cm} (24)

\[ t_2 = \frac{V_{DD}}{V_{out} + V_p} t_f \]  \hspace{1cm} (25)

\[ t_3 = \frac{V_{tn}}{V_{DD}} t_f \]  \hspace{1cm} (26)

\( \mu_n \) - Mobility of electrons

\( \mu_p \) - Mobility of holes

\( C_{ox} \) - Gate oxide capacitance per unit area

\( E_{CN} \) - Electric field for electrons

\( E_{CP} \) - Electric field for holes

\( V_{sat} \) - Velocity of saturation

\( V_{tn} \) - Threshold Voltage of NMOS Transistor

\( V_{sp} \) - Threshold Voltage of PMOS Transistor

After discussing transistor completely, the next step is modeling its ‘RC’ effects of CMOS Inverter in different regions of operation. The Resistance of transistor can be modeled over a range of time (\( t_1, t_2 \) ) [10]

\[ R_{eq} = \frac{1}{2} \left[ R_{dp}(t_1) + R_{dp}(t_2) \right] \]  \hspace{1cm} (27)

\[ = \frac{1}{2} \left[ \frac{V_{ddp}(t_1)}{I_{dp}(t_1)} + \frac{V_{ddp}(t_2)}{I_{dp}(t_2)} \right] \]  \hspace{1cm} (28)

**TABLE IV**

Equivalent RC Modeling of CMOS inverter

\[ R_{eq} = R_{dp} \] & \[ C_{eq} = \sum C \] \hspace{1cm} (29)

The equivalent resistance & Capacitance of the CMOS inverter are modeled in three different regions of operation during the interval \( \left( t_1, t_2 \right) \), as given in Table IV [9]. Now the RC interconnect circuit is simplified as in Fig.11.

The time constant due to each node is obtained by computing equivalent resistance seen across each capacitance, with all capacitances open circuited. The time constant at the node \( V_v \) is equal to in [6]

\[ \tau = R_{eq} \left[ C_{eq} + C_{eq} + C_{eq} + C_{eq} + C_{eq} + C_{eq} + C_{eq} + C_{eq} + C_{eq} + C_{eq} \right] \]  \hspace{1cm} (30)

The voltage at victim node is given by

\[ V_v = V_{DD} \left( 1 - e^{-\frac{t}{\tau}} \right) \]  \hspace{1cm} (31)

The above expression is much effective and accurate to estimate voltages at aggressor and victim nets in time domain. To compute peak value, this expression needs only time constant. Within one iteration, voltage at the victim net can be computed using (31) considering (30) as time constant. We demonstrate the accuracy of our model by conducting an experiment with the following 0.18µm technology specifications.

\( \mu_n = 670 \text{ cm}^2 / \text{v} - \text{s} ; C_{ox} = 1.6 \text{ fF/cm}^2 \)

\( \mu_p = 250 \text{ cm}^2 / \text{v} - \text{s} ; E_{CN} = 0.476 \text{ V} \)

\( V_{tn} = 0.2 \text{ V} ; V_{sp} = -0.2 \text{ V} ; E_{CP} = 1.28 \text{ V} \)

\( V_{sat} = 8 \times 10^6 \text{ cm} / \text{s} ; V_{DD} = 2.5 \text{ V} \)

\( L = 0.25\mu m ; W_{N1} = 5\mu m ; W_{P1} = 10\mu m ; \quad W_{N2} = 5\mu m ; W_{P2} = 10\mu m \);
The circuit behavior is modeled and tabulated in TABLE V.

TABLE V
Sample Experiment Data

<table>
<thead>
<tr>
<th>$V_{in}$ (V)</th>
<th>$R_1$</th>
<th>$R_2$</th>
<th>$R_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.3</td>
<td>0.8</td>
<td>0.8</td>
<td>0.2</td>
</tr>
<tr>
<td>0.2</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$V_{DD}$ (mV)</th>
<th>$I_{disp}$ ($\mu$A)</th>
<th>$R_{eq1}$ (K$\Omega$)</th>
<th>$C_{eff1}$ (fF)</th>
<th>$t$ (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>117</td>
<td>13.43</td>
<td>46</td>
<td>0.37</td>
</tr>
<tr>
<td>0.19</td>
<td>420</td>
<td>0.19</td>
<td>620</td>
<td>0.68</td>
</tr>
<tr>
<td>1.91</td>
<td>80</td>
<td>0.71</td>
<td>185</td>
<td>0.68</td>
</tr>
<tr>
<td>0.28</td>
<td>279</td>
<td>279</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>0.42</td>
<td>279</td>
<td>279</td>
<td>1.68</td>
<td>1.68</td>
</tr>
</tbody>
</table>

$V_{t} = V_{DD}(1 - e^{-\frac{t}{\tau_1}})$

$t_1 < t \leq t_2$

$V_{t} = V_{DD}(1 - e^{-\frac{t}{\tau_2}})$

$t_2 < t \leq t_3$

$V_{t} = V_{DD}(1 - e^{-\frac{t}{\tau_3}})$

$t_3 < t \leq t_{gr} + \frac{t_f}{2}$

$V_{peak} = V_{DD} e^{-\frac{t}{\tau_4}}$

$t > t_{gr} + \frac{t_f}{2}$ (32)

$V_{peak}$ is the peak value at the far end node of victim net at

$t = \frac{t_f}{2} + t_{gr}$. The time constants at different intervals $\tau_{v1}$, $\tau_{v2}$, $\tau_{v3}$, and $\tau_{v4}$ are computed using (30), by substituting the corresponding R&C values of Short Channel CMOS Inverter, from Table IV. Using (32), we can estimate the complete noise behavior in time domain. Fig.12 is the comparison of our metric with SPICE Simulation.

Results of Simulation on the two Capacitively Coupling Short Channel CMOS Inverter Based RC Interconnect model Using TSPICE and Our Metric.

<table>
<thead>
<tr>
<th>$P_1$</th>
<th>$N_1$</th>
<th>$N_2$</th>
<th>$R_a$</th>
<th>$C_a$</th>
<th>$C_v$</th>
<th>$C_C$</th>
<th>$C_{L1}$</th>
<th>$C_{L2}$</th>
<th>$spic$</th>
<th>$OU$</th>
<th>$R$</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>20</td>
<td>20</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>420</td>
<td>439</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>40</td>
<td>40</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>248</td>
<td>265</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>40</td>
<td>40</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>358</td>
<td>368</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>20</td>
<td>20</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>566</td>
<td>599</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>20</td>
<td>40</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>361</td>
<td>376</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>40</td>
<td>20</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>235</td>
<td>276</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>40</td>
<td>40</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>392</td>
<td>405</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>80</td>
<td>80</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>221</td>
<td>228</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>40</td>
<td>40</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>409</td>
<td>415</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>40</td>
<td>80</td>
<td>28.5</td>
<td>300</td>
<td>300</td>
<td>400</td>
<td>0.82</td>
<td>0.5</td>
<td>258</td>
<td>248</td>
<td></td>
</tr>
</tbody>
</table>
E. Analytical Delay Models

We now develop analytical 50% delay model for RC interconnect using our proposed models (16) and (32). The 50% delay is defined as the time difference between 50% points of the input and far-end output of the aggressor net. Equating the aggressor far end voltage to 0.5Vdd in (16) and (32) and determine ‘t’, which is denoted as \( t_a \) followed by

\[
50\% \text{Delay} = t_a / 2 - t_a \tag{33}
\]

Our proposed delay models for linear and non-linear driver are validated with different line parasitics as in Table VIIA & VIIB respectively. The maximum, minimum and mean estimation errors are

E. Analytical Energy Dissipation Model

Consider Fig.6, the source of energy dissipation in all the capacitors is \( V_{dd} \) through \( R_a \), as the adjacent wire is quiet. Hence we find the energy dissipation in the low to high transition of the input source is [12] by

\[
E_{L \rightarrow H} = \int_{0}^{T/2} \frac{[V_{dd} - V_a(t)]^2}{R_a} dt \tag{34}
\]

In (34) the voltage drop across the resistor can be computed by applying KVL in Fig.6 as follows.

\[
V_{dd} - V_a(t) = e^{-t/T} V_{dd} \tag{35}
\]

The energy dissipation in all the capacitors through \( R_a \) over an interval of \((0, T/2)\) is given by

\[
E_{L \rightarrow H} = \frac{V_{dd}^2}{2R_a} \left( 1 - e^{-T/T} \right) \tag{36}
\]

Using (36), we can find the energy dissipation by all capacitors in linear and non-linear resistance based drivers for an interval \((0, T)\), which are tabulated for different line parasitics in Table VIIA & VIIIB. To take combined effect of delay and energy dissipation due to RC interconnect, we introduce a new performance metric, Energy-50% Delay Product (EDP). Fig.14 and Fig.15 show EDP per clock cycle of an RC interconnect with linear driver and non-linear driver respectively.

<table>
<thead>
<tr>
<th>Table VIIA</th>
<th>Results of Delay and Energy dissipation due to RC interconnect with linear resistance as driver.</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_1 ) KΩ/m</td>
<td>( R_s ) Ω</td>
</tr>
<tr>
<td>11</td>
<td>500</td>
</tr>
<tr>
<td>9</td>
<td>75</td>
</tr>
<tr>
<td>17</td>
<td>325</td>
</tr>
<tr>
<td>12</td>
<td>190</td>
</tr>
<tr>
<td>9</td>
<td>527</td>
</tr>
<tr>
<td>8</td>
<td>270</td>
</tr>
<tr>
<td>10</td>
<td>625</td>
</tr>
<tr>
<td>15</td>
<td>800</td>
</tr>
<tr>
<td>13</td>
<td>270</td>
</tr>
<tr>
<td>9</td>
<td>26</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table VIIB</th>
<th>Results of Delay and Energy dissipation due to RC interconnect with non-linear resistance as driver.</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_a ) &amp; ( R_v ) KΩ/m</td>
<td>P1</td>
</tr>
<tr>
<td>11</td>
<td>40</td>
</tr>
<tr>
<td>9</td>
<td>40</td>
</tr>
<tr>
<td>17</td>
<td>80</td>
</tr>
<tr>
<td>12</td>
<td>80</td>
</tr>
<tr>
<td>9</td>
<td>80</td>
</tr>
<tr>
<td>8</td>
<td>40</td>
</tr>
<tr>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td>15</td>
<td>80</td>
</tr>
<tr>
<td>13</td>
<td>100</td>
</tr>
<tr>
<td>9</td>
<td>100</td>
</tr>
</tbody>
</table>
III. Conclusion

We proposed accurate closed form solutions to obtain Crosstalk Noise Voltage waveform in time domain for an RC interconnect in two cases. We addressed main drawbacks of Devgan’s and Heydari’s metrics, such as, adjustment to compute time constant of RC network and considering inaccurate value as steady state value using Devgan’s metric in calculating peak amplitude of crosstalk. Further, our model reduces the computational overhead, as it takes one iteration to find peak amplitude of crosstalk noise at any node of aggressor and victim nets. Further we developed another model to handle non-linear resistance as the driver. We have considered the short channel effects of the CMOS transistors in this case. Results show that our metric captures the noise waveform shape well and yield an average estimation error of 3.366 % for noise peak over a wide range, in the linear driver case and 5.3% in the non-linear driver case. We applied our analytical models to derive analytical delay and energy estimation models. Finally, we conclude that our RC interconnect models are accurate, fast and real time solution for the signal integrity issue in complex wiring system.

REFERENCES

P.Chandra Sekhar received his Post Graduation in 1999 from JNTU, Hyderabad, India in Digital Systems Specialization. He is currently working toward the Ph.D. Degree in the area of high performance VLSI integrated Circuit Design.

He was technical consultant in a manufacturing company of analytical chemical instruments from 1991 to 1999. Then he worked as Assistant Professor in Vagdevi Engineering College, India from 1999 to 2001. Since 2001 he is serving as Assistant Professor in Department of ECE, Osmania University, India. His research interests include analytical modeling of interconnect effects and development of CAD tools.


He joined Avionics Design Bureau, Hindustan Aeronautics Limited, Hyderabad, India in 1977 and was involved as a researcher in the design and the development of communication equipment. Since 1991, he is serving as faculty member Department of ECE, Osmania University, India and teaching regular academic courses (B.E., M.E. and Ph.D.)in VLSI design and Digital communication.