Low Voltage Low Power FGMOS based Voltage Differencing Transconductance Amplifier and Its Applications

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ABSTRACT
This paper presents a low voltage low power configuration of voltage differencing transconductance amplifier based on floating gate MOSFET. The proposed VDTA variant operates at supply voltage ±0.7 V with total static power dissipation of 90 µW due to low voltage feature of floating gate MOSFET. The circuit maintains the acceptable bandwidth of 173 MHz with increase linear input voltage range. Two applications have been presented to demonstrate the effectiveness of the proposed active block. A novel first order differential all pass filter employing a single FGMOS based VDTA and three capacitors has been implemented. This filter exhibits low THD of output signal and can be tuned by bias current. As another application, voltage mode dual input and dual output filter has been discussed to realize low, high and band pass filter functions. The band pass filter is tunable over frequency range from 98.4 MHz to 3.37 MHz. The simulations are accomplished using SPICE and TSMC 180 nm CMOS technology to validate the efficacy of the proposed circuit.

Keywords: Floating gate MOSFET; voltage differencing transconductance amplifier; low voltage; low power.

1. INTRODUCTION

The profound demand of portable electronic devices and scaling of technology have impelled researchers to develop low voltage analog signal processing circuits. Various low voltage analog techniques including bulk driven, self-cascode, sub-threshold MOSFETs, floating gate MOSFETs [1]-[7] exist in literature to design low voltage analog systems while meeting design specifications. FGMOSFET is the most suitable technique for low voltage low power analog applications as it reduces the dependency on threshold voltage. The supply voltage and power dissipation can be reduced in applications using floating gate MOSFET technique. Various analog signal processing circuits have been designed using a number of new active elements [8]-[21]. The behavioral model of various new active elements is reported in [8]. One of the active element mentioned in [8] is voltage differencing transconductance amplifier (VDTA) which is formed by replacing current differencing unit of current differencing trans conductance amplifier (CDTA) by voltage differencing unit thereby enhancing the electronic tunability of the circuit. VDTA can be used in voltage as well as transconductance based applications as it possesses two different values of trans conductance along with current outputs while input applied is differential voltage. Various applications based on VDTA are reported in [22,23]. The simple CMOS realization of VDTA proposed by Yesil et al .[15] is quite interesting but lacks in low power feature of an active element. Therefore, the objective of this paper is to propose a modified VDTA using FGMOS technique working at low supply voltage with reduced power consumption. Two applications of FGMOS based VDTA have been realized in this paper. A new first order differential all pass filter is implemented using a single FGMOS VDTA and three capacitors. Another application is voltage mode biquad filter exhibiting low, high and band pass filter functions. It is designed using a single FGMOS VDTA and two capacitors.

Section II of the paper gives the basic of FGMOS transistor and its operation. The new low power FGMOS based VDTA is explained in section III. Both applications of FGMOS based VDTA is implemented in section IV. Simulation results and comparison are given in section V followed by conclusion in section VI.

2. FLOATING GATE MOSFET

Floating gate MOSFET is a low voltage analog design technique. It has a floating gate with n number of inputs. Two layers of polysilicon are used to form first and secondary gates. Fig. 1 shows the FGMOS with N input and its equivalent circuit considering all capacitances and connections.

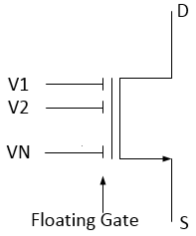

Figure 1 (a). Floating gate MOSFET with N inputs

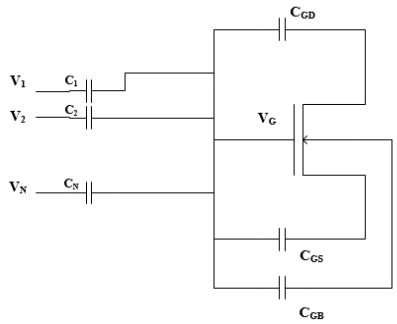

Figure 1 (b). Equivalent circuit floating gate MOSFET

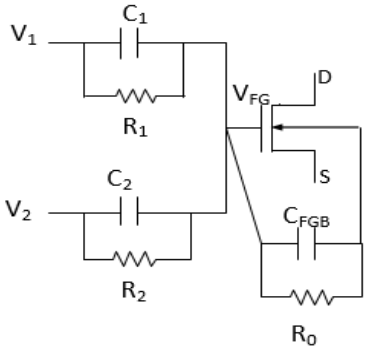

Figure 1 (c). Model of floating gate MOSFET with two inputs

The capacitance of FGMOSFET can be given as a sum of all capacitances CN where it ranges from 1 to N including capacitance at floating gate as well as parasitic capacitance present in the MOSFET. The voltage at floating gate is VFG and expressed in equation (2) after assuming that there is isolation at floating gate and Vi are the inputs voltages and QFG is amount of charge trapped in FGMOS while fabricating it.

$$CT = CGB + CGD + CGS + \sum_{i=1}^{N} CN \quad (1)$$

$$VFG = \sum_{i=1}^{N} \frac{Ci}{CT} + \frac{CGSVD}{CT} + \frac{CGSVS}{CT} + \frac{QFG}{CT} \quad (2)$$

The current of FGMOS transistor operating in linear and saturation region are expressed as

$$ID = \frac{\mu CoxW}{2L}\left(\left(\sum_{i=1}^{N} \frac{CiViS}{CT} + \frac{CGDVDS}{CT} + \frac{CGBVBS}{CT} + \frac{QFG}{CT} - VT\right)VDS - \frac{VDS^2}{2}\right) \quad (3a)$$

$$ID = \frac{\mu CoxW}{2L}\left(\sum_{i=1}^{N} \frac{CiViS}{CT} + \frac{CGDVDS}{CT} + \frac{CGBVBS}{CT} + \frac{QFG}{CT} - VT\right)^2 \quad (3b)$$

The aspect ratio and threshold voltage of FGMOS are W/L and VT and VS,VD,VB are terminal voltages of FGMOS at terminals.

If we assume that the sum of all capacitances Ci very large compared to parasitic capacitances CGD, CGB and QFG, then the equations 3(a) and 3(b) can be simplified as

$$ID = \frac{\mu CoxW}{2L}\left(\left(\sum_{i=1}^{N} \frac{CiViS}{CT} - VT\right)VDS - \frac{VDS^2}{2}\right) \quad (4a)$$

$$ID = \frac{\mu CoxW}{2L}\left(\sum_{i=1}^{N} \frac{CiViS}{CT} - VT\right)^2 \quad (4b)$$

The macro model of FGMOS transistor [6] given in the fig. 1(c) is used to simulate it to overcome the issue of dc convergence. A resistor of large value is connected in parallel with each capacitor to form floating gate inputs and the condition to be fulfilled is Ri = 1/((kCi)= 1000 GΩ where k is the transconductance parameter and Ci is the respective input capacitance value.

3. PROPOSED FGMOS BASED VDTA

The novel low voltage implementation and circuit symbol of the FGMOS based VDTA is shown in the figure 2 and 3. Two transconductance stages [23] with two floating gate MOSFETs in each stage are utilized to realize the circuit. The two input FGMOSFET is implemented as mentioned in [24]. The proposed block exhibits salient features such as low quiescent power dissipation while maintaining acceptable bandwidth .

The differential input voltage is applied at V_P and V_N of the first transconductance stage and transformed to current I_Z at terminal z by transconductance gain of first stage. The intermediate voltage at terminal Z contributes to currents at terminals x+ and x- by transconductance gain of second stage. Both transconductance gains are electronically tunable by bias currents available externally. The terminal relationship of VDTA is described below :

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_p \\ V_n \\ V_z \end{bmatrix}$$

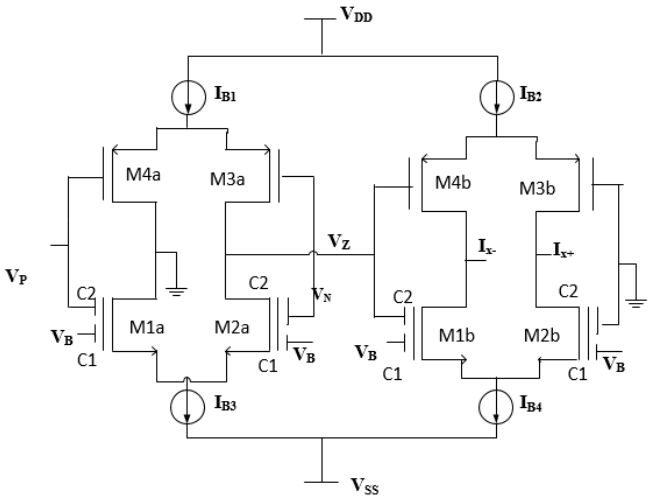

Figure 2: FGMOS VDTA implementation

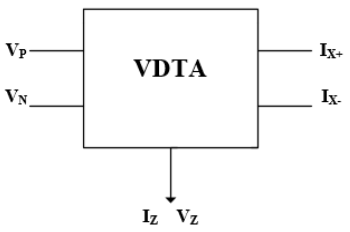

Figure 3 : Symbol of VDTA

By using the analysis in mentioned in [23] and in equation XX, the input and output small signal transconductance are found to be:

$$g_{ma} = \left(\left(\frac{C_1/C_T g_{m1a} * C_2/C_T g_{m2a}}{C_1/C_T g_{m1a} + C_2/C_T g_{m2a}}\right) + \left(\frac{g_{m3a} * g_{m4a}}{g_{m3a} + g_{m4a}}\right)\right) \quad (5)$$

$$g_{mb} = \left(\left(\frac{C_1/C_T g_{m1b} * C_2/C_T g_{m2b}}{C_1/C_T g_{m1b} + C_2/C_T g_{m2b}}\right) + \left(\frac{g_{m3b} * g_{m4b}}{g_{m3b} + g_{m4b}}\right)\right) \quad (6)$$

C_1 and C_2 are input capacitances of transistors M_1 and M_2 of both stages and C_T is the total capacitance as shown in the equation 1.

where gi is defined as the transconductance of a transistor and given by equation 7

$$gi = \sqrt{I_{Bi} \cdot \mu . C_{ox} \cdot \frac{Wi}{Li}} \quad (7)$$

IB is the bias current of ith transistor, μ is the mobility of either nmos or pmos transistor, Cox is gate oxide capacitance per unit area and W/L is aspect ratio of ith transistor.

The output impedance of the circuit at output stage is given as

$$r_{out} = \left(\left(\frac{C_1/C_T g_{m1b} C_1/C_T g_{m2b} g_{m3b} g_{m4b}}{C_1/C_T g_{m1b} C_1/C_T g_{m2b} (g_{m3} + g_{m4b})}\right) + (C_1/C_T g_{m1b} + C_1/C_T g_{m2b}) g_{m3b} g_{m4b}\right) \quad (8)$$

After simplification, the above expression is

$$r_{out} = \left(\left(\frac{g_{m1b} g_{m2b} g_{m3b} g_{m4b}}{g_{m1b} g_{m2b} (g_{m3} + g_{m4b})}\right) + (g_{m1b} + g_{m2b}) g_{m3b} g_{m4b}\right) \quad (9)$$

Thus, the circuit maintains the high output conductance at output stage while lowering the supply voltage.

4. APPLICATIONS OF FGMOS BASED VDTA

4.1 First Order Differential All Pass Filter

A new differential first order all pass filter is proposed in this section. It is implemented using on a single FGMOS VDTA and three capacitors as illustrated in the figure 4. V_1 and V_2 are the input signals applied at input terminals of FGMOS based VDTA and V_{id} is the difference of input voltages V_1 and V_2 . The output voltage V_o and output current I_o are obtained from output terminals x- and x+ respectively.

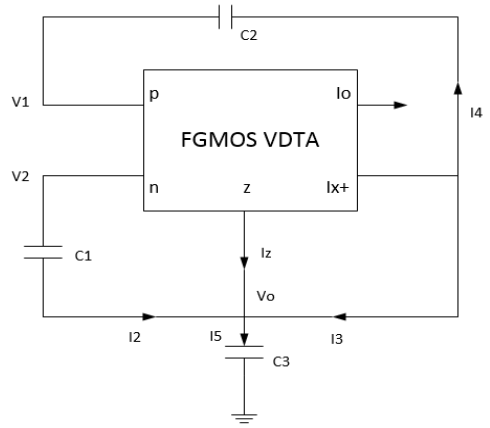

Figure 4. FGMOS VDTA based first order differential all pass filter.

According to KCL and routine analysis, the current Iz is expressed as

$$I_1 + I_2 + I_3 - I_5 = 0 \quad (10)$$

Using the properties of VDTA, the simplified equation is

$$gm_1V_2 - gm_1V_1 + sC_1(V_1 - V_o) + sC_2(V_o - V_2) - gm_2V_o - sC_3V_o = 0 \quad (11)$$

Assuming that all three capacitors are equal,

$$-gm_1(V_1 - V_2) + sC(V_1 - V_2) - gm_2V_o - sCV_o = 0 \quad (12)$$

$$(sC - gm_1)(V_1 - V_2) - gm_2V_o - sCV_o = 0 \quad (13)$$

$$(sC - gm_1)(V_1 - V_2) = (sC + gm_2)V_o \quad (14)$$

$$\frac{V_o}{(V_1 - V_2)} = \frac{(sC - gm_1)}{(sC + gm_2)} \quad (15)$$

Consider $gm_1 = gm_2$ for simplification,

$$\frac{V_o}{(V_{id})} = \frac{(sC - gm)}{(sC + gm)} \quad (16)$$

$$I_o = I_{x+} = gm_2V_o \quad (17)$$

$$\frac{I_o}{(V_{id})} = gm_2\frac{(sC - gm)}{(sC + gm)} \quad (18)$$

The phase response, voltage gain and transconductance gain of this differential all pass filter is

$$\Phi(\omega_p) = \pi - 2\tan^{-1}\left(\frac{\omega pC}{gm}\right) \quad (19)$$

$$\left|\frac{V_o}{(V_1-V_2)}\right| = \left|\frac{V_o}{(V_{id})}\right| = 1 \quad (20)$$

$$\left|\frac{I_o}{(V_{id})}\right| = gm \quad (21)$$

which further can be written as

$$\left|\frac{I_o}{(V_{id})}\right| = \sqrt{I_B \mu C_{ox}(W/L)} \quad (22)$$

and the pole frequency is

$$\omega_p = \left(\frac{C}{\sqrt{I_B \mu C_{ox}(W/L)}}\right) \quad (23)$$

The sensitivities w.r.t ωp are mentioned below.

$$S_{IB}^{wp} = 1.5\,,\ S_C^{wp} = -1 \quad (24)$$

4.1.1 Non-Ideal Analysis

The effect of parasitic impedances and voltage and current tracking errors on performance of differential all pass filter is discussed in this section. Non- ideal terminal relationship of FGMOS VDTA is given below:

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} \alpha_p g_{m1} & \alpha_n g_{m1} & 0 \\ 0 & 0 & \beta g_{m2} \\ 0 & 0 & -\beta g_{m2} \end{bmatrix} \begin{bmatrix} V_p \\ V_n \\ V_z \end{bmatrix}$$

where α_p and α_n are errors in transconductance gain from p and n terminals to z terminal. β denotes the error in the transconductance gain from z to x terminal.

Parasitic effects

Assume that the parasitic impedances at terminals p,n,z and x are R_p, C_p R_n, C_n ,R_z, C_z ,R_x and C_x respectively. Ci is the summation of parasitic capacitances at n, z and x terminals and Gi is addition of conductance at n, z and x terminals. Considering these impedances, the modified voltage and current transfer functions are:

$$\frac{V_o}{(V_{id})} = \frac{(sC-\alpha_n gm_1)}{(s(C+Ci)+Gi+\beta gm_2)} \quad (25)$$

$$\frac{I_o}{(V_{id})} = \beta gm_2\left(\frac{(sC-\alpha_n gm_1)}{(s(C+Ci)+Gi+\beta gm_2)}\right) \quad (26)$$

The pole frequency, phase response and voltage gain due to modified expressions are:

$$\omega p = \left(\frac{Gi+\alpha_n gm}{C+Ci}\right) \quad (27)$$

$$\Phi(\omega_p) = \pi - 2\tan^{-1}\left(\frac{\omega pC}{\alpha_n gm}\right) - 2\tan^{-1}\left(\frac{\omega p(C+Ci)}{Gi+\beta gm2}\right) \quad (28)$$

$$\left|\frac{V_o}{(V_{id})}\right| = \frac{\sqrt{(\omega pC)^2-(\alpha_n gm)^2}}{\sqrt{(\omega p(C+Ci))^2+(Gi+\beta gm2)^2}} \quad (30)$$

It can be seen that parasitic impedances affect pole frequency, phase response and voltage gain.

4.2 Universal Biquad Filter using FGMOS VDTA

The voltage mode biquad filter is implemented using the proposed FGMOS based VDTA and two capacitors as shown in the fig. 3.2. The filter has two inputs and two outputs. Low pass, high pass and band pass functions are realized using this filter with condition mentioned in the table 1

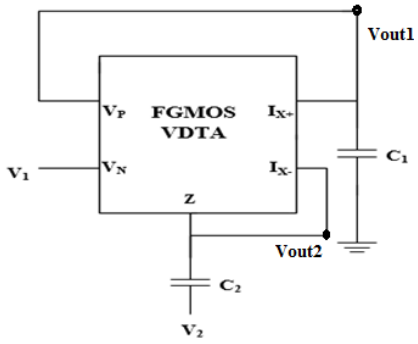

Figure 5. FGMOS VDTA based LP,HP, BP filters implementation

Table 1 Input conditions for biquad filter.

Input Conditions	**Filter Function**
V1= Vin, V2=0	Low Pass, Band Pass
V1=0, V2= Vin	High Pass, Band Pass

The respective transfer functions according to the input conditions can be given as

For $V_1 = V_{in}$ and $V_2 = 0$

$$\frac{V_{out2}}{V_{in}} = \frac{sC_1 g_{m1}}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}} \text{ ; BP filter function} \quad (32)$$

$$\frac{V_{out1}}{V_{in}} = \frac{g_{m1}g_{m2}}{s^2 C_1C_2 + sC_1g_{m2} + g_{m1}g_{m2}}$$; LP filter function (33)

For $V_2 = V_{in}$ and $V_1 = 0$

$$\frac{V_{out1}}{V_{in}} = \frac{sC_2g_{m2}}{s^2 C_1C_2 + sC_1g_{m2} + g_{m1}g_{m2}}$$; BP filter function (34)

$$\frac{V_{out2}}{V_{in}} = \frac{s^2 C_1C_2}{s^2 C_1C_2 + sC_1g_{m2} + g_{m1}g_{m2}}$$; HP filter function (35)

The quality factor Q, frequency ω_0 and bandwidth BW are given by equations mention below:

$$Q = \sqrt{\frac{gm1}{gm2}\frac{C2}{C1}}$$ (36)

$$\omega 0 = \sqrt{\frac{gm1}{C1}\frac{gm2}{C2}}$$ (37)

$$BW = \frac{gm2}{C2}$$ (38)

The sensitivities wr.t frequency is expressed as

$$S_{gm1}^{w0} = S_{gm2}^{w0} = 0.5 , S_{C1}^{w0} = S_{C2}^{w0} = -0.5$$ (39)

4.2.1 *Non Ideal Analysis*

Parasitic effects

The filter implementation circuit based on FGMOS VDTA is shown in the figure 5 will be analyzed to check the effect of parasitic impedances. Ideally, capacitances appearing at respective terminals p, n,z and x are approximately zero in value and resistances appearing in parallel at respective terminals are very high valued. As shown the figure 5, a grounded capacitor C2 is connected to port Z to terminate it and after parasitic inclusion, it appears in parallel to parasitic R_z and C_z. ($R_z \parallel C_z$). The value of C_2 used in the design is quite higher than C_z and the value of R_z is much higher than external impedance at port z in the circuit. Hence, there is no unwanted pole contribution due to parasitic.

5. SIMULATION RESULTS AND COMPARISON

Floating gate MOSFET based realization of voltage differencing transconductance amplifier is proposed in this work using the model given by Adrel-Goldminz [23]. The design is simulated using SPICE in technology TSMC 0.18 µm. The aspect ratios of each transistor in the circuit are given in the table 2.

Table 2. Aspect ratio of FGMOS VDTA transistors

Transistors	W/L ratio
M1,M2,M5,M6	10
M3, M4, M7, M8	48

The VDTA circuit utilizes four FGMOSFETs with capacitors, C1=C2=200 fF and V_B= 0. 7V. The DC transfer characteristics curve of IX- and IX+ with respect to V_Z for the proposed VDTA is shown in the fig. 6. All bias currents are I_{B1}= I_{B2}= I_{B3}= I_{B4}=150 µA. It is clear from this figure that maximum input voltage range goes from -0.6 V to +0.6 V which provides wide input voltage range for operation at low supply voltage of ±0.7 V. The DC response of input stage of VDTA can be given by IX+ as shown in the fig. 7 Fig. 8 shows the transconductance gain of 74 dB at biasing currents of 150 µA. The bandwidth of proposed VDTA is 173 MHz as shown in the fig.9, so it can be utilized for applications requiring wide frequency range.

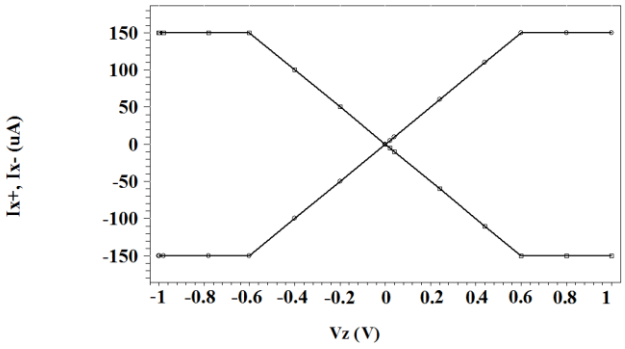

Figure 6: IX- and IX+ with respect to VZ

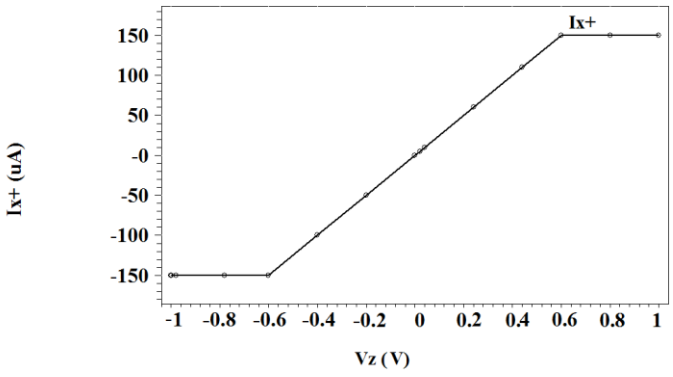

Figure 7 : IX+ with respect to VZ

Table 3 depicts the comparison between the CMOS VDTA in [15] and FGMOS VDTA proposed in this paper. The supply voltage is lower than circuit in [15] and power dissipation is low. The filter application also operates at same low supply voltage ±0.7 V and input voltage linear range is increased thus increasing the input voltage range.

Differential all pass filter is simulated with each capacitor value of 1pF. The transient response of the circuit for applied differential input of 150mV with frequency 1 MHz. Low THD with respect to differential input voltage at pole is achieved for all pass filter at pole frequency and is shown in the fig.11. The voltage mode filter with dual inputs and outputs is simulated using the proposed FGMOS based VDTA with C1 = 1 pF and total capacitance at Z terminal, CT = 1 pF to attain quality factor of 1 at supply voltage of ± 0.7 V. A Center frequency of approximately 100 MHz is achieved. conditions V2 = Vin and V1 = 0. Fig. 12 shows gain frequency responses of band pass, high pass and low pass filter functions with center frequency of around 100 MHz when V1 = Vin and V2 = 0 and high pass and bandpass filter functions for input conditions V2 = Vin and V1 = 0

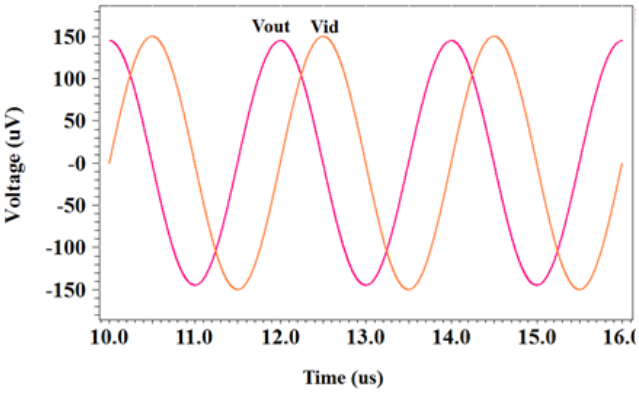

Figure 10. Transient response of differential all pass filter using FGMOS VDTA.

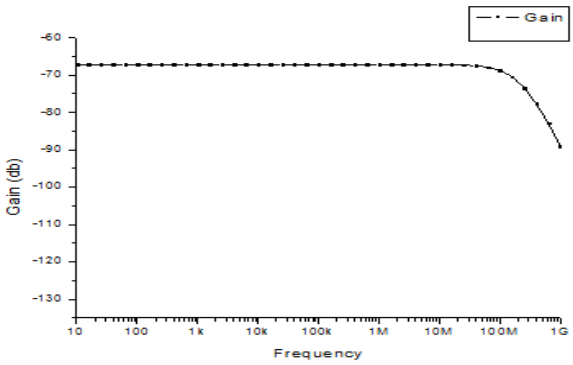

Figure 8: Transconductance gain (IZ/VP-VN) at biasing current of 150µA.

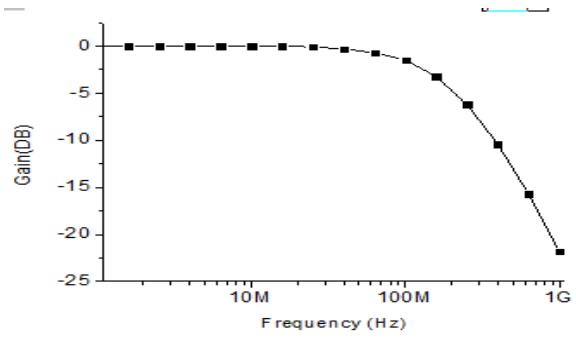

Figure 9: Bandwidth of proposed VDTA.

Table 3: Comparison of proposed work with [15]

Parameters	[15]	Proposed work
Technology	180nm	180nm
Supply Voltage	±0.9V	±0.7V
Input Range	±0.4V	-0.6V to +0.6V
Bandwidth at 150µA	Not reported	173Mhz
Power consumption	Not reported	90µW

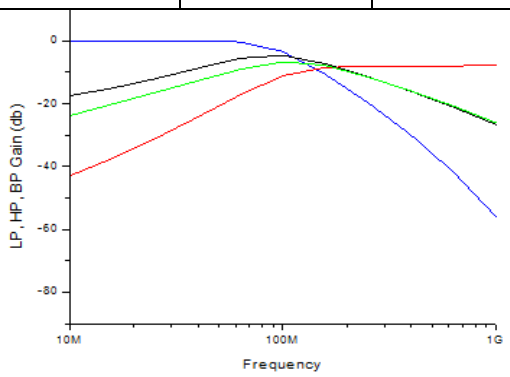

Figure 11: Gain frequency responses of LP, BP, HP filters using FGMOS VDTA

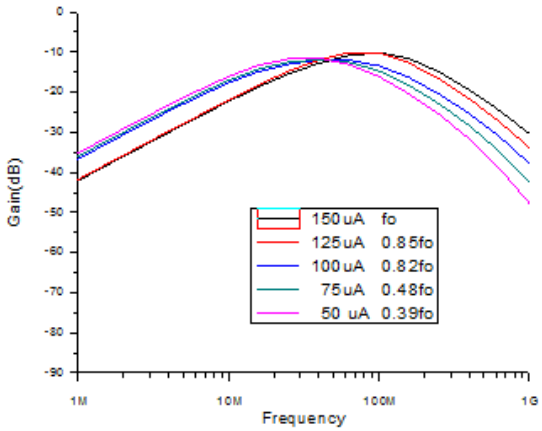

Figure 12: Tuning of frequency for band pass response

Figure 12 shows the tuning of frequency for band pass response. Biasing current is varied from 150 µA to 50 µA with constant quality factor. The pole is varying with variation in the biasing current. The frequency at biasing current 150 µA for band pass function is 98.47 MHz. It varies frequency, fo from 98.47 MHz to 39.37 MHz. By reducing biasing current to its half value, the frequency also reduces to half of fo.

6. CONCLUSIONS

This article presents FGMOS based voltage differencing transconductance to meet the demand of low power applications. The circuit is operating at lower supply voltage with lesser power dissipation. The block provides wide linear voltage range in addition to wider bandwidth. Two applications: first order differential all pass filter and voltage mode universal filter are realized using FGMOS VDTA. Both applications validate the effectiveness of the proposed circuit. FGMOS VDTA is useful for low voltage analog signal processing applications.

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