Multilevel Inverter Design Using Coupled Inductor with Improved Performance

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***Abstract*- This paper proposes a novel multilevel inverter design based on improvement of Total Harmonic Distortion and power efficiency corresponding to the reduction of diodes and capacitors from traditionally used topology as well as switching loss of the system. The proposed topology uses split coil coupled inductor and its mutual inductance property in order to produce 6-switch 7-level voltage output. IGBT switching is implemented in the inverter to produce a fundamental 50Hz output signal with reduced THD and power efficiency. Simulations are done using MATLAB-SIMULINK to validate the design and the expected outcomes. This proposed inverter is expected to be highly efficient if implemented for micro-inverter applications due to its compactness and loss reduction.**

Keywords— Multilevel Inverter, Coupled Inductor, Total Harmonic Distortion, Switching Loss, SIMULINK.

I. INTRODUCTION

Multilevel Inverter has become popular and widespread because of having multiple advantages over conventional inverters including better waveform quality and as an alternative in high voltage requirement situations. These has resulted into many fold researches which derived multiple well-established topologies with both advantages and drawbacks [1]-[2]. In each topology there are some trade-offs between cost, weight, efficiency and waveform. In cascaded H-Bridge topology while the weight and cost is reduced it results in increased power loss whereas the flying capacitor topology has reduced power loss in exchanged of being heavier in nature with increased cost [3].

Different modifications of the above mentioned topologies has been done in order to improve the drawbacks. One of this has been use of coupled inductors which while producing multilevel output also provides alternative paths for outputs. As a result the switching devices operates in lower current environment than the output current [4]-[6]. Also reduced number of switches is essential to improve harmonic distortion and power loss which resulted into several modifications of original topologies [7]-[8].

This paper introduces a novel design of a multilevel inductor working on the principle of coupled inductor thus enabling the power IGBT switches to operate in low current and low frequency condition resulting in lower switching loss. This design also uses 6 switches for desired 7 level input which also ensures low power consumption and better waveform in output. Analog Butterworth filter is used to estimate pure sine-wave with 50Hz fundamental frequency. This has been achieved with a relatively low switching frequency reducing the overall switching loss contributing to the overall reduction.

One of the main characteristics of this design is being capacitor-less which decreases the weight of the system making it more compact and improves output waveform [3]. For this reason electrolytic capacitors are being replaced in micro-inverter topologies as well [9]. This proposed design eliminates the need of capacitors which are integral part of conventional topologies.

Another aim of the design is to reduce total harmonic distortion. THD improvement is essential for multilevel inverter as being one of the significant factor of it [10]. The THD factor in this paper has been significantly improved using Modified PWM techniques which allows the use of the design without any complex filter to be used.

II. PROPOSED TOPOLOGY

Fig 1 shows the proposed topology for multilevel inductor.

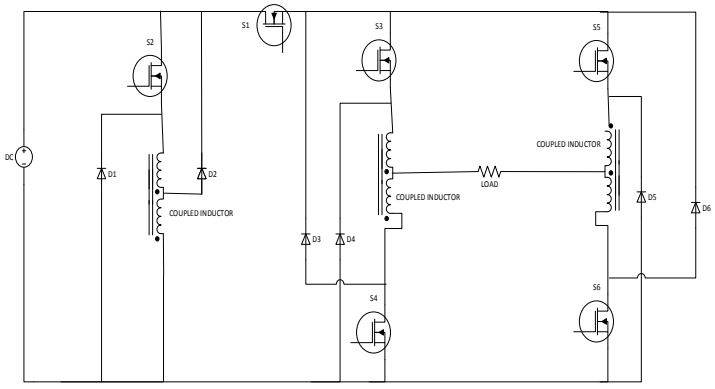

Fig. 1: Circuit Setup for Proposed Multilevel Inverter

There are three coupled inductors used to get seven levels of output voltage. For this circuit construction minimum number of switches are six. The mutual inductance of the coupled inductors contributed to the multilevel output voltage. The switching pattern used for the system led the system to operate in six mode of operation. Each operating modes are mentioned in the switching sequence table

Table 1: Switching sequence for modes of operation

Modes	S1	S2	S3	S4	S5	S6	Level
	0	0	0	0	0	0	0
Mode1	0	1	0	1	1	1	Vdc/4
Mode2	1	0	0	1	1	1	Vdc/2
Mode3	1	0	0	1	1	0	Vdc
	0	0	0	0	0	0	0
Mode4	0	1	1	1	0	1	-Vdc/4
Mode5	1	0	1	1	0	1	-Vdc/2
Mode6	1	0	1	0	0	1	-Vdc

IGBT was used as our primary switching device. It allows to work in improved switching speed and dynamic performance. Also because of lower gate voltage requirement it can bet tuned for lower switching loss.

6 modes of operation have been used for voltage level operation from 0 volt level. For this some distinct switching sequence have been used which is mentioned in Table 1. Figure 7 shows the different switching functionalities for corresponding voltage output in order to achieve the desired 7 level voltage output.

Low frequency PWM signal was used to produce multilevel output. Complex SPWM signal input was avoided commonly used in conventional topologies which requires complex logical circuit implementation [11]

This topology uses a low frequency PWM signal to implement the desired multilevel output. Thus by decreasing the switching frequency along with the number of switches being used it was possible to decrease the switching loss to a major extent.

III. SIMULATION MODEL

Fig. 2 shows the simulation model that has been designed in order to simulate and analyse different circuit outputs and parameters.

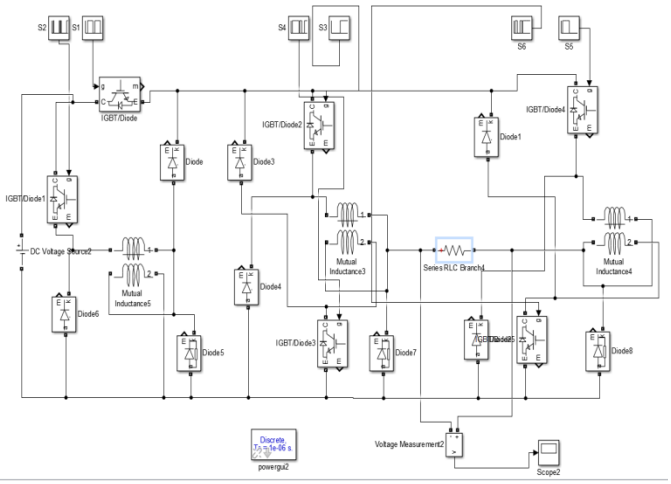

Fig. 2: Simulation Model in MATLAB-SIMULINK Environment

For designing the model MATLAB-SIMULINK environment is used. IGBTs are modelled according to the specified model used. Mutual inductance block is used to design the coupled inductors.

IV. SIMULATION ANALYSIS

A. Output Analysis: Fig. 3 shows the 7 level Inverter output voltage before filter. For implementing 220V RMS output with 50 HZ fundamental frequency output was measured AC peak voltage as 311V for 220V RMS AC Voltage.

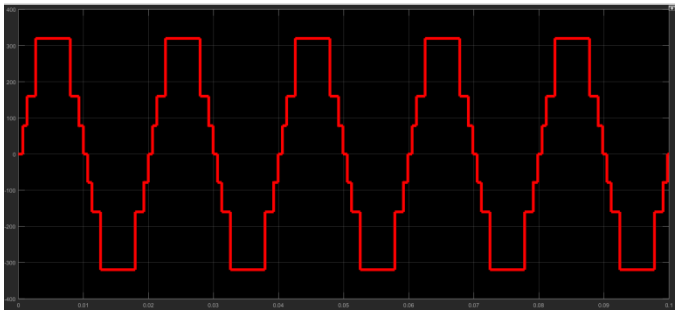

Fig 3: 7 level Output Waveform

B. Total Harmonic Distortions (THD) Analysis: Reduction of Total Harmonic Distortion is one of the major aim of this design. For this simulation model FFT Analysis Tool from powergui has been used. Fig. 4 shows the FFT analysis of the 7 level output waveform which gives a THD of 13.99% under the condition of 50Hz fundamental frequency and 1000 Hz maximum frequency. This are the results obtained before the use of the filter. This is well acceptable for all kinds of industrial uses especially in renewable energy application like photovoltaic cell.

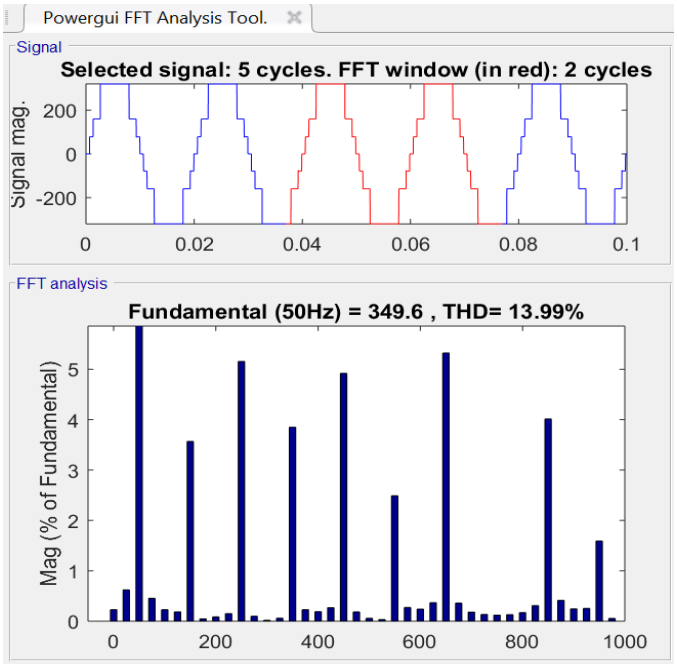

Fig. 4: FFT Analysis of Output Waveform

THD analysis of the simulation proves that a significant improvement is made without the use of any complex filter thus reducing the weight and cost of the inverter.

C. Switching Loss Analysis: As number of switches has been reduced along with switching loss per power IGBT, an improved loss condition can be shown

Switching Power Loss formulae is given as follows,

$P=\frac{1}{2} I_d . V_{b.}(t_{off}+t_{on}).f+1/2\ C_{oss}.V_d^{2.}f$

i.e. $P=(Eon+Eoff)*f$

For calculating for the given condition taking TK18A30D Power IGBT as our primary switching device and using its condition for Eon=333μJ, Eoff=537μJ for ideal conditions [12] and for our maximum switching frequency which is f=300Hz , switching loss can be calculated as .21 Watt per switch at a maximum value.

D .Output Current Analysis: One of the advantages of using coupled inductor in designing inverter is having high output current while keeping the switches working in reduced current environment. Here distinction between amplitude level of Output Current and IGBT Current operating level is shown in Fig. 5 and Fig. 6

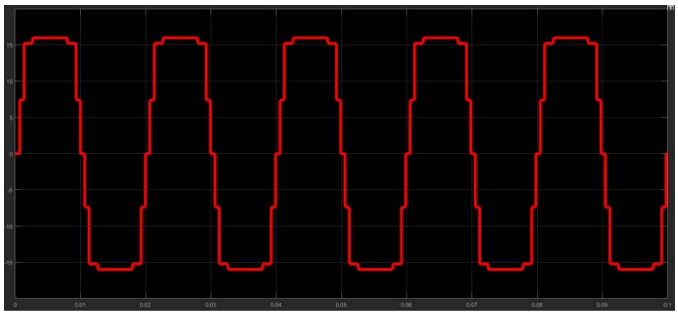

Fig 5: Output Multilevel Current Level

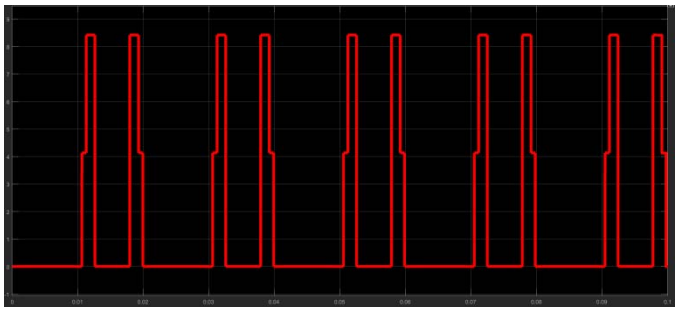

Fig. 6: IGBT3 Operating Current

Here, the IGBT switches in H-Bridge portion operates at around 50% of the rated output current which produces a significant decrease in current rating of switches. Such arrangements are suitable for high current applications [5][14].

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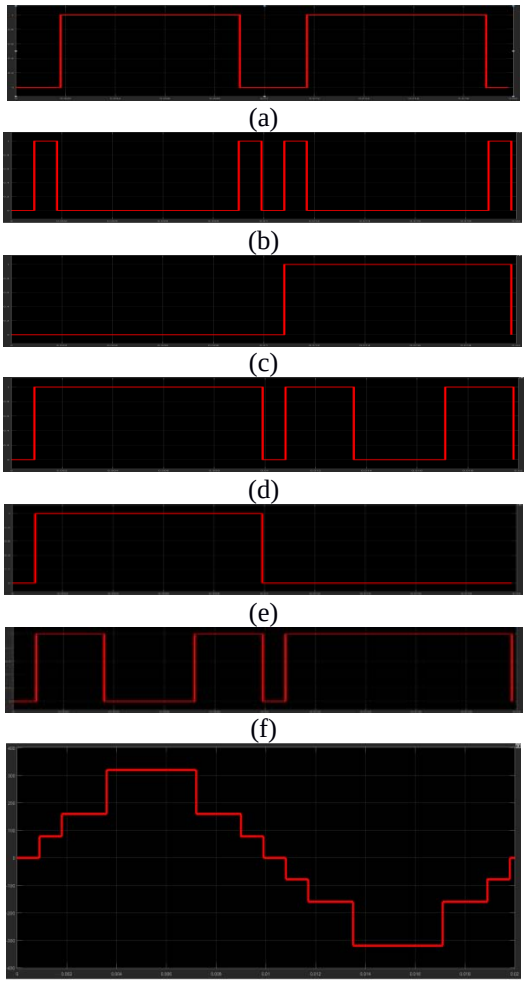
V. Control Strategy

In this proposed inverter topology a modified PWM technique is used to obtain lower THD multilevel output. It reduces the THD as much as that of SPWM technique. Referenced design [13] has implemented hybrid SPWM technique where the THD is reduced to 17.79%. Moreover, some other techniques of SPWM such as, Phase Shifted, In Phase Disposition, phase opposition disposition, alternate phase opposition disposition and their corresponding THD improvement data are given by 18.25%, 18.06%, 17.56%, 18.16%. Implementing SPWM technique through hardware is rather complex then providing PWM signals to the gate of the switches. The proposed modified PWM technique is implementable by using any programmable microcontroller through hardware programming. Figure shows the input gate pulses produced to obtain the lower THD multilevel output.



(a) (b) (c) (d) (e) (f) (g)

Fig. 7: Chronological Switching Patterns of 6 Switching Devices and Output Waveform of 1 full cycle.

The multilevel output has THD of 13.99% which is less than that of the SPWM techniques used (figure-7). Without the modified PWM THD of the output for the design in consideration was was 28.78%.

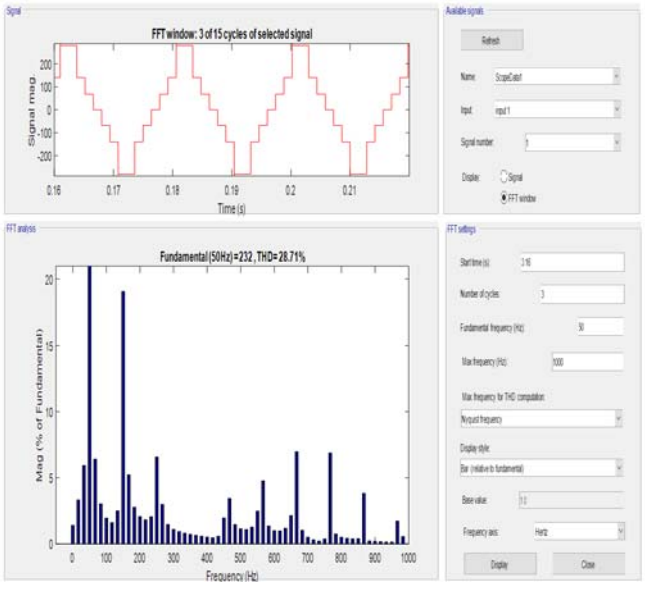


Fig 8: FFT Analysis of output waveform (before Modified PWM technique

VI. RESULTS AND DISCUSSION

The paper successfully implemented its desired output by decreasing the number of switches being used for similar coupled inductor Topology [14]. These combined with lower switching frequency gives us reduced switching power. Another aspect of the analysis was to reduce Total Harmonic Distortions. An impressive THD of 13.99% was achieved in such compactness without any addition of filter. These factors enables the design to be further analysed in renewable energy applications due to its reduced weight nature.

VII. CONCLUSION

In this paper an improved topology for micro-inverter was simulated and its characteristics were compared with conventional multilevel inverters. This model achieved a very low THD factor with low switching frequency. Also as no capacitor was used, making the circuit very compact. Besides being designed with coupled inductor topology it achieved high output current in comparison with other conventional topologies enabling it to be used for motor drives and generators. The topology was also developed keeping further use in solar panel in mind. Since cost of the circuit is also low, this model is feasible for Solar Panels.

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