Solving circuits by multiple transformation graphs

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***Abstract*—**This paper deals with solving electronics circuits by method of the transformation graphs only. As described, the Mason´s formula for calculation of the result can be left out in selected cases, and the theory of the transformation graphs is quite sufficient for the whole full graph solving selected simply circuits with the switched capacitors, too.

***Keywords*—** Transformation graph, Mason´s formula, MC-graph, resulting graph, algebraic minors.

I. Introduction

THE transformation graphs are used for construction final graph to solving electronics circuits and final graph is calculated by Mason´s formula. It means this method is combination graph and numerical methods, booth. But solving is possible by graphs only in selected circuits, as is described follows.

II. Princip of the Method

One of the method possibilities how to calculate a matrix determinant is repeated application of (1)

$$y_{ij} = \tilde{y}_{ij} - \tilde{y}_{in} . \frac{\tilde{y}_{nj}}{\tilde{y}_{nn}} \qquad (1)$$

until the order of the matrix decreases generally from the n-th order to the second order, i.e. to the form (2)

$$\begin{array}{|c|c|} \hline y_{11} & y_{12} \\ \hline y_{21} & y_{22} \\ \hline \end{array} \qquad (2)$$

as is shown in [5]. From this matrix, the voltage transfer is then calculated by the algebraic complements method as a ratio (3)

$$\frac{V_2}{V_1} = \frac{\Delta_{1:2}}{\Delta_{1:1}} \qquad (3)$$

where $\Delta_{1:2} = -y_{21}$ and $\Delta_{1:1} = y_{22}$. The matrix is thus reduced up to a dot matrix with a single component. This reduction can be described by means of incidence matrices, for the component $\Delta_{1:2} = -y_{21}$ in the following way, as is shown in Fig1.

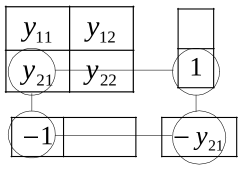

Fig.1 reduction for the component $\Delta_{1:2} = -y_{21}$

Reduction for the component $\Delta_{1:1} = y_{22}$ is shown in Fig.2.

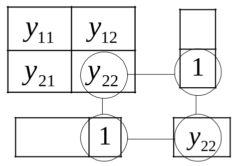

Fig.2 reduction for the component $\Delta_{1:1} = y_{22}$

The reduction of the matrix can be represented by the transformation graph [2].

The above described reduction to a dot matrix can also be carried out by a transformation graph, when a complete MC-graph [4] showing a second-order matrix is reduced to its own loop corresponding with a dot matrix. The transfer of the branches of the transformation graph is then given by the components of the incidence matrices for the component $\Delta_{1:2} = -y_{21}$ like this, as is shown in Fig.3, where ▷ is transfer of the current and → transfer of the voltage.

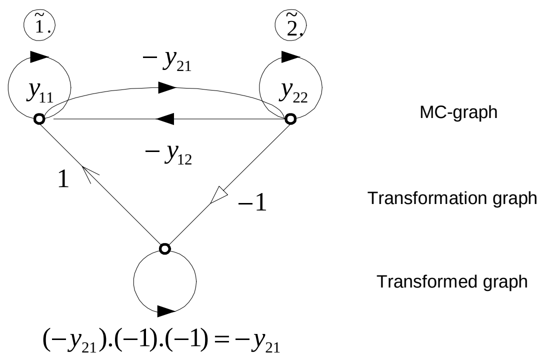

Fig.3 graph of the reduction $\Delta_{1:2} = -y_{21}$

Another possibility how to plot this transformation graph is directly breaking down the relation for an algebraic comment.

For example for the complement $\Delta_{1:2}$ it holds that (4)

$$\Delta_{1:2} = \Delta_{1>0:2>0} \tag{4}$$

which is interpreted as row one is going to zero and column two too, which can be interpreted for the matrix transcription of complements as leaving out the first row and the second column. However, since in an admittance (5) matrix rows correspond to currents I and columns to voltages V,

$$\begin{array}{c|c|c|} & V_1: & V_2: \\ \hline I_1: & y_{11} & y_{12} \\ \hline I_2: & y_{21} & y_{22} \\ \hline \end{array} \tag{5}$$

according to the relation $\Delta_{1:2} = \Delta_{1>0:2>0}$ thus leaving out the first row in the matrix is represented by leaving out the branch with the current transfer to the first node in the transformation graph and leaving out the second column in the matrix is equivalent to leaving out the branch with the voltage transfer from the second node in the transformation graph.

Then for the complement $\Delta_{1:1}$ it holds (6)

$$\Delta_{1:1} = \Delta_{1>0:1>0} \tag{6}$$

which in matrix transcription means leaving out the first row and the first column in the matrix, and this can be interpreted as leaving out the branch with both the current and voltage transfer to the first node in the transformation graph, so there is only the branch to the second node left. Thus the transformation graph representing the relation $\Delta_{1:1} = \Delta_{1>0:1>0}$ is shown in following Fig.4.

In such cases, this construction can spare us from the necessity to use the Mason's rule for evaluating the resulting graph; the graph construction is actually a graphic representation of multiple algebraic components.

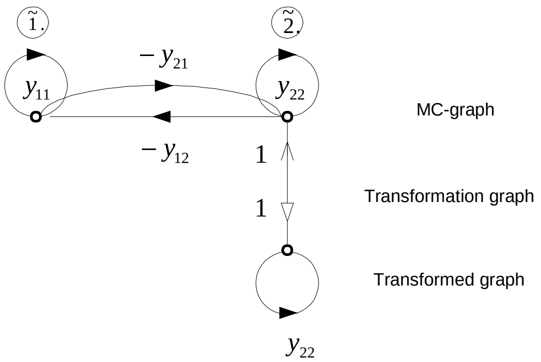

Fig.4 graph of the reduction $\Delta_{1:1} = y_{22}$

In such cases, this construction can spare us from the necessity to use the Mason's rule for evaluating the resulting graph; the graph construction is actually a graphic representation of multiple algebraic components.

III. Evaluation of the Transformation Graph

Rules for evaluation of the transformation graph described in [1], [6], [8] is very simply:

The admittance after transformation is given by the relation

$$Y = a^V.\tilde{Y}.a^I \tag{7}$$

where a^V is transfer of the voltage branch, a^I is transfer of the current branch and α can be ± 1. If the branch is transformed to the branch or the loop to the loop, then $\alpha = +1$, if the loop is transformed to the branch or the branch is transformed to the loop, then $\alpha = -1$.

Described evaluation is shown in Fig.5, for $\alpha = -1$ on the top and for $\alpha = +1$ at the bottom.

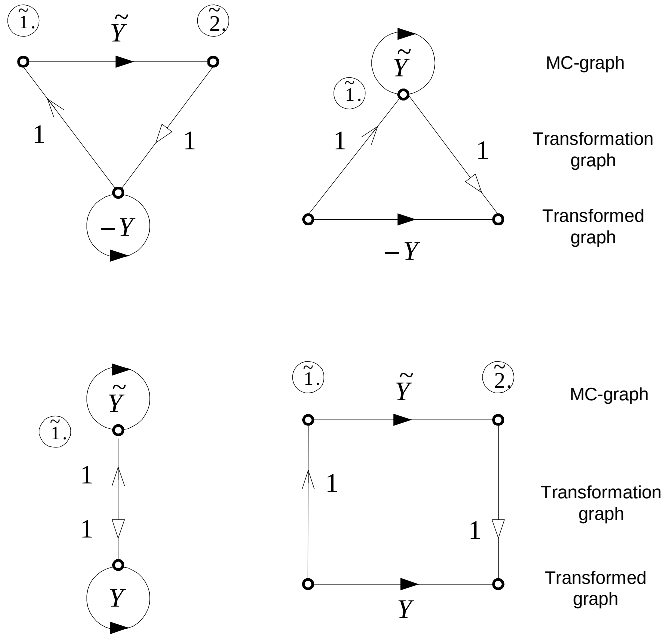

Fig.5 rules for evaluation of the transformation graphs

IV. Example

In the course of the very circuit solution, e.g. for a circuit of an inverting summator with a schematic diagram in Fig.6 an MC-graph is drawn in Fig.7 on the top.

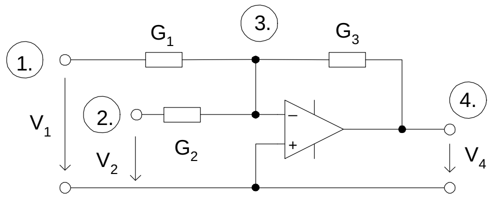

Fig.6 circuit diagram to the example

We are considering the change of amplification of the operational amplifier, the transformation graph of the operation amplifier with the break-point frequencies ω_T, ω_2 [1], [6] is shown in Fig.8.

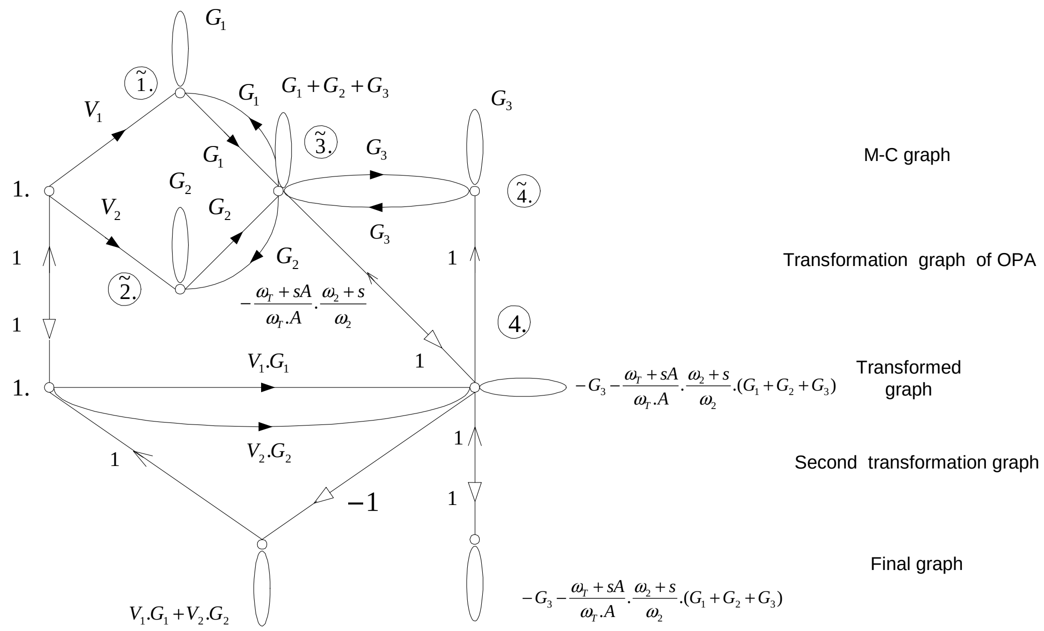

Fig.7 graph solving circuit from Fig.6

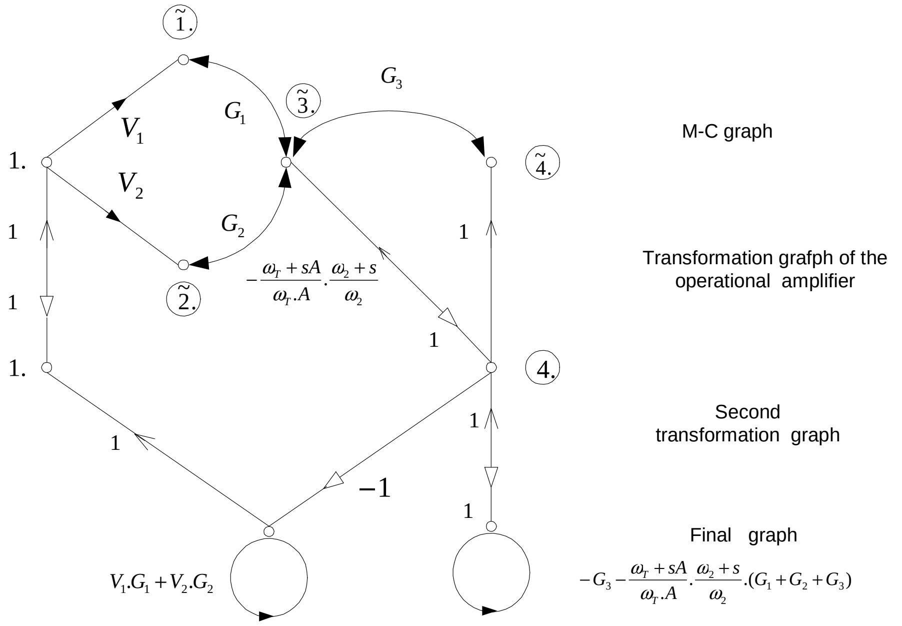

Fig.9 graphical solution of the circuit from Fig.6 by a simplified MC-graph, transformed graph is left

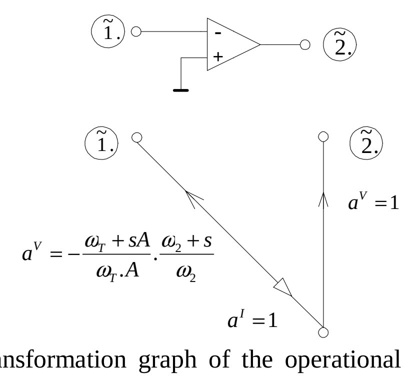

Fig.8 transformation graph of the operational amplifier with break point frequencies

Into this graph, we draw a transformation graph of the operational amplifier including the change of its amplification in an open loop. As a result, we get the transformed graph in the middle. From this transformed graph, the resulting graph drawn at the bottom is plotted by means of another transformation graph.

This graph construction is actually a graphic representation of the algebraic components [3], in this case double ones. The output voltage is then directly given by the relation (8), where $s = j\omega$ and ω is frequency where is transfer calculated.

$$V_4 = -\frac{V_1.G_1 + V_2 G_2}{G_3 + \frac{\omega_T + sA}{A.\omega_T}.\frac{\omega_2 + s}{\omega_2}.(G_1 + G_2 + G_3)} \qquad (8)$$

For the solution itself it is not necessary to plot the original MC graph in detail. Its construction can be just implied in a simplified way [6] as shown in Fig.9, where is left transformed graph, too.

V. Verification

To compare, we will bring forward a solution of the same inverting summator by a commonly used modified nodal method [9]: as the circuit contains four nodes and one operational amplifier, the hybrid matrix describing the circuit will have four rows and columns plus one added row and column of the operational amplifier stamp, so it will look this way:

For the calculation, the method of linear superposition will be used, when the voltage V_4 is given by the contribution by the voltage V_1 with a zero voltage V_2 (i.e. with a grounded node 2) with the value of $V_4^{(1)}$, for which with the use of the multiple signed minors method, for example in [1], [5], [6] it holds that (9)

$$V_4^{(1)} = V_1.\frac{\Delta_{1,2:4,2}}{\Delta_{1,2:1,2}} \qquad (9)$$

when the grounded node 2 corresponds to omitting the 2nd row and the 2nd column in the hybrid matrix, and by the contribution by the voltage V_2 with a zero voltage V_1 (i.e. with a grounded node 1) with the value of $V_4^{(2)}$, for which with the use of the multiple signed minors method it holds that (10)

$$V_4^{(2)} = V_2.\frac{\Delta_{2,1:4,1}}{\Delta_{2,1:2,1}} \qquad (10)$$

when the grounded node 1 corresponds to omitting the 1st row and the 1st column in the hybrid matrix, so the resulting voltage V_4 is given as (11) after numeration by an expansion along the item of the last column i.e. identical with the result obtained by the transformation graph method.

$$V_4 = V_1.\frac{\Delta_{1,2:4,2}}{\Delta_{1,2:1,2}} + V_2.\frac{\Delta_{2,1:4,1}}{\Delta_{2,1:2,1}} =$$

$$= \frac{V_1.\Delta_{1,2:4,2}.(-1)^1 + V_2.\Delta_{2,1:4,1}.(-1)^2}{\Delta_{1,2:1,2}} =$$

$$= \frac{-V_1.\begin{vmatrix} -G_1 & G_1+G_2+G_3 & 0 \\ 0 & -G_3 & 1 \\ 0 & -\frac{A.\omega_T}{\omega_T+sA}.\frac{\omega_2}{\omega_2+s} & 0 \end{vmatrix}.(-1)^1 + V_2.\begin{vmatrix} -G_1 & G_1+G_2+G_3 & 0 \\ 0 & -G_3 & 1 \\ 0 & -\frac{A.\omega_T}{\omega_T+sA}.\frac{\omega_2}{\omega_2+s} & 0 \end{vmatrix}.(-1)^2}{\begin{vmatrix} G_1+G_2+G_3 & -G_3 & 0 \\ -G_3 & G_3 & 1 \\ -\frac{A.\omega_T}{\omega_T+sA}.\frac{\omega_2}{\omega_2+s} & -1 & 0 \end{vmatrix}.(-1)^0} =$$

$$= -\frac{V_1.G_1 + V_2 G_2}{G_3 + \frac{\omega_2 + s}{\omega_2}.\frac{\omega_T + sA}{A.\omega_T}.(G_1 + G_2 + G_3)} \qquad (11)$$

The member $\frac{\omega_2 + s}{\omega_2}.\frac{\omega_T + sA}{A.\omega_T}$ in (7) and (11) concerning break point frequencies on the amplification characteristics.

VI. The Use For Solving Simple Switched Capacitor Circuits

A. Solving by the Method of Equivalent Resistors

The method of equivalent resistors described for instance in [9] is the simplest method of solving SC circuits and it consists in replacing a switched capacitor by an equivalent resistor, whose resistance value issues from the relations between the charge and the voltage $Q = C.U$ and from the definition relation for the current $I = \frac{Q}{T}$. After substituting the first relation into the second one, we get an equation $I.T = C.U$ from which the ratio between voltage and current can be expressed by (12)

$$R = \frac{U}{I} = \frac{T}{C} \qquad (12)$$

which is just the value of the resistance R, which is equivalent to the capacitor C switched with the period T. The disadvantage of this method is that it does not concern the so called periodicity of discrete circuits' characteristics.

The use of the above described method of evaluating a graph with two nodes when solving SC circuits by the method of equivalent resistances will be illustrated in the following example of the simply CMOS switched integrator [7].

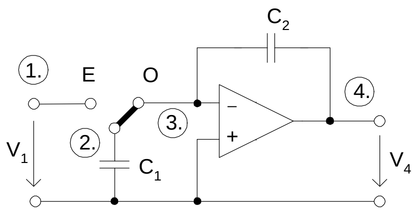

Fig.10 circuit diagram to the example

When solving the circuit whose diagram is shown by Fig.10 by the method of equivalent resistances, the switched capacitor is first replaced by an equivalent resistor with the conductance $f_S.C_1$, by which we get the diagram in Fig.11.

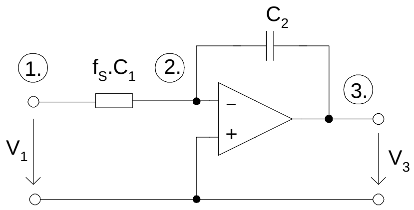

Fig.11 circuit diagram from Fig.10 after replacing the switched capacitor with a equivalent resistor

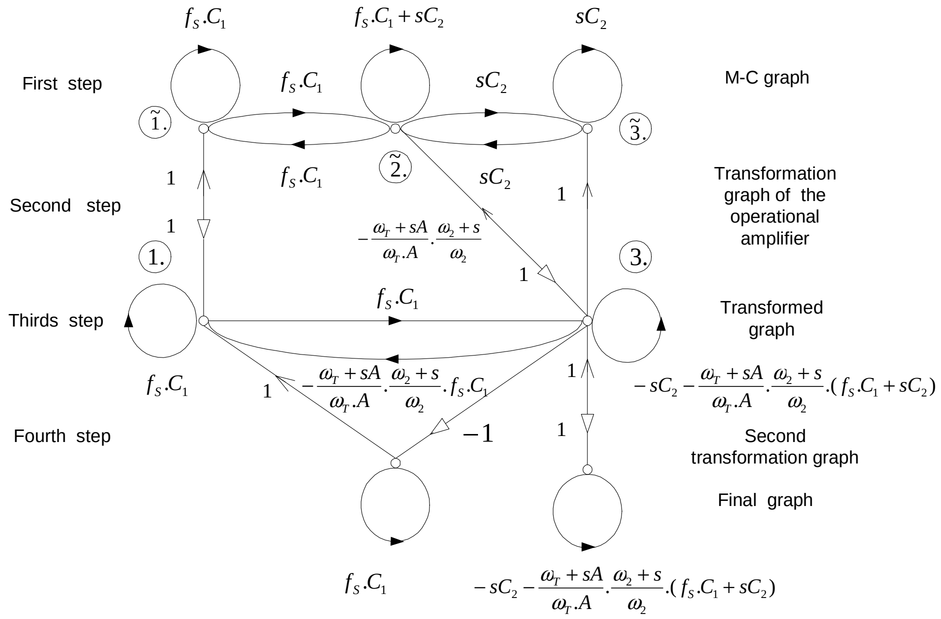

Fig.12 Graphical solution of the circuit from Fig.10

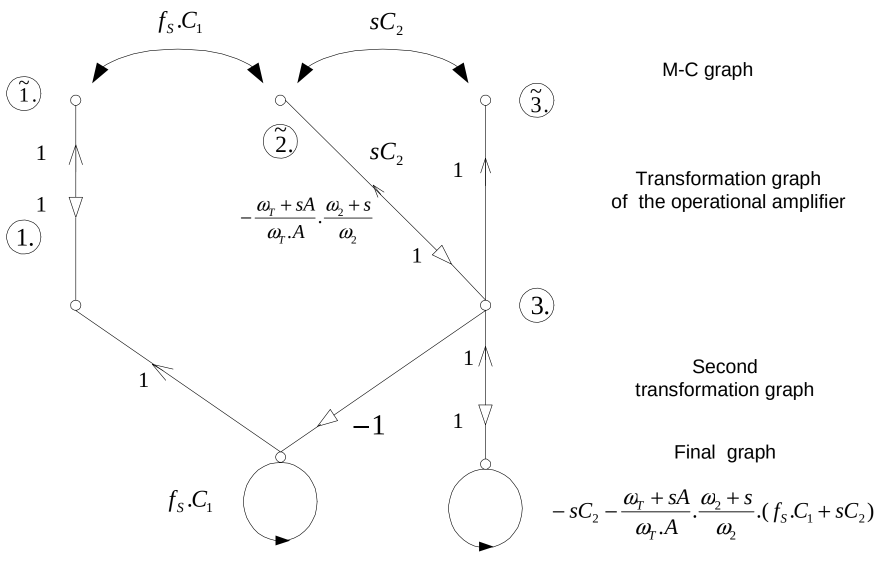

Fig.13 graphical solution of the circuit from Fig.9 by a simplified MC-graph

For this diagram, we draw the MC-graph which is in Fig.12 at the top.

In the next step, a transformation graph of an operational amplifier is drawn into this graph. The transformation graph can also include the influence of its varying amplification and frequency.

The result is the transformation graph in Fig.12 in the middle. Finally, by drawing in the second transformation graph described in paragraph 1 we get the resulting graph with two terms, the first of which indicates the numerator and the other the denominator of voltage transfer.

Then the voltage transfer of the solved circuit is given by the formula (13)

$$\frac{V_3}{V_1} = \frac{f_S.C_1}{sC_2 + \dfrac{\omega_T + sA}{A.\omega_T}.\dfrac{\omega_2 + s}{\omega_2}.(f_S.C_1 + sC_2)} \qquad (13)$$

where in the numerator there is the first resulting graph and in the denominator the other one.

For the solution itself it is not necessary to plot the original MC graph in detail. Its construction can be just implied in a simplified way [6] as shown in Fig.13, where is left transformed graph, too.

B. Verification

We will bring forward a solution of the same circuit from Fig.10 by used modified nodal method:

$$\frac{V_3}{V_4} = \frac{\Delta_{1:3}}{\Delta_{1:1}} = \frac{\begin{vmatrix} -f_S.C_1 & f_S.C_1 + sC_2 & 0 \\ 0 & -sC_2 & 1 \\ 0 & -\dfrac{A.\omega_T}{\omega_T + sA}.\dfrac{\omega_2}{\omega_2 + s} & 0 \end{vmatrix}}{\begin{vmatrix} f_S.C_1 + sC_2 & -sC_2 & 0 \\ -sC_2 & sC_2 & 1 \\ -\dfrac{A.\omega_T}{\omega_T + sA}.\dfrac{\omega_2}{\omega_2 + s} & 1 & 0 \end{vmatrix}} =$$

$$= \frac{-(-\dfrac{A.\omega_T}{\omega_T + sA}.\dfrac{\omega_2}{\omega_2 + s}).(-f_S.C_1)}{-sC_2.(-\dfrac{A.\omega_T}{\omega_T + sA}.\dfrac{\omega_2}{\omega_2 + s}) - f_S.C_1 + sC_2} =$$

$$= \frac{f_S.C_1}{sC_2 + \dfrac{\omega_2 + s}{\omega_2}.\dfrac{\omega_T + sA}{A.\omega_T}.(f_S.C_1 + sC_2)} \qquad (14)$$

C. Solving by a Method of Z-Transformations

In [8] the construction of a transformation graph switched by capacity (i.e. by capacity including the switch) is described. This graph is shown in Fig.13.

This graph makes it possible to solve the circuit from Fig.10 by means of *z*-transformation, but without distinguishing the phases of switching. By adding another transformation graph described in chapter II. into the transformation graph of the switch and operational amplifier, we can consequently obtain the resulting relation, as shown in Fig.14.

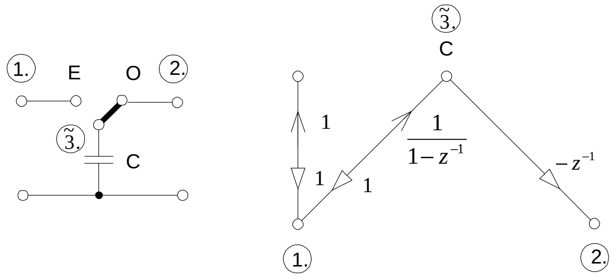

Fig.13 transformation graph switched by capacity

Thus the resulting transfer will be (15)..

$$\frac{V_3}{V_1} = \frac{z^{-1}\dfrac{1}{1-z^{-1}}C_1}{-C_2} = -\frac{z^{-1}}{1-z^{-1}}.\frac{C_1}{C_2} \qquad (15)$$

where $z = \exp(j\omega.f_S^{-1})$ and f_S is sampling rate.

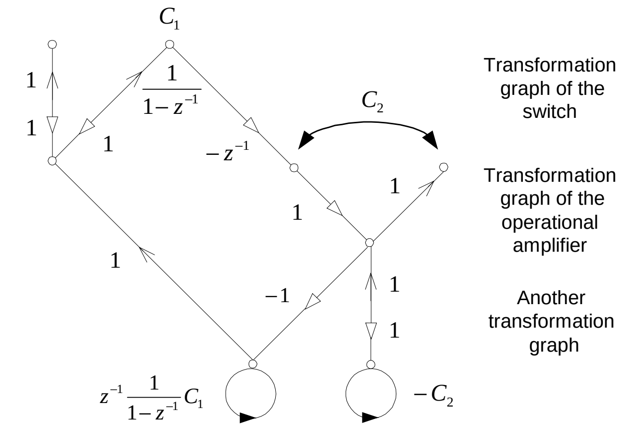

Fig.14 graphical solution of the circuit from Fig.10

If the break point frequencies are considering, then graph is shown in Fig.15, resulting transfer in this case will be (16).

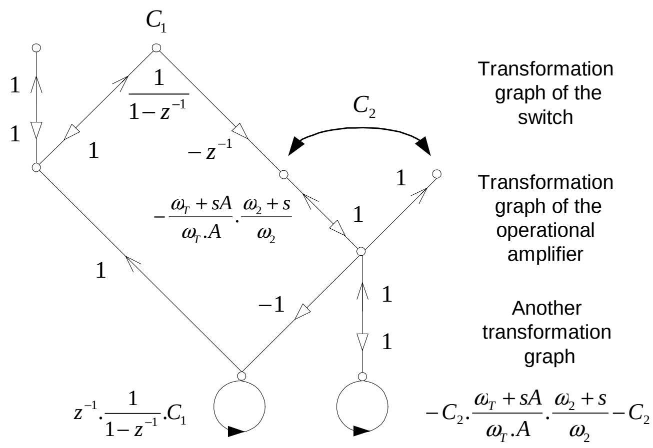

Fig.15 solution of the circuit with break point frequencies

$$\frac{V_3}{V_1} = \frac{z^{-1}\,\frac{1}{1-z^{-1}}\,C_1}{-C_2.\frac{\omega_T + sA}{A.\omega_T}.\frac{\omega_2 + s}{\omega_2} - C_2} \qquad (16)$$

The described method seems to be suitable for graph solution of simple circuits with the switched capacitors described by the z-transformation, too.

Solution by described methods another (but rather difficult) circuits will be forward. Analyzed circuit diagram, contained two capacitors C_2, C_4, two switched capacitors C_1, C_3 and operation amplifier is shown in Fig.16.

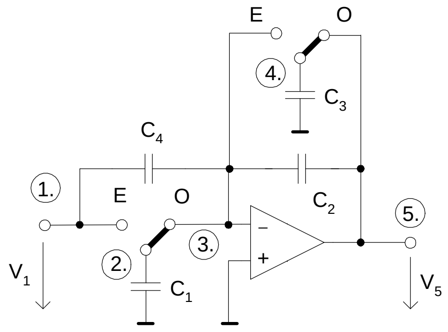

Fig.16 circuit diagram to the example another circuits

We draw the MC-graph which is in Fig.17 at the top, where

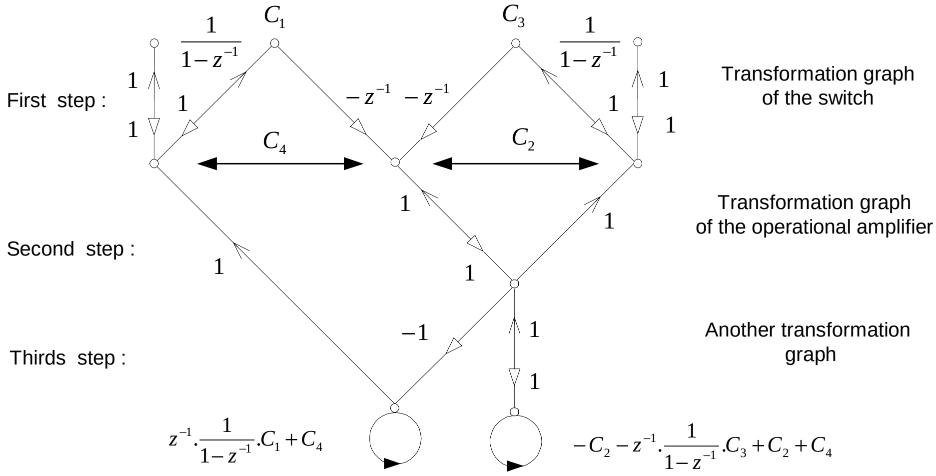

Fig.17 graphical solution of the circuit from Fig.

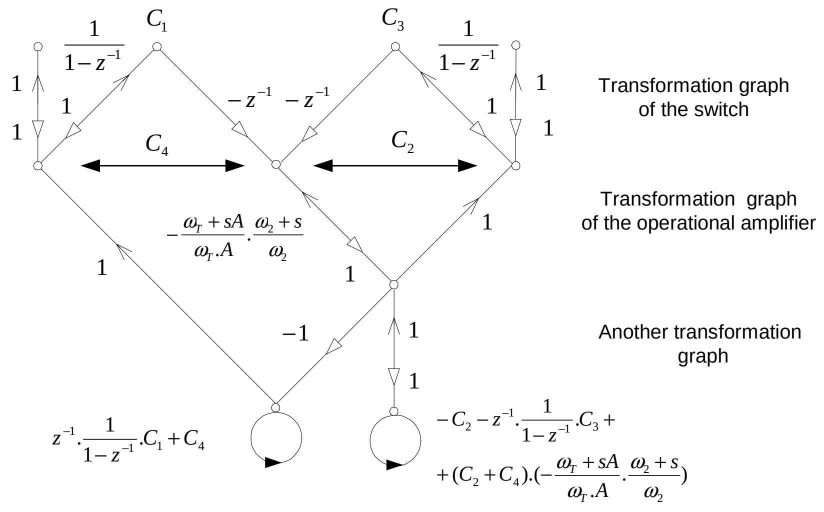

Fig.18 graphical solution of the circuit from Fig.16

the branch of the capacitor C_3 go back, because transfer of the signal by the capacitor C_3 is from node 5 (where is output of the operational amplifier) to node 3 (where is input of this amplifier).

Then the voltage transfer from Fig.17 of the solved circuit is given by the following formula (17).

$$\frac{V_5}{V_1}=\frac{z^{-1}.\frac{1}{1-z^{-1}}.C_1+C_2}{-C_2-z^{-1}.\frac{1}{1-z^{-1}}.C_3+C_2+C_4}=$$

$$=-\frac{z^{-1}.\frac{1}{1-z^{-1}}.C_1+C_2}{z^{-1}.\frac{1}{1-z^{-1}}.C_3-C_4} \qquad (17)$$

If the break point frequencies are considering, then correspondent graph is shown in Fig.18, resulting transfer in this case will be (18).

$$\frac{V_5}{V_1}=\frac{z^{-1}.\frac{1}{1-z^{-1}}.C_1+C_2}{-(C_2+C_4).\frac{\omega_T+sA}{A.\omega_T}.\frac{\omega_2+s}{\omega_2}-z^{-1}.\frac{1}{1-z^{-1}}.C_3-C_2}$$

$$=-\frac{z^{-1}.\frac{1}{1-z^{-1}}.C_1+C_2}{(C_2+C_4).\frac{\omega_T+sA}{A.\omega_T}.\frac{\omega_2+s}{\omega_2}+z^{-1}.\frac{1}{1-z^{-1}}.C_3+C_2} \qquad (18)$$

As we can see, some circuits contained switched capacitors without distinguishing the phases of switching, operational amplifier with break point frequency can be solved by described full graph method, too. Construction of this graph is very simply.

VII. CONCLUSION

The Mason´s formula for calculation of the result can be left out in selected cases, and the theory of the transformation graphs is quite sufficient for the whole solving. If the Mason´s formula is used for evaluation of the final graph, then transformed graph is necessary. In described method, Mason´s formula is replaced by another transformation graph from chapter II. therefore transformed graph can be left. As is shown, the solving by described method is in one step reduced this way.

Thanks to its clarity, the graphic method gives well arranged look to analyzed circuit with switched capacitors and operational amplifier, too.

The described method seems to be suitable for graph solution of simple circuits when the application of Mason´s rule is not required.

REFERENCES

[1] Biolek, D., *Solving Electronic Circuits*. BEN Publisher Prague, 2004.

[2] Biolek,D., Biolkova,V. „Analysis of Circuits Containing Active Elements by using Modified T-graphs.“ Contribution to the book *"Advances in Systems Science: Measurement, Circuits and Control"*, WSES Press, Electrical and Computer Engineering Series, 2001. Editors N. E. Mastorakis and L.A. Pecorelli-Peres, pp. 279-283. ISBN 960-8052-39-4

[3] Biolek,D., Biolkova,V., "Flow Graphs Suitable for Teaching Circuit Analysis.“ in *Proceedings of the 4th WSEAS International Konference on Applications of Electrical Engineering – AAE´05*, Praque, Czech Republic, March 13-15, 2005.

[4] Biolek,D., Biolkova,V., „Flow Graphs for Analysis (not only) Current-Mode Analogue Blocks.“ Contribution to the book *"Recent Advances in Circuits, Systems and Signal Processing"*, WSEAS Press, Electrical and Computer Engineering Series, 2002. Editors N. E. Mastorakis and G. Antoniou, pp. 151-156. ISBN 960-8052-64-5.

[5] Čajka,J., *Theory of the Linear Circuits*, SNTL/ALFA Prague/Bratislava, 1979.

[6] Dostál, T., „The analysis of the switched circuits with the active components". *Electronic horizont*, 45(1), 1984, pp. 21-26

[7] Kliros,G.S.,Andreatos,A.S. "Using Transistor Roles in Teaching CMOS Integrated Circuits". *Proceedings of the 3rd WSEAS/IASME International Conference on ENGINEERING EDUCATION*, Vouliagmeni, Greece, July 11-13, 2006, pp.171-176.

[8] Mikula,J., Dostál,T., "A design to capacitor-switched networks using MC graphs". *Electronic horizont*, 42(6), 1987, pp. 560-566.

[9] Pospíšil, J., Dostál, T. *Electronic circuits and systems I.* BUT Brno, 1991.

[10] Vlach, J., Singhal, K., *Computer Methods for Circuit Analysis and Design.*. Van Nostrand Reinhold, New York, 1994.

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