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A Novel Thermal Modeling of Through Silicon Vias in 3-D IC structures

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Abstract - **Heat mitigation is a major challenge in 3-D IC (Three-Dimensional Integrated Circuit) realization. A study of the analytical thermal behavior of the TSV (Through Silicon Via) is very important. Simple and compact yet other models were found deficient to solve this problem in the literature survey. In this paper resistance networks are used to model the heat transfer of the TSVs, in both vertical and horizontal directions, in simpler and compact models. The accuracy of such models is compared with commercially available CFD (Computational Fluid Dynamics) tool. The error of corrections between the tool and developed models are corrected by multiplication factors, resulted within 4.18% accuracy. Varying the thicknesses of a liner, filer, soldering and substrate materials are studied concerning heat transfer physical behavior of three planar TSV stacked systems. The major purpose is to incorporate both vertical and horizontal thermal resistance networks captured more accurately in heat dissipated paths. Proposed models of TSVs can be used in the active interposer simulations or in the face2face fabrication stacked methods of the 3-D IC structures.**

Keywords— Thermal conductivity, Interposer, Fitting coefficient, Thermal resistance.

I. INTRODUCTION

TSVs are the pillars of the 3-D IC structures. These are used in active and passive interposers. The reason for getting heated is high current that sustained inside the TSV, hence more parasitic effects observed, thus thermal energy generated. TSVs interconnects manufactured using dual damascene procedures, usually with copper, as explained in [1]-[2]. The effects of TSVs, when grouped in arrays, exhibit more electromagnetic and mutual thermal coupling through the silicon substrate, resulting in the degradation of the slew of the signals/clocks. Hence more power consumption can occur as studied in [3]. Thermal Through Silicon Vias (TTSVs) introduced to reduce the temperatures, as one approach to solve thermal challenges [4]. Before that, the thermal generations inside the signal TSVs should be well studied. Such observations conclude that thermal convection of the 3-D ICs is not scaled by stacking [5]-[11]. Demonstrated that via effects must be considered to evaluate accurately the thermal capability of 3-D ICs. Thermal simulations for the TSVs should be done in the multi-planar environment than simulating in single planar, along with intermediate structures taken into consideration, because of the advantages that, eliminating initialization of thermal boundary conditions for every die/plane, with lesser number of iterations, will result in more accuracy [12]-[13].

Physically heat traverse in all directions from the point of the heat source. The novel method of considering the TSV in one-dimensional space found to be insufficient to model heat transfer of the objects involved [14]-[16]. Hotspot models have shown to be efficient for design stages and thermal analysis. Jason and Zhang [17], formulate the TTSV via minimization problem with temperature constraints as a constrained nonlinear programming problem based on the thermal resistive models. Haihua Su, et al [18] did a full-chip leakage power estimation considering the power supply and temperature variations, can guide sources of the power losses. Ankur Jain, Robert E Jones, et al [19], model the heat and aid in the development of thermal design guidelines for 3-D ICs. Brent Goplen and Sachin, have come up with an efficient thermal-via-placement method [20]. Resulting thermal-via placements have lowered the temperatures and thermal gradients with minimal use of thermal vias, John H. Lau et al [21], concluded that, distinguished pairs of staggered heat sources on the 3-D TSV chips lead to better thermal performance than the pair of overlapped heat sources. Jos´e L. Ayala, et al [22], proposed an effective mechanism to optimize the thermal profile of 3-D integrated systems, with the use of a Nano-grid of TSVs. Accurate modeling of the thermal effect has been developed in a 5-tier 3-D IC stack. Later, they proposed the capability of a nanostructure of thermal through-silicon vias to improve the thermal response of the 3-D systems.

Madhavan. Swaminathan, et al [23] from Georgia university discussed the novel electrical design challenges for 3-D integrations, which helps in addressing the thermal issue as one of the major challenges. This discusses the electrical modeling of the interposer is not only trivial, due to lossy and semiconducting behavior and temperature effect. Electrothermal modeling of through silicon via interconnects, using the partial-element equivalent-circuit (PEEC) method was discussed by Xiao-Peng Wang et al [24].

Therefore, the research gap related to the present investigation is lack of simple models, lateral conduction given less importance and heat losses ignored in the 3-D stacks, where the TSVs join from one plane to another. The present paper considers heat transmission in all the direction, by representing in lateral and vertical directions to capture this physical phenomenon, in simple and compact models. The developed models are considered the physical structures of the components and material parameters to match in the industry.

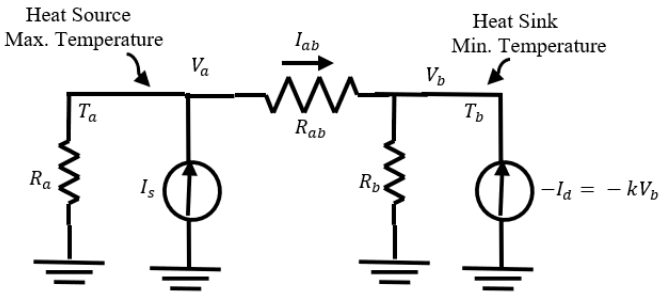

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Fig. 1. Electrical modeling of TSV thermal parameters.

The mesh-based simulation is done by the Autodesk's 2017 versioned CFD tool [25]. Through which, FEM (Finite Element Method) analysis is compared to check the accuracy of the developed models. CFD modeling considers the thermal flow distribution on the structures. The material property and mesh grids and physical structures are major parameters involved in the simulations.

Following section II will have a brief explanation of the single plane thermal models in comparison with multi-mode multi-planar models. Section III discusses the thermal performance of the TSV parameters, with various results observed using computations and CFD tool readings. Relevant conclusions and summary are drawn in section IV.

Nomenclature:
Subscripts and Symbols

R_1, R_4, R_7 = resistances of the silicon substrates (Ω)
R_s = resistance of the heatsink (Ω)
R_3, R_6, R_9= resistances of the liner (Ω)
R_2, R_5, R_8= resistances of the filler (Ω)
R_x, R_y= resistances of the bonding material (Ω)
R_a, R_c, R_d, R_f = resistances of TSV pads (Ω)
R_b, R_e = resistances of the soldering material (Ω)
δT = temperature difference (℃)
T_0-T_7 = temperature nodes of the 3-D IC stack (No units)
q_1, q_2, q_3 = voltage sources (W/mm^3)
x_1, x_2 = fitting coefficients (No Units)
A_0 = footprint of experimental area (um^2)
A = larger area of the silicon substrate (um^2)
tSi = thickness of the silicon substrate (um^2)
t_D= thickness of the ILD (Inter-Layer Dielectric) layer (um^2)
t_b = thickness bonding layer (um^2)
k_{si} = thermal conductivity of silicon substrate (W/m.K)
k_D = thermal conductivity of ILD (W/m.K)
k_b = thermal conductivity of bonding martial (W/m.K)
k_L= thermal conductivity of liner (W/m.K)
k_f= thermal conductivity of filler (W/m.K)
k_s= thermal conductivity of soldering material (W/m.K)
r = radius of TSV (um)
t_L= thickness of insulator liner (um)
l_{ext}= TSV segment, extended into silicon substrates (um^2)
V_p= volume of TSV pad (um^3)
V_s= volume of soldering bump (um^3)
h= height/thickness of the soldering bump (um)

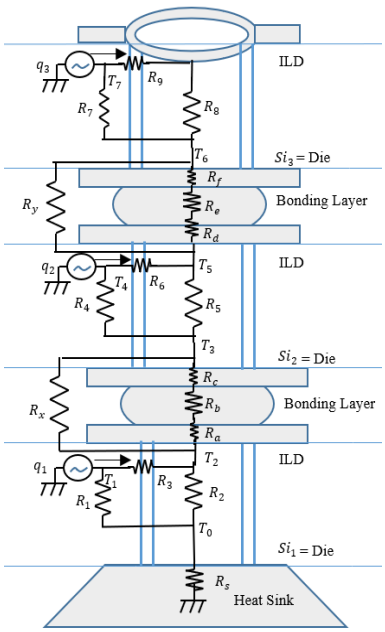
II. COMPACT MODELING OF TSV

Employing the controls system theory, the basic analogy of a physical thermal system can be represented with an equivalent electrical resistance model. The resistance is considered as positive resistance, as per the present realization of sub-micron technology behaviors inside the TSVs. Meaning that as thermal resistance increases to oppose the rate of current. A heat source is analogs to the current source. Mini Ni et al [26], analyze the use of thermal TSVs (TTSV) in reducing the temperatures, in a multi-tier multi-die 3-D system. Electrical voltages are analogous to temperature differences in the circuit. Electrical resistance is analogous to thermal resistance. Current sources are analogous to thermal sources. Thus, the heat transfer phenomenon can be as simplified as shown in Fig. 1. Total heat generated from the heat sources represented by the current source I_s. Total heat dissipated from the circuit represented by drain current I_d. Thus, a voltage-controlled current source in the circuit is the current source I_d. The ambient temperature is represented by circuit ground. The maximum temperature in a 3-D IC stack is located near the heat sources represented by V_a. The minimum temperature is located near the dissipation surfaces of the heat sink, represented by V_b. Hence, obtained the following equations (A) and (B) for the above circuit shown in Fig. 1.

$$I_s = \frac{T_a - T_b}{R_{ab}} + \frac{T_a}{R_a} \quad (A)$$

$$I_d = \frac{T_a - T_b}{R_{ab}} - \frac{T_b}{R_b} \quad (B)$$

In the above system, a decrease in R_{ab} makes a decrease in V_a and an increase in V_b. This means that TTSVs will anyway decrease the maximum heat and increase the minimum heat in a 3-D stack system. Similarly, Kirchhoff's law is applied for the entire three-tier stacking of TSV as shown in Fig. 2a. This shows the entire assembly of the 3-D-planar structure with single TSV, considered in the experimental setup. The group of the TSVs also studied in the later part under the same 3-D-planar structure. The materials and the structure would remain the same even in case of different technologies and dimensions in the various foundries. Hence in this structure, Si_1, Si_2, Si_3 are three dies, along with ILD layers (Inter-Layer Dielectric) interconnected with soldering material, surrounded by a bonding material. Each of 'Si' layer will intern have the BEOL (Back End Of Line) metallization composed internally, as ILD (shown with violet color in Fig. 2b), via TSV. Where there are actual heat sources inside each of the dies (q_1, q_2, and q_3). Different thermal resistances R_1 to R_9 are associated with the structure. T_0-T_7 are different temperature nodes, as shown in Fig. 2a. R_s is the heat sink resistance. On applying Kirchhoff's Current Law (KCL), on this structure, equations could be obtained as further. These thermal resistances based on the physical shape and dimensions of TSVs. The footprint of the experimental step is represented by A_0 area. tSi, t_D, and t_b, are the thickness of the silicon substrate, ILD layer, and bonding



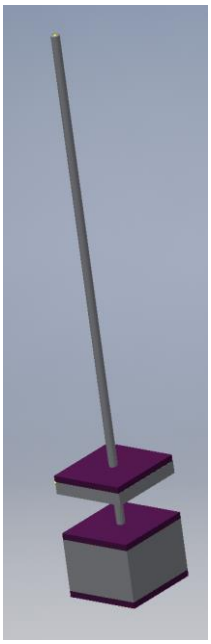


Fig. 2a. Three-tier/planar structure of stacked TSV with analogs electrical resistances. Fig. 2b. Showing Si_2, Si_3, ILD parts of three-tier/planar structure of stacked TSV, structure used in CFD simulations.

$$q_3 = \frac{T_7 - T_6}{R_9 + R_8} + \frac{T_7 - T_6}{R_7} \quad (1)$$

$$\frac{T_7 - T_6}{R_7} + \frac{T_7 - T_6}{R_8 + R_9} = \frac{T_6 - T_5}{R_y} + \frac{T_6 - T_5}{R_f + R_e + R_d} \quad (2)$$

$$\frac{T_6 - T_5}{R_y} + \frac{T_6 - T_5}{(R_f + R_c + R_d)} = \frac{T_5 - T_4}{R_6} + \frac{T_5 - T_3}{R_5} \quad (3)$$

$$q_2 = \frac{T_4 - T_5}{R_6} + \frac{T_4 - T_3}{R_4} \quad (4)$$

$$\frac{T_5 - T_3}{R_5} + \frac{T_4 - T_3}{R_6} = \frac{T_3 - T_2}{R_x} + \frac{T_3 - T_2}{R_a + R_b + R_c} \quad (5)$$

$$\frac{T_3 - T_2}{R_x} + \frac{T_3 - T_2}{(R_a + R_b + R_c)} = \frac{T_2 - T_1}{R_3} + \frac{T_2 - T_0}{R_2} \quad (6)$$

$$q_1 = \frac{T_1 - T_2}{R_3} + \frac{T_1 - T_0}{R_1} \quad (7)$$

$$T_0 = R_s(q_1 + q_2 + q_3) \quad (8)$$

layer respectively. k_{si}, k_s, k_D, k_b, k_L, and k_f are the thermal conductivities of the substrate, soldering, ILD, bonding, liner and filler materials of TSV respectively. r and t_L are the radii of TSV and thickness of insulator liner respectively. In the experimental set up of Fig. 2b, the whole TSV structure does not run through like TTSV inside the 3-D IC stacks, that is entering through the bonding material and substrates.

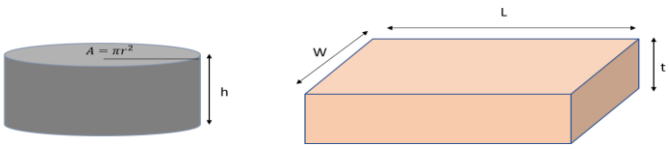


Fig. 3a. A micro bump soldering shapes and its area. Fig. 3b. The pad of the TSVs and its area.

x_1 and x_2 are fitting coefficients used to optimize the thermal resistance models to match the software simulations to decrease the discrepancy of the models from CFD simulations. These can be practically determined by the CFD simulations. Because simulations in turn, consider material property, martial mesh structure, lattice structures including the physical dimensions. Therefore x_1 and x_2 could be used, to compromise above mentioned reasons. Because of the reason that horizontal thermal transfer is more complex as described through R_3, R_6, R_9, R_x, and R_y. 'l_{ext}' is the segment, if TSV extends into the silicon substrate in the first plane. Solving (1)-(8), by the substitution of (11)-(25) results into different nodal temperatures T_0-T_7, in three-planar 3-D IC stacks, using matrices method as in (9).

$$X \times Y = Z \quad (9)$$

Where X matrix represents the resistance values in the equation of temperature nodes from T_0-T_7. Y matrix represents the unknown temperature nodes and the Z matrix represents the sources of thermal energies.

These models can be used to solve any 'N' number of planes. For 'N' planes, 3-D IC structures, R_1 - R_3 are the resistances of TSVs in the first plane. R_4 - R_6 are the resistance of TSVs in the second plane. R_7 - R_9 represents TSV in the third plane, and it can be repeated, for larger scale. R_2, R_5, R_6 are the resistance of filler material. The R_3, R_6, R_9 are the resistance of liner material. R_a, R_c, R_d, and R_f are the resistances of pads of the TSVs, as in Fig 3b. R_b , and R_e are resistances of soldering material. These are short cylindrical micro bump structures, as shown in Fig. 3a. The volume of the pad (15) and the soldering bumps (16) required to subtract in calculating R_x , and R_y resistors, as shown in equation (25). R_x , and R_y are the resistances of bonding materials. In the rest of the paper, let these developed models be called Model M. The little bulging of the soldering sidewalls ignored and considered as a short cylindrical shape for the simplicity of calculations. The loose connections or the voids in soldering bumps lead to huge leakage of current. Therefore, the thermal energy generated will be more, hence considered the resistance of such components as important in this paper. The basic thermal conduction resistance can be calculated as below.

$$R = \frac{Q}{k\,P} \quad (10)$$

Where Q is the length of the conductor, P is the area of the conductor and k is the thermal coefficient of the conducting material. Similarly, all resistors could be obtained as further,

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$$R_1 = \frac{1}{x_1 A}\left(\frac{t_D}{k_D} + \frac{l_{ext}}{k_{si}}\right) \quad (11)$$

$$\text{Where } A = A_0 - \pi(r + t_L)^2$$

$$R_2 = \left(\frac{t_D + l_{ext}}{x_1\, k_f \pi r^2}\right) \quad (12)$$

$$R_3 = \frac{\ln(r + t_L) - \ln r}{2\pi x_2 k_L (t_D + l_{ext})} \quad (13)$$

$$R_4 = \frac{1}{x_1 A}\left(\frac{t_D}{k_D} + \frac{t_{si2}}{k_{si}}\right) \quad (14)$$

$$V_p = tWL \quad (15)$$

$$V_s = \pi r^2 h \quad (16)$$

$$R_5 = \frac{t_D + t_{si2}}{x_1 k_f \pi r^2} \quad (17)$$

$$R_6 = \frac{\ln(r + t_L) - \ln r}{2\pi x_2 k_L (t_D + t_{si2})} \quad (18)$$

$$R_7 = \frac{1}{x_1 A}\left(\frac{t_D}{k_D} + \frac{t_{si3}}{k_{si}}\right) \quad (19)$$

$$R_8 = \frac{t_{si3}}{x_1 k_f \pi r^2} \quad (20)$$

$$R_9 = \frac{\ln(r + t_L) - \ln r}{2\pi x_2 k_L t_{si3}} \quad (21)$$

$$R_s = \left(\frac{t_{si1} - l_{ext}}{x_1\, k_{si}\, A_0}\right) \quad (22)$$

$$R_a = R_c = R_d = R_f = \frac{t}{k_f\, x_1 WL} \quad (23)$$

$$R_b = R_e = \frac{h}{k_s\, x_2 \pi r^2} \quad (24)$$

$$R_x = R_y = \frac{1}{k_b\, x_2}\left(\frac{2t + h}{\ln(A) - (\ln(V_p) + \ln(V_s))}\right) \quad (25)$$

III. RESULT ANALYSIS

The Autodesk toolsets used to draw the polygons and substituted martial constants, to get the analytical simulation results. The experimental setup was made sure, that more than 25000 mesh points were used for each of the components in the assembly. The run time was high because of these more mesh points to get accurate temperatures. Radiation and other effects are ignored. Heat flux is uniform and normal to the top surfaces. Adiabatic boundary conditions are applied on all four sides of the stacked system. In between stacked surfaces are isothermal. Compared CFD results and model values and drew the various graphs.

The footprint area A_0, of the setup used as 100um x 100um. The footprint area A_0, of the setup used as 100um x 100um. The thicknesses of the first silicon die are 500um and l_{ext}=1um. The bottom surface of the heatsink assumed to be 25 °C. The top layers of each plane are having a uniform power density of 700 W/mm^3, with each ILD layer of heat sources with 70W/mm^3. The liner of TSV used is SiO_2 (k_L=1.4W/(m.K)). The materials used [27], for low k dielectrics for ILD (k_D=1.4W/ (m.K)), soldering (k_s=1.0W/(m.K) and bonding (k_b=1.0W/(m.K)) respectively. Since ILD will have the power dissipating metals, k_D is adopted to have the effects of metal within ILD layers. In the following sections, the various components affecting the temperatures inside the TSVs are discussed. The summary of the average error and max errors are listed in Table1.

A. Variation of the filler material radius:

The study of thermal performance is studied by varying the different radii of the filler material as copper used, in the experiments. By considering general manufacturability dimensions the radius of the filler material 'r', varied from 0.5um to 17um. Due to limitation of fabrications the, $tSi_2 = tSi_3$=5um, chosen for $0.5um \leq r \leq 1um$ and $tSi_2 = tSi_3$=45um, chosen for $6um \leq r \leq 17um$. Other parameters are mentioned as shown in Fig. 4a. As the radius (r) thickness of the filler martial (copper) got increased from 0.5um to 17um the temperatures (δT) developed inside the TSV is decreased. But, when $0.5um \leq r \leq 1um$, a rise in temperature observed, because of more lateral thermal conduction happens. Model M achieves the reasonable accuracy with the need of fitting coefficients. Model M follows CFD values. The maximum error between these two models is 12.7% and the average error between the models is 4.7%.

The different temperatures observed at the different nodes as shown in Fig. 2a and Fig 4b. As shown in (12)-(20), the resistances R_2, R_5 and, R_8 significantly decrease, and (non-monotonically) abnormally from T_2, the nodal temperature starts decreasing. As filler material gets thicker than 0.5um-5um temperature variations in T_0-T_7, remain the same inside the 3-D stacked assembly. The highest observed temperature is 58.02℃, and the lower was 46.88℃.

B. Variation of the liner material thickness:

The thickness (t_L) of the liner material SiO_2 is varied from 0.5um to 6um, this results in thermal energy getting accumulated inside the liner material, as shown in Fig. 5a. Other parameters considered are also present in Fig. 5a. Here the maximum difference is 13.15% and the average difference accuracy is 5.2% between Model M and CFD simulations. This shows the behavior of the Model M, is almost matching with the CFD simulations.

As illustrated in (13), (18), (21) the R_3, R_6, R_9 increase as liner thickness increases, resulting in temperature rise. Fig. 5b shows that T_0 - T_2 and T_3 - T_7 nodal temperatures remain in almost constant temperature irrespective of liner thickness, but there is a significant change happen from T_2 - T_3, because, rest

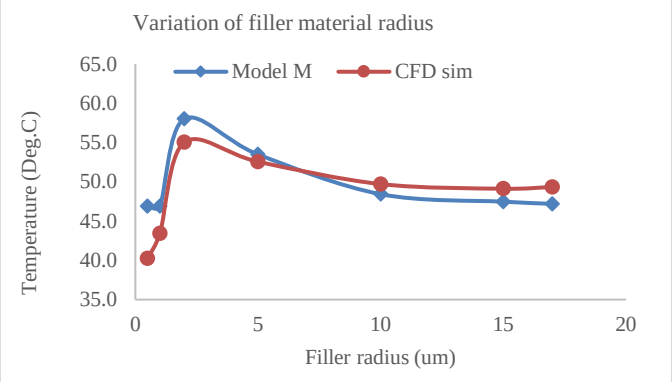

Fig. 4a. Effects of variation of filler material radius in three planar, 3-D IC stacked systems. Other parameters used are, t_L=0.5um, t_D=7um; For 0.5um ≤ r ≤ 5um, $tSi_2 = tSi_3 = 5$um, for 6um ≤ r ≤ 17um, $tSi_2 = tSi_3$=45um. x_1=1.5 and x_2=0.6.

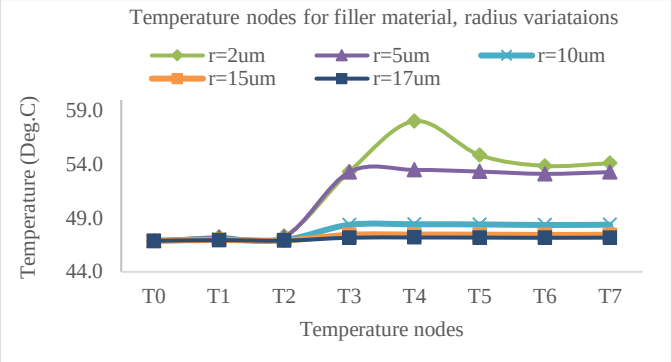

Fig. 4b. Nodal temperature variations, in three planar, 3-D IC stacked systems, when the filler material radius is varied. Other parameters used are, t_L=0.5um, t_D=7um, for 0.5um ≤ r ≤ 5um, $tSi_2 = tSi_3$= 5um. For 6um ≤ r ≤ 17um, $tSi_2 = tSi_3$= 45um. x_1=1.5 and x_2=0.6.

of the nodes are far from the heat sink, also the thermal circuits get ended in these nodes. The highest temperature observed is 53.78 ℃ and the lowest is 53.66℃.

C. Variation of the substrate material thickness:

If the thickness of tSi_2 and tSi_3 are varied the reduction in temperature is observed in the three planar 3-D IC stacked systems as shown in Fig. 6a. Other parameters mentioned in Fig. 6a, to carry out this experiment. Thicknesses within the range, 1um ≤ $tSi_2 = tSi_3$ ≤ 10um, decrease the temperature inside TSV, and for tSi_2 ≥ 20um, temperature difference (δT) increases. As tSi_2 and tSi_3 increase thermal resistance along with a vertical path increase rather than in a horizontal direction. Hence, as specified in (11), (14) and (19), the R_1, R_4, R_7 increase as substrate thickness gets increased, as shown in Fig. 2a. In Fig. 6a. Model M's overall error difference is 12.08% and the average error difference is 4.8%, with the actual simulations.

Fig. 6b gives different nodal temperatures. The maximum value is 49.50℃. The smallest value is 49.36℃. The non-monotonical slope observed at node T_2-T_3, on all variations of the substrate thicknesses, because the more efficient heat sink

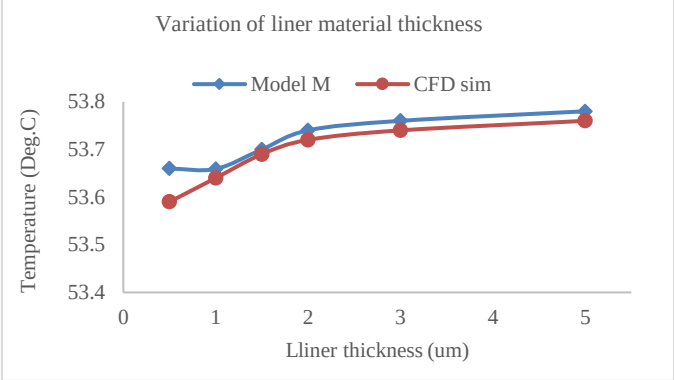

Fig.5a. Effects of variation of liner material thickness in three planar, 3-D IC stacked systems. Other parameters used are, $tSi_2 = tSi_3$= 45um, r=5um, t_D=7nm, for 0.5um ≤ t_L ≤ 5 um. x_1=1.5 and x_2=0.6.

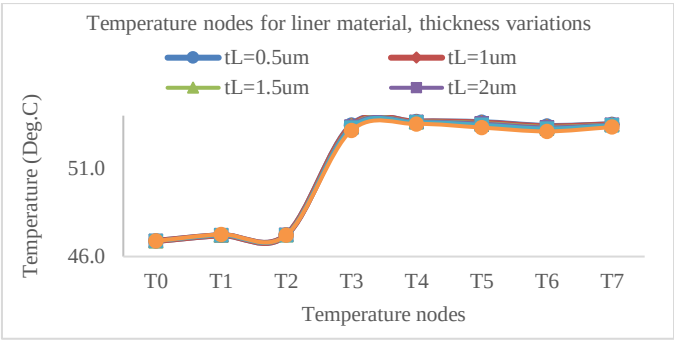

Fig. 5b. Nodal temperature variations, in three planar, 3-D IC stacked systems, when the liner material thickness is varied. Other parameters used are, $tSi_2 = tSi_3$ = 45um, r=5um, t_D=7nm, for 0.5um ≤ t_L ≤ 5um. x_1=1.5 and x_2=0.6.

absorbed heat, from its serial heat sources. Also, the thermal circuits get ended at these nodes.

D. Variation of soldering material thickness:

The soldering material could play an important role while using the bonding layers between the two stacked dies. This is not well studied as a part of thermal circuits in the series of papers referred, so far. This is the major thermal heat component that distributes, heat next to TSV in the stacked assembly. Hence ignoring this may not complete the study of the components involved in the stacking of 3-D IC systems. Fig. 7a covers the effects of thickness variations. Other parameters considered are mentioned in Fig. 7a. As specified in (24) R_b, R_e are the resistance of soldering materials. For 1um ≤ h ≤ 10um, the temperature increases, in a speedy slope, whereas h ≥ 10um, the temperature difference (δT) takes almost the same temperature. This shows that the thermal resistance will decrease or can remain in almost same temperatures, as it allows a more vertical thermal path in its increased thicknesses. Model M's average error is 4.8%, whereas the max error was 12.07%. Fig.7b shows that the nodal value changes as per the thickness of soldering material varied from 1um to 30um.

In Fig.7b, the T_2-T_3 nodes, observe non-monotonical thermal values because of heat sink absorbed temperatures from the heat sources, also the thermal circuits get ended at these nodes. The

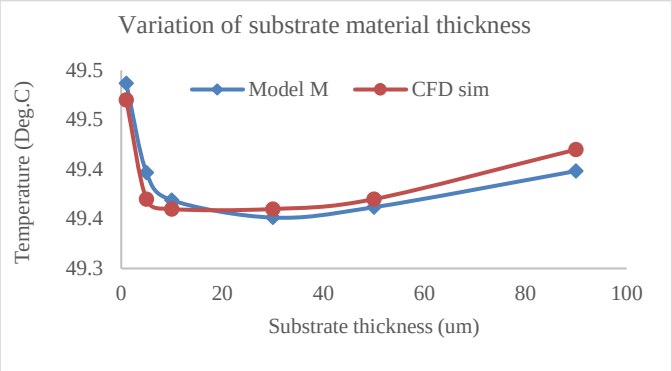

Fig. 6a. Effects of variation of substrate thickness in three planar, 3-D IC stacked systems. Other parameters used are, t_L=1um, t_D=7um, r=8um, for 10um $\leq tSi_2 = tSi_3 \leq$ 90um. x_1=1.5 and x_2=0.6.

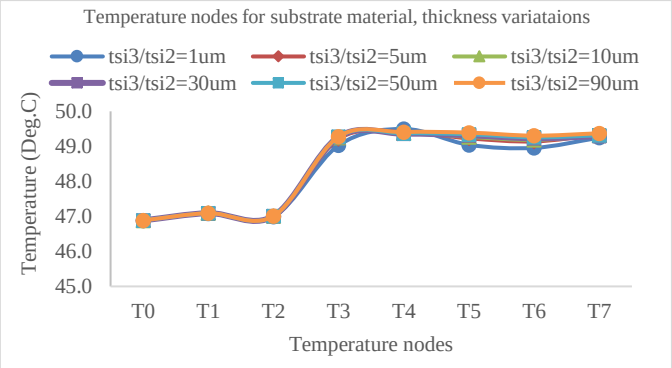

Fig. 6b. Nodal temperature variations, in three planar, 3-D IC stacked systems, when the substrate material thickness is varied. Other parameters used are, t_L=1um, t_D=7um, r=8um, x_1=1.5 and x_2=0.6.

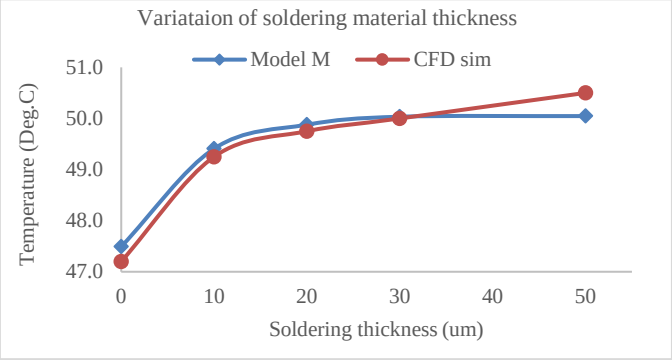

Fig. 7a. Effects of variation of soldering material thickness, in three planar, 3-D IC stacked systems. Other parameters used are, t_L=1um, t_D=7um, r=8um, for 0.5um $\leq$ h $\leq$ 50um. x_1=1.5 and x_2=0.6.

Table I
The Errors And Temperature Observations Summary

Models	Max Error	Avg Error	Max Temp (℃)	Min Temp (℃)
Variation of filler	12.70%	4.7%	58.02	46.88
Variation of liner	13.15%	5.2%	53.78	53.66
Variation of substrate	12.08%	4.8%	49.50	49.36
Variation of soldering	12.07%	4.8%	54.50	47.20
Group of TSVs	7.35%	1.4%	-	-

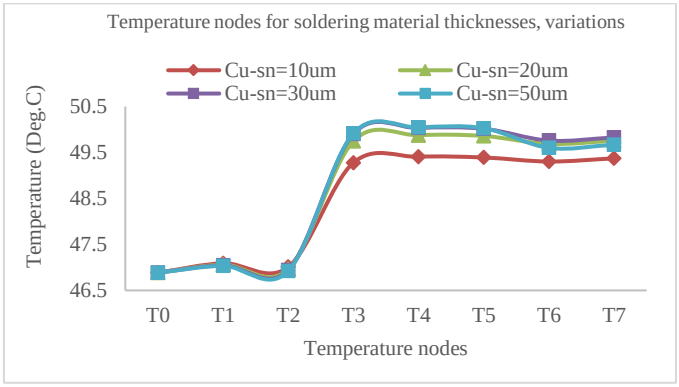

Fig. 7b. Nodal temperature variations, in three planar, 3-D IC stacked systems, when the soldering material thickness is varied. Other parameters used are, t_L=1um, t_D=7um, r=8um, for 0.5um $\leq$ h $\leq$ 50um. x_1=1.5 and x_2=0.6.

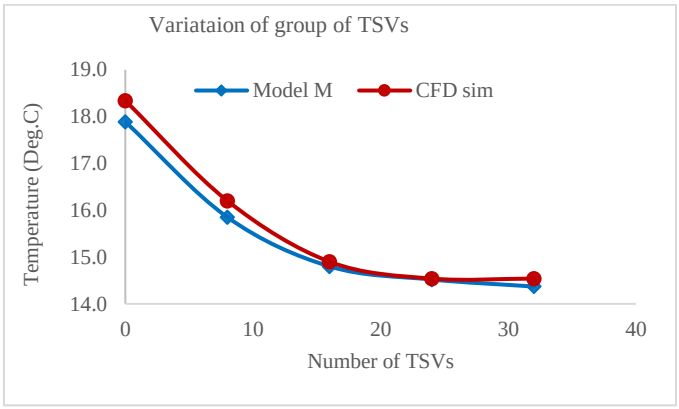

Fig. 8. Temperature variations, in three planar, 3-D IC stacked systems, when multiple TSVs are used instead of single TSVs. Other parameters used are, t_L=2um, t_D=7um, $tSi_2 = tSi_3$=20um, r_0=10um, for 1 $\leq$ n $\leq$ 32. x_1=1.5 and x_2=0.6.

maximum heat dissipated is 54.50 ℃, the minimum observed temperature is 47.20 ℃.

E. Variation of the group of TSVs:

Many studies have been revealed that, instead of a thicker diameter of a single TSV, the thinner diameters of many TSVs can reduce the temperature rise inside the TSVs. Usually, thermal TSV (TTSV) will be used as a solution. But, connecting the same signal net to multiple TSVs, similar to via ladders, or via pillars fashion, as used in the physical design of the chip-making process, can reduce the total resistance as well as improve the EM (Electromigration) and physical strength of the signal nets. Therefore, this experiment is carried out. Where the TSV with radius ' r_0', if divided into 'n' number of the radii of new TSVs should be equal to the original TSVs radius of ' r_0'. Hence $r_n = \frac{r_0}{\sqrt{n}}$. Since the thermal resistance goes into parallel fashion, the total resistance effect will get decreased.

Fig. 8. explains the decrease in temperature difference (δT), as multiple TSVs increased till 32 sets, connecting to the same signal net. Here, the lateral surfaces increase to conduct the heat. Therefore, heat gets divided into multiple TSVs. But it limits to value 'n'. The total error difference is about 7.35%.

Model M's average error differs within 1.4%, compared to CFD simulations.

IV. CONCLUSIONS

Studied literature limitations were lack of simple models. Lateral thermal conduction had been given less importance and heat losses ignored in the 3-D IC stacks, where the TSVs join or connect from one plane to another. Heat dissipation path from the source of heat is not simply the addition of vertical and horizontal resistance networks. It spreads out three-dimensionally. Such a complex phenomenon is fundamentally flawed, by incorporating both vertical and horizontal thermal resistance networks captured in an accurate heat dissipated paths. These models can be extended to a different process with different materials and different geometrical parameters. Different materials will decide the x_1 and x_2 values. The various graphs reveal different facts. The modeled equations follow the commercially available tool simulations, the error correction gets uses of multiplication factors. By increasing the thicknesses of filler material, the thermal resistance decreases, as more heat conducts through the filler material. Another study shows that by increasing the thickness of dielectric material thermal energy increases, inside liner material. Also seen that by increasing the thickness of the substrate martial the thermal issue re-appears, because it must carry the same power developed under all TSVs materials. By increasing the thickness of soldering material, the thermal resistance decreases, as more heat passed through the soldering material, in a vertical path. The group of TSVs effects shows the thermal issue reduces as the temperature gets distributed among other TSVs.

Another important observation is that, in general, the smaller the thickness of filler, liner, soldering and substrate materials the heat conducted more in the horizontal direction than in vertical direction. Conversely, for the higher thickness of the above materials, heat conduction is more in vertical than horizontal directions, hence the abnormal temperature curves observed in the graphs. Thermal residual stresses in silicon can be the scope of further analysis of this paper. In this paper, it has been demonstrated that, presented thermal models can have 4.18% accuracy compared to software simulated values.

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