Simulation and Design of Voltage Controlled Amplifier for Dynamic Expanders

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Abstract— A design of an advanced voltage controlled amplifier made with the aid of electrical circuit simulator Multisim and mathematical computation engine Maple is discussed in this paper. This amplifier is supposed to be used in audio signal processing systems like dynamics expanders and so on. In addition, a block diagram of a complex dynamic volume expander is proposed here.

Keywords— operational amplifier, voltage-controlled amplifier, audio processing, VCA design, volume expander

I. INTRODUCTION

VOLTAGE-CONTROLLED amplifiers (VCAs) are widely used in audio systems for several purposes. In this case a voltage-controlled amplifier was designed in order to be used in audio dynamic expander with the range of 10 dB. Audio recordings are usually processed by dynamic range compression which shall ensure better signal-to-noise ratio and lower demands on the output power of the reproducing device. On the other hand, this compression leads to dynamic range distortion that can, in some cases, end in disruptive effects. Because we usually do not know how the parameters of the dynamic compression were set at the moment of audio signal processing, we are unable to process the reverse expansion. Nevertheless there is still a possibility to make an estimation of these parameters.

Let us expect we have the proper driving unit and need the executing circuit – a low-distortion amplifier the gain of which can be set by the external control voltage. The gain of the VCA is adjustable in the range from 0 to + 10 dB and the amplification factor is linearly dependent on the driving voltage (1 to 3.25 V). There are several possibilities how to achieve this. We could for example employ a CC-CFA application (modified for larger voltages) as shown in [1], or operational transconductance amplifiers [2], but all these concepts seem too complex to this application. Another

Manuscript received June 29, 2011: Revised version received XXXXXX. This work was supported by by the European Regional Development Fund under the project CEBIA-Tech No. CZ.1.05/2.1.00/03.0089 and by the Internal Grant Agency at TBU in Zlin, project No. IGA/45/FAI/10/D.

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possibility, utilizing a discrete BJT differential amplifier driven by the bias current, suffered from insufficient input voltage swing. For these reasons we decided to build a circuit that employs one quad low noise amplifier and a unipolar transistor connected as a driven resistor. The linearity of the unipolar transistor for large audio signals is ensured by the local feedback according to [5] and the linearity of amplification factor dependence on the control voltage is ensured by using a complementary reference amplifier. The accuracy of this kind of linearization is highly dependent on how the device parameters in both amplifiers are matched together. For this reason, several simulations were made to verify the proper function of the circuit. In the physical design it is necessary to ensure the field effect transistors of both amplifiers were placed one near the other so they were of the same temperature. Moreover the field effect transistors shall be paired in order their threshold voltages (and their transfer characteristics) were similar.

II. CIRCUIT DESCRIPTION

This chapter provides a description of the appropriate circuit.

A. General description

Generally, the circuit can be particularized into several blocks, as can be seen in Fig. 1. The basic requirements are as follows:

- The input gain is variable in the range from 10 to + 10 dB.
- At the nominal input voltage of 0.775 V (0 dBu) the overexcitation of the whole circuit must be at least 10 dB.
- The input impedance of the VCA must not be dependent on the control voltage.
- The frequency response must be in a tolerance of 1 dB in the whole audible range considering all operation modes without any dependence on the control voltage.
- Considering the maximum amplification factor of 10 dB, minimal voltage swing of 20 V must be ensured at the output of the circuit. To achieve this, the optimal power supply voltage is around ± 15 V.

The input gain setting is assured by a linear potentiometer being connected in the net of resistors so it acted as logarithmical one. This is because stereo linear potentiometers usually embody better parameters matching of their both channels. Afterwards the signal, the level of which is now set by the input amplifier to the correct level, proceeds to the voltage controlled amplifier VCA 1 where it is amplified by the proper amplification factor. This amplification factor is set by the DC voltage level at the output of the DC control voltage amplifier. The linear dependence of the amplification factor on the input control voltage is achieved by utilizing the negative feedback from the voltage controlled amplifier VCA2 back to the DC control voltage amplifier. The lange amplifier. The VCA2 amplifier only amplifies the accurately set reference voltage. Therefore it gives the information of the amplification factor reached at the appropriate control voltage.



Fig. 1 Block diagram of the VCA

B. Detailed description

The schematic layout of left channel of the circuit (for simplicity, the right channel, which is identical, is not shown here) can be seen in Fig. 4. The circuit employs one connector, SV1, by the help of which it is connected to the main board of the expander. This connector is common to both channels and is connected in a symmetrical way. How the pins are connected can be seen in table 1. The pins in brackets are used by the right channel that is not shown in the Fig. 4.

The input amplifier with variable gain employs the operational amplifier IC1B. This amplifier is connected as a differential amplifier both inputs of which are driven by the input signal. If the appropriate resistor net was ideally balanced, the amplification factor of this amplifier would be $1/\infty$. By connecting a potentiometer to pins 3, 4, 5 we can make this structure disbalanced according to the potentiometer setting. The principle of superposition allows us to form an expression describing how the amplification factor depends on setting the potentiometer:

$$A_{IC1B} = 20 \cdot \log\left(-\left(\frac{R2}{R1 + R2} \cdot \left(1 + \frac{x \cdot P + R5}{(1 - x) \cdot P + R4}\right) - \frac{x \cdot P + R5}{(1 - x) \cdot P + R4}\right)\right) \quad (1)$$

where R1 to R5 are values of the appropriate resistors $[\Omega]$, P is the value of the potentiometer resistance $[\Omega]$ and x is a potentiometer setting factor that belongs to the interval from 0 to 1. The gain of the preamplifier is then expressed in [dB]. Optimal values of the resistors were found by several mathematical calculations applied to (1) in Maple. For the values indicated in Fig. 4 the dependency of amplification factor on setting the potentiometer with a resistance of 100 k Ω can be seen in Fig. 2.



Fig.2 Quasi-logarithmical preamplifier gain adjusting (optimised by Maple)

The signal voltage-controlled amplifier is built with the operational amplifier IC1A. It is also connected as a differential amplifier but the feedback is invariable now. The amplification factor depends on the resistance of T1 transistor. As stated in [2], the amplification factor of such differential amplifier can be expressed like:

$$A_{diff} = 20 \cdot \log\left(\frac{R_a}{R_b}\right) \tag{2}$$

Where $R_a = R11 = R12 [\Omega]$ and $R_b = R8 = R10 [\Omega]$ and A_{diff} is the differential amplifier gain expressed in [dB].

Table 1 SV1 Connector Pinout

Pin	Description
1, (19)	Signal input
2, (20)	Signal output
3, 4, 5, (17, 18, 15)	Gain potentiometer
6, (16)	Control voltage
7, (13)	Output for VU meters (dry signal)
8, (14)	Output for VU meters (wet signal)
9	+ 15 V supply
10	- 15 V supply
11	GND

The lower the internal impedance of T1 is, the lower is the voltage at its drain (the voltage drop on R9 ises). In this configuration, theoretically, the amplification factor can vary from 0 to 3.9. Considering we need to restrain the

amplification factor to the interval from 1 to approximately 3.25, we can deduce the values of several devices. The transistor BF245B achieves a minimal drain-to-source resistance of approximately 200 Ω . Considering possible non-linearity and dispersion of parameters it is reasonable to add 220 Ω R13 resistor to it. Neglecting the influence of resistors R15 and R25, for the output voltage there is the following expression available:

$$A(U_{GS}) = \left(\frac{R12}{R10}\right) \cdot \left(1 - \frac{R14 \cdot \left(\frac{r_{DS_0}}{1 - \sqrt{\frac{|U_{GS}|}{U_p}}} + R13\right)}{R14 + R13 + 1 - \sqrt{\frac{|U_{GS}|}{U_p}}}\right) - \frac{R14 \cdot \left(\frac{r_{DS_0}}{1 - \sqrt{\frac{|U_{GS}|}{U_p}}} + R13\right)}{R14 \cdot \left(\frac{r_{DS_0}}{1 - \sqrt{\frac{|U_{GS}|}{U_p}}} + R13\right)}\right)$$
(3)

Where:

- A(U_{GS}) is the amplification factor as a function of the U_{GS} voltage at the transistor T1 (considering the VCA1 according to Fig. 1) [-].
- R9, R10, R12, R13, R14 are the values of appropriate resistors [Ω] (see Fig. 4).
- U_{GS} is the gate-to-source voltage at the field effect transistor [V]. For the proper function of the circuit it must be lower than 0.
- U_P is the threshold voltage of the appropriate field effect transistor [V].
- r_{DS0} is the minimal internal resistance of the field effect transistor [Ω].

In order the equation (3) could be employed, the following requirements must be fulfilled:

$$R8 = R11 \land R10 = R12 \tag{4}$$

Where R8, R10, R11 and R12 are the values of the resistors applied in the circuit (see Fig. 4) [Ω].

As can be seen, the amplification factor is dependent on the value of U_{GS} and it is obvious that this dependency is not linear. With Maple, the function A(Ugs) for transistors with U_P from -3 to -2.5 V can be displayed according to Fig. 3. The meanings of the quantities displayed at the appropriate axes are as follows: A – amplification factor [-], U_{GS} – gate-to-source voltage at the appropriate transistor [V], U_P – threshold voltage of the appropriate transistor [V].



Fig. 3 Amplification factor A [dB] dependency on Ugs [V] and Up according to equation (3)

Another complication arises from the fact that there exists an influence of the gate-to-source voltage U_{GS} by signal voltage which will produce a perceptible distortion for large signals. This effect and its cancellation is described in [5]. According to [5], the distortion is cancelled by resistors R15 and R25.

Let us briefly describe the mechanisms to be employed when using the FET as a voltage-controlled resistor. The typical N-channel JFET operating characteristics are depicted in Fig. 4.



 V_{DS} – Drain-Source Voltage (V)

Fig. 4 Typical N-channel JFET operating characteristics [5]

According to [5], "for a junction field-effect transistor (JFET) under certain operating conditions, the resistance of the drainsource channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor. Maximum drain-source current, IDSS, and minimum resistance r_{DS}(on), will exist when the gate-source voltage is equal to zero volts ($V_{GS} = 0$). If the gate voltage is increased (negatively for n-channel JFETs and positively for p-channel), the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS}(off)$. Thus the device functions as a voltagecontrolled resistor. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drainto-source is different for each value of gate-source bias voltage. The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low."

The extension of the characteristics shown in the Fig. 4 into the third quadrant can be seen in Fig 5. It is obvious that for small signals the FET transistor can be operated at both polarities while its characteristics remain symmetrical. However, concerning the level of noise it is not convenient to decrease the signal level to approximately 100 mV in order the distortion caused by the FET was cancelled. For larger signals we obtain quite strong distortion. The description of this effect can be found in [5]. This effect is based on the fact that "the channel depletion layer increases as VDS reduces the drain current so that a pinch-off condition is reached when



Fig. 5 Extension of FET characteristics from Fig. 4 [5]

This effect can be cancelled by a simple resistor feedback by feeding the transistor gate with the small amount of the



Fig. 6 Voltage-controlled amplifier circuit diagram

processed signal. "The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the VGS bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the dc gate control voltage and not on the drain signal, unless the VDS = VGS – VGS(off) locus is approached." [5] The mentioned feedback is in the VCA ensured by the resistors R15, R25 and R24, R26.

Moreover, the transistor T1 is driven near its minimal drainto-source resistance the nonlinearity of which is in addition eliminated by adding R13 resistor. When the transistor T1 is nearly closed, its nonlinearity increases but this effect is cancelled by R14 resistor that also determines the minimal amplification factor of the voltage-controlled amplifier. For the proper function of the circuit, only transistors with Up \geq 2.6 V can be used so their function was not affected by large signals up to + 10 dBu.

An auxiliary amplifier of the same construction is made with the operational amplifier IC1D. This amplifier serves to define a dependence of the amplification factor on the control voltage. This amplifier is fed with the DC voltage of 1 V. This level is set by the rotary trimming resistor R27. It is supposed the supply voltage is stabilized and no further reference voltage source is needed though. Let us assume that the amplifiers made with the operational amplifiers IC1A and IC1D are identical, which means that all used components are of zero value tolerances. Then the output voltage of the auxiliary amplifier refers to the amplification factor set by the Ugs voltage of the T2 transistor and this amplification factor indirectly corresponds to the amplification factor of the signal VCA. The output of the auxiliary amplifier serves as a feedback for the DC input amplifier made with the operational amplifier IC1C. This DC amplifier sets the control voltage Ugs of the transistors T1 and T2 to such level in which the output voltage of the auxiliary amplifier is equal to the input control voltage. In other words, if both, the signal and the auxiliary amplifier are of equal characteristics, their amplification factor is equal to the control voltage connected to the PIN6 of the SV1 connector. Obviously, this dependence is only valid for the amplification factors achievable with the appropriate circuit construction. In our case 1 V control voltage refers to the amplification factor of 1 (0 dB) and 3.25 V refers to the amplification factor of 3.25 (+10 dB). To prevent driving the PN junctions of T1 and T2 transistor to their on-state in case the control voltage exceeded the upper boundary there is the diode D1 connected at the output of the IC1D operational amplifier. Its cathode is connected to a potential roughly equal to its junction potential so the transistors cannot be driven by voltages higher than zero. The rotary trimming resistor R30 serves to balance the small differences of the threshold voltages of the T1 and T2 transistors. However, for the proper function of the circuit these transistors should be paired and mounted close each to other in order their temperature was equal. The capacitors C6 and C7 are to cancel the influence of not-symmetrically-set rotary trimming resistor R30 to the feedbacks made with resistors R15, R25 and R24, R26. The capacitor C1 was added after the simulation experiences that proved that the feedback loop tends to oscillate.

III. HARDWARE DESIGN

The printed circuit board of the VCA has been designed with the view of its application inside a complex dynamic expander. The PCB is double-layered and provided with a connector SV1 so the VCA can be plugged into the main board of the expander. As the module is being constructed as a prototype, only cheap and conventional parts has been used. The PCB is drawn with 6.25 mil grid. Trace widths are 12.5 mil as well as the insulation gaps. The right channel was created as a mirrored left-channel pattern. All devices except the rightchannel operational amplifier are top-side mounted. The layouts of the PCB can be seen below. The PCB dimensions are 90 x 45 mm.



Fig. 7 PCB layout (bottom layer)



Fig. 8 PCB layout (top layer)



Fig. 9 Left channel devices layout and vias

IV. SIMULATION RESULTS

Several simulations were made in order to proof the design of the circuit. Firstly only the preamplifier made with the IC1B operational amplifier was checked. Secondly, other simulations were run on the whole circuit as it is shown in Fig. 6.

A. Preamplifier

Several simulations of the preamplifier circuit were made in order to check its gain adjustment, frequency response, distortion, input impedance and output voltage swing. First of all there were 5 AC analyses made in order to verify the frequency response and gain adjustment. These analyses were run for 5 different gain potentiometer settings (0 %, 25 %, 50 %, 75 % and 100 %) at the range of frequencies from 10 Hz to 100 kHz. The result of these analyses can be seen in Fig. 10. The results of the simulation proved that the gain is adjustable from approximately -10.5 dB to approximately + 11 dB and that the control progression is logarithmical. At the worst there is a 0.2 dB attenuation at 100 kHz compared to 1 kHz when the gain is set to + 10 dB.



Fig. 10 Preamplifier frequency response at several gain settings

The distortion was simulated by Fourier analysis at the frequencies of 1 kHz and 15 kHz, in both cases also for 5 gain settings. In all cases the input was fed with 0 dBu sinusoidal signal. The results can be seen in Fig. 11.



Fig. 11 Preamplifier total harmonic distortion versus its gain setting

Defining the input impedance is quite more complicated. To do this an indirect method was used. The complex element of the impedance has been neglected. The input of the circuit was fed with 1 kHz sinusoidal signal the amplitude of which was 1 V and the current through the signal source was measured. Then the input resistance was calculated. It was found that the input impedance varies from 35 to 75 k Ω , depending on the gain setting.

The voltage swing was proved by feeding the circuit with + 20 dBu 1kHz sinusoidal signal when the gain was set to + 10 dB. Smooth limitation at the levels of ± 13.5 V was indicated. This refers to the overexcitation of 21.8 dB.

B. Voltage-controlled amplifier

Simulations of the VCA were carried on the whole circuit shown in the Fig. 6, together with the preamplifier. Throughout the simulations, frequency response of the circuit was checked as well as the dependency of the amplification factor on the input control voltage and its time response to the input control voltage shift. Secondly, noise analyses and distortion analyses were processed.

The frequency response was checked at the preamplifier gain set to 0 dB and the VCA amplification factor set to 0 dB and + 10 dB. The simulation results can be seen in Fig. 12. It is obvious the frequency response is flat it the range of audible frequencies.

The amplification factor dependency on the input control voltage is shown in Fig. 8 and 9. The input of the circuit was fed with 1 kHz 0 dBu sinusoidal signal while the control voltage was changed within the range from 0.75 to 3.5 V. Smooth and steep control voltage changes were applied. The rise and fall periods were considered to be at least 5 and 10 ms because there is no need to change the control voltage faster.



Fig. 12 The whole VCA frequency response at the preamplifier gain set to 0 dB and the VCA amplification factor set to 0 dB and + 10 dB

The noise analysis was made for the 0 dBu input signal, 0 dB preamplifier gain and two VCA amplification factors - 0 dB and + 10 dB. The frequency range was restricted from 200 Hz to 10 kHz and no weighting filter was applied. Compared to the 0 dBu signal level this method helped us to estimate the signal-to-noise ratio to 90 dB at minimal and 86 dB at maximal amplification factor.

To discover how the total harmonic distortion depends on the amplification factor setting, Fourier analyses were processed for amplification factors of 0, +3, +6 and +9 dB with the input sinusoidal signal of 0 dBu level

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Fig. 13 VCA response to the input control voltage (slow sweep)



Fig. 14 VCA response to the input control voltage (fast sweep)

and 1 kHz frequency. The results were as follows: If the amplification factor was lower than 7 dB, the total harmonic distortion was lower than 0.01 %. At the amplification of 9 dB the total harmonic distortion was lower than 0.05 %.

V.PROPOSITION OF DYNAMIC VOLUME EXPANDER

The VCA described in this paper was designed in order to be utilized as a module of a complex dynamic volume expander. In the text below we provide a brief description of the dynamic volume expander project.

A. Intention

The dynamic volume expander is intended for a partial restoration of the compressed audio recordings. It is a hardware device that should serve for audio signal processing experiments.

B. Control elements

Several control elements are supposed to be employed in order the parameters of expansion could be adjusted:

- Master level a potentiometer used to set the gain of the preamplifier of the VCA as mentioned above.
- Output attenuator a potentiometer connected at the output of the VCA that should adjust the level of the expanded signal at the output of the device.
- Threshold a potentiometer adjusting the threshold of the circuit producing the control voltage to drive the amplification factor of the VCA. It adjusts the threshold above which the dynamic expansion is processed.
- Slope a potentiometer adjusting the gain of the circuit producing the control voltage to drive the amplification factor of the VCA. By setting the gain of the controlling



Fig. 15 Dynamic volume expandér block diagram proposition

unit above the preset threshold it defines the strength of the expansion.

- Attack a potentiometer setting the attack time of the controlling circuit.
- Decay a potentiometer setting the decay time of the controlling unit.

C. Expander blocks

The expander should consist of the following block. The block diagram can be seen in Fig. 15.

- Power source unit provides stabilized voltage to all modules.
- Input buffer and filter ensures optimal input impedance of the device and cuts off subsonic frequencies that could affect the controlling circuits of the expander.
- VCA voltage-controlled amplifier described in this paper in full details.
- Four channel rectifier signal rectifier obtaining the levels of the stereo audio signal before and after the expansion.
- Output buffer output amplifier driving the connected devices and/or headphones.
- Controlling unit a circuitry driven from the rectifier, processing the control voltage for the VCA according to the adjustment of Threshold, Slope, Attack and Decay parameters.
- Four channel VU meters displaying the levels of the signal before and after the expansion.
- Control elements

VI. CONCLUSION

In this paper the design of the voltage controlled amplifier that is suitable for dynamic volume expanders is described. The design was processed with the aid of several software tools, mainly Maple and Multisim. The simulation results are incorporated in this paper as well as the proposition of the dynamic volume expander that could employ the described VCA.

ACKNOWLEDGEMENT

This work was supported by by the European Regional Development Fund under the project CEBIA-Tech No. CZ.1.05/2.1.00/03.0089 and by the Internal Grant Agency at TBU in Zlin, project No. IGA/45/FAI/10/D.

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