An Equation-Based Circuit Design Technique for DC/DC Converters with Symbolic Computation System

Tamiyo Nakabayashi, Keiji Nakabayashi, and Fujio Kako

***Abstract*—**We present a new technique of equation-based circuit design for DC/DC converters. It models the characteristics on frequency domain of a buck DC/DC converter with a loop compensation, and expresses as a transfer function. And it optimizes efficiently design parameters of MLCC capacitor, which is a kind of output capacitors, in order to satisfy the circuit design specification. We implemented the technique as an equation-based design program for buck DC/DC converters using Scilab. Our experimental results demonstrate that our technique has the capacity of dealing with the practical industrial design/analysis, and its performance is superior to that of a power electronics circuit simulator.

***Keywords*—**buck DC/DC converter, MLCC capacitor, loop compensation, equation-based circuit design, transfer function, Scilab.

I. Introduction

DC/DC converters are very important electronic circuits for power management ICs. They convert one input direct current (DC) voltage level, and generate another output DC voltage level. And they have been widely used in portable electronic devices such as smart phones and personal computers that are supplied with power from batteries. Today, DC/DC converters are essential parts of ECU (Engine Control Unit) for automotive application [9]-[10],[24]-[26]. In this paper, we present a new technique of equation-based circuit design for DC/DC converters. We briefly review previous main research activities with respect to equation-based circuit design.

In the area of analog electronic circuits, so far several methods of equation-based circuit design have been proposed for efficiency of the circuit design. In particular a method using GP (Geometric Programming) has attracted considerable attention [19]-[21], [31]-[32]. The method simplifies the circuit equations and device model equations into first-order or second-order approximations, and formulates a circuit design problem as a constrained optimization problem. It applies a global optimization algorithm by GP in order to solve the problem, and obtains optimized design parameters (equations parameters) for the circuit design specification. This method using GP has been applied in CMOS circuit designs such as op-amps (operational amplifiers) [19]-[21], [31]-[32], pipelined ADC [37], and DC/DC buck converter [36]. However the method has the disadvantages of being not able to deal with non-convex problems that are important in many design cases, and causes errors between optimized results and circuit simulation results in deep-submicron devices region [18].

On the other hand, an equation-based method with symbolic analysis has been proposed. The scope of this method is restricted to the analysis of linear or weak nonlinear circuits in such frequency domain as the Laplace domain (s-domain) and the z-domain. It extracts a mathematical representation for the circuit in terms of the transfer functions by using symbolic computation (symbolic manipulation). The transfer functions extracted are implemented into computer algebra system, such as Mathematica, and the frequency and phase responses of the circuit are computed [22]-[23].

In the research of [23], the concepts and techniques of symbolic analysis for analog circuits are introduced, and are implemented as a symbolic simulator program called ISAAC (Interactive Symbolic Analysis of Analog Circuits), which have been developed by Katholieke University Leuven. ISAAC is able to analyze lumped, linear, time-invariant circuits in the complex frequency domain, and return the circuit symbolic transfer functions and the circuit elements represented by symbols. In the research of [22], the capabilities of computer algebra systems (CAS) are illustrated by application examples in analog circuit design, such as a low pass filter, a BJT amplifier, and an LC ladder.

Furthermore, in the research of [16], the basic principle of symbolic circuit analysis is presented. And it is discussed the implementation technique using a computer algebra tool Mathematica. In the research of [42], new software for symbolic analysis and symbolic designs of signal processing system (digital filter) is presented, and is implemented into Mathematica. Recently some tools for analog circuit design and simulation using symbolic circuit analysis have been developed [13]-[15]. In the research of [38], as a new attempt, it has been proposed a new symbolic verification methodology for analog and mixed signal (AMS) design, and has been applied in a third order Delta-Sigma (DS) modulator.

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However in the equation-based method with symbolic analysis described above, in most cases, the targets of analysis are limited to relatively simple linear analog circuits such as RLC ladder, op-amps, analog filter, and digital filter (z-domain) [13]-[16], [22]-[23], [38], [42]. It does not deal with practical industrial analog circuit design. And, the differences of results between symbolic circuit analysis and numerical circuit simulation also have been not adequately verified.

In the area of DC/DC converters, a few symbolic analysis program packages have been developed. They generate the averaged model automatically, from a netlist composed of a converter topology and some inputs describing the operation of the converter, and simulate it [17], [39]-[41]. However the disadvantage of this model is that it does not consider the feedback control loop for phase compensation used in DC/DC converters.

So far, in our research of [12], we have developed a simplified circuit model equation for describing the characteristics of a DC/DC converter including a (switching) feedback control loop. And we have presented a technique optimizing circuit model parameters in order to satisfy a design specification by using a computer algebra program Mathematica [29]. The feedback control loop is a most essential part in DC/DC converters. The adjustment of the frequency response of this feedback control loop, which is called loop compensation, is needed to assure loop stability and optimize the transient response of the power supply. The frequency response is determined by the gain, phase, and crossover frequency of the loop reaction to the changes in load current at all frequencies. A Bode Plot is used to show the gain and phase of the frequency response [12], [17], [44].

The loop compensation is very sensitive to the characteristics of the output capacitor in the feedback control loop. The gain of the loop is largely dependent upon an effective capacitance in the output capacitor. And the phase margin is largely dependent upon a stray resistance, which is called ESR (equivalent series resistance), in the output capacitor.
Therefore, in the circuit design of DC/DC converters, an optimal output capacitor is needed in order to stabilize the loop [1]-[4], [5]-[8], [11], [33]-[35], [44]. Furthermore, the ESR influences also the ripple output voltage [43].

Under the above mentioned background, we propose an equation-based circuit design technique for DC/DC converters. In particular, it focuses on the optimization of the parameters in the output capacitor, which is composed of the ESR and the effective capacitance. The technique we present can be applied to a wide variety of DC/DC converter. But in this work, first we consider a buck converter that has a loop compensation system called as type III-B Compensator [1], [3], [4], as a typical case of Step-down DC/DC converter, and derive a detailed transfer function to model accurately the characteristics in the frequency domain (s-domain). Next we consider the relationship between the ESR and the effective capacitance with respect to MLCC (Multi Layer Ceramic Capacitor) capacitor [5], [33]-[35], which is a kind of output capacitors. And, we develop a new optimization procedure using a parameter sweep technique and apply it to the combination of the transfer function and the governing equation of ESR, and determine the optimal MLCC capacitor to satisfy the design specification of the buck DC/DC converter.

We implemented our technique described above into Scilab [30] as an equation-based design program for buck DC/DC converters. In our experiments, we applied the program to the circuit design of a practical industrial buck DC/DC converter, and obtained frequency responses by sweeping the parameter that is correspond to the ESR and the effective capacitance of MLCC capacitor. And we selected the optimal parameter to be satisfied the design specification.

Furthermore, as the comparison with existing circuit simulation method, under the same conditions and settings, we ran frequency-domain analysis in netlist-level on a power electronics circuit simulator, which is called as SIMPLIS [27]. The results of frequency responses by our program are in accord with those of the circuit simulator. This implies that our technique produces correct results. And our program is 70 times faster than SIMPLIS. These results demonstrate that our technique has the capacity of dealing with the practical industrial design/analysis, and its performance is comparable to that of the power electronics circuit simulator.

In the next section, we explain a buck DC/DC converter that has a loop compensation called as type III-B Compensator, and derive an accurate transfer function. Section III describes the characteristics of MLCC capacitor. Section IV describes our technique for the optimization of MLCC capacitor, and implements it into Scilab. Section V describes our experiments and compares the results. We conclude the paper in Section VI.

NOMENCLATURE

f Frequency domain [Hz]
s Complex number in the Laplace transform [-]
R_{ESR} ESR (equivalent series resistance) of the output capacitor [V]
C_o Effective capacitance of the output capacitor [F]
DF Dissipation factor of the output capacitor [-]
α_{ESR} Fitting parameter of the output capacitor [-]
V_{in} Input voltage of the buck converter [V]
V_{out} Output voltage of the buck converter [V]
I_o Maximum output current [A]
V_{osc} Peak to peak amplitude of the oscillator of the PWM (pulse width modulation) [V]
d Duty ratio of the output pulse of the PWM [-]
V_e Output voltage of the error-amplifier [V]
V_{ref} Reference voltage the error-amplifier [V]
R_{Load} Load resistance [Ohm]
F_s Switching frequency [Hz]
F_0 Unity gain frequency (Zero cross frequency) [Hz]
F_{LC} Double pole at the resonance frequency of the LC filter [Hz]
F_{ESR} Zero produced by the ESR of the output capacitor [Hz]
$G_p(s)$ Transfer function of the power stage

$G(s)$ Transfer function of the power stage including the PWM
$W(s)$ Transfer function of the PWM generator
$H(s)$: Transfer function of the compensation network
$M(s)$: Transfer function of the whole loop gain of the buck converter
F_{z1} First zero of the compensation network [Hz]
F_{z2} Second zero of the compensation network [Hz]
F_{p1} First pole of the compensation network [Hz]
F_{p2} Second pole of the compensation network [Hz]
F_{p3} Third pole of the compensation network [Hz]
C_{c1} First capacitor of the compensator [F]
C_{c2} Second capacitor of the compensator [F]
R_{c1} First resistor of the compensator [Ohm]
R_{f1} First feedback resistor of the compensator [Ohm]
R_{f2} Second feedback resistor of the compensator [Ohm]
R_{f3} Third feedback resistor of the compensator [Ohm]
C_{f3} Feedback capacitor of the compensator [F]
Θ Maximum phase lead of the compensator [degree]

II. Our Equation Based Modeling

A. Buck Converter

Buck converters are also called Step-down converters. They are used to step a input direct current (DC) voltage down from a higher level to a lower level. We consider a synchronous buck converter with voltage-mode control and voltage-mode error-amplifier as depicted in Fig. 2.1. The synchronous buck converter is composed of two power MOSFETs, an output inductor, an output capacitor, and a feedback control loop for phase compensation. This specific buck topology derives its name from the control method of the two power MOSFETs. The on-off control is synchronized in order to provide a regulated output voltage. And it prevents that the two power MOSFETs turn on at the same time. The feedback control loop is composed of an error-amplifier, a type III-B compensation network (type III-B Compensator [1]), and a PWM generator.

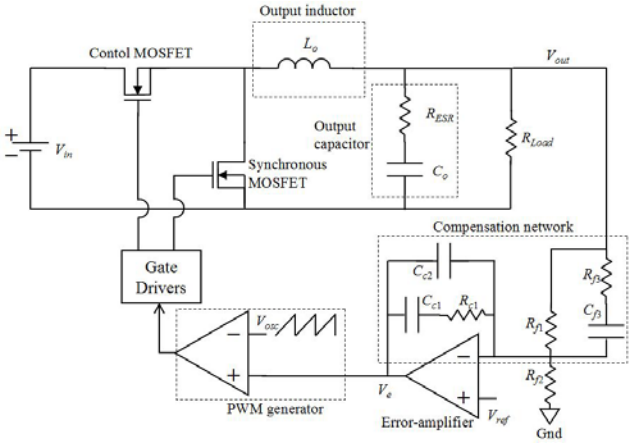


Fig. 2.1: Circuit schematic of a synchronous buck converter with a voltage-mode error-amplifier.

B. Transfer Function

The circuit of the synchronous buck converter depicted in Fig. 2.1 is able to be modeled with large three blocks. Figure 2.2 depicts the block diagram of the synchronous buck converter. The power stage ($G_p(s)$) comprises the two power MOSFETs, the drivers the output inductor, the output capacitor and the load resistance. The model of the PWM generator ($W(s)$) is expressed as the reciprocal of the peak to peak amplitude of the oscillator (V_{osc}) [1]. The compensator block ($H(s)$) is composed of the error-amplifier and the compensation network as depicted in Fig. 2.3. Furthermore, the power stage including the PWM ($G(s)$) is defined as a product of $W(s)$ and $G_p(s)$.

In the following, we derive these transfer functions. Note that we omit a detail explanation of the derivation of the transfer functions.

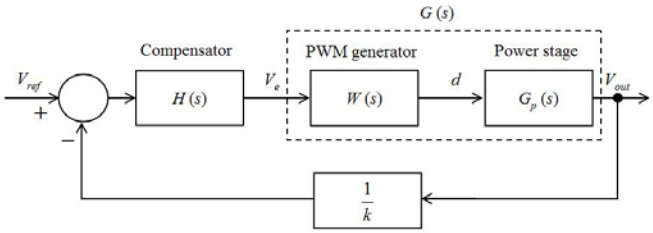


Fig. 2.2: Block diagram of the synchronous buck converter.

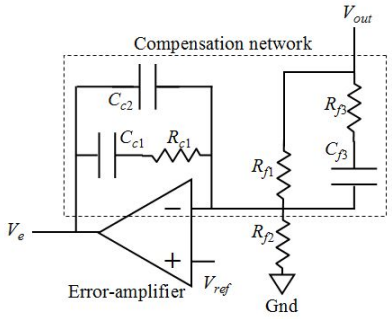


Fig. 2.3: Type III-B compensator

First we derive the transfer function of the power stage ($G_p(s)$) expressed as Eq. (2-1).

$$G_p(s)=\frac{V_{out}}{d}(s) = \frac{R_{Load}\left(sC_oR_{ESR}+1\right)}{s^2L_oC_o\left(R_{Load}+R_{ESR}\right)+s\left(L_o+C_oR_{Load}R_{ESR}\right)+R_{Load}}\times V_{in} \quad (2\text{-}1)$$

Under the condition of Eq. (2-2), we obtain the equation (2-3).

$$R_{Load} >> R_{ESR} \quad (2\text{-}2)$$

$$\frac{R_{Load}}{R_{Load}+R_{ESR}} \approx 1.0 \quad (2\text{-}3)$$

Furthermore, under the condition of Eq. (2-4), we obtain the equation (2-5).

$$L_o + C_o R_{Load} R_{ESR} << R_{Load} + R_{ESR} \tag{2-4}$$

$$\frac{\left(L_o + C_o R_{Load} R_{ESR}\right)}{R_{Load} + R_{ESR}} \approx 0.0 \tag{2-5}$$

Hence, the denominator in Eq. (2-1) is able to be approximated as given below.

$$\begin{aligned} & s^2 L_o C_o \left(R_{Load} + R_{ESR}\right) + s\left(L_o + C_o R_{Load} R_{ESR}\right) + R_{Load} \\ & = \left(R_{Load} + R_{ESR}\right)\left\{ s^2 L_o C_o + s\frac{\left(L_o + C_o R_{Load} R_{ESR}\right)}{R_{Load} + R_{ESR}} + \frac{R_{Load}}{R_{Load} + R_{ESR}} \right\} \\ & \approx \left(R_{Load} + R_{ESR}\right)\left(s^2 L_o C_o + 1\right) \end{aligned} \tag{2-6}$$

Therefore, we rewrite Eq. (2-1) and obtain the following equation (2-7).

$$G_p(s) = \frac{V_{out}}{d}(s) \cong \frac{R_{Load}\left(sC_o R_{ESR} + 1\right)}{\left(s^2 L_o C_o + 1\right)\left(R_{Load} + R_{ESR}\right)} \times V_{in} \tag{2-7}$$

The root of the numerator in Eq. (2-7) is the zero of the transfer function of the power stage. Similarly the roots of the denominator in Eq. (2-7) are the poles of the transfer function the power stage. The transfer function of the power stage has a double pole at the resonance frequency of the LC filter, and has a zero produced by the ESR of the output capacitor. The frequency of the double pole and the frequency of the zero are given by Eqs. (2-8) and (2-9), respectively. In particular, the frequency of the zero is an essential parameter of the output capacitor and depends on the kind of the capacitor used.

$$F_{LC} = \frac{1}{2\pi\sqrt{L_0 C_0}} \tag{2-8}$$

$$F_{ESR} = \frac{1}{2\pi C_o R_{ESR}} \tag{2-9}$$

As mentioned above, the transfer function of the PWM generator (W (s)) is expressed as Eq. (2-10). And the power stage including the PWM (G (s)) is expressed as Eq. (2-11).

$$W(s) = \frac{1}{V_{osc}} \tag{2-10}$$

$$G(s) = G_p(s) \times W(s) = G_p(s) \times \frac{1}{V_{osc}} \tag{2-11}$$

The transfer function of the compensator block (H (s)) is expressed as Eq. (2-12). Note that it is modeled by the impedance ratio as depicted in Fig. 2.3.

$$\begin{aligned} H(s) = \frac{V_e}{V_{out}} &= -\frac{\frac{1}{sC_{C2}} // \left(R_{C1} + \frac{1}{sC_{C1}}\right)}{R_{f1} // \left(R_{f3} + \frac{1}{sC_{f3}}\right)} \\ &= -\frac{\left(sR_{C1}C_{C1} + 1\right) \times \left[sC_{f3}\left(R_{f1} + R_{f3}\right) + 1\right]}{sR_{f1} \times \left(C_{C1} + C_{C2}\right) \times \left[1 + sR_{C1}\left(\frac{C_{C1}C_{C2}}{C_{C1} + C_{C2}}\right)\right] \times \left(sR_{f3}C_{f3} + 1\right)} \end{aligned} \tag{2-12}$$

Under the condition of Eq. (2-13), we obtain the equation (2-14).

$$C_{C1} >> C_{C2} \tag{2-13}$$

$$\frac{C_{C1}C_{C2}}{C_{C1} + C_{C2}} \cong C_{C2} \tag{2-14}$$

Therefore, we rewrite Eq. (2-12) and obtain the following equation (2-15).

$$H(s) = \frac{V_e}{V_{out}} \approx -\frac{\left(sR_{C1}C_{C1} + 1\right) \times \left[sC_{f3}\left(R_{f1} + R_{f3}\right) + 1\right]}{sR_{f1} \times C_{C1} \times \left(1 + sR_{C1}C_{C2}\right) \times \left(sR_{f3}C_{f3} + 1\right)} \tag{2-15}$$

The roots of the numerator in Eq. (2-15) are the zeros of the transfer function of the compensator. Similarly the roots of the denominator in Eq. (2-15) are the poles of the transfer function the compensator. Thus, the compensator has two zeros and three poles as given below:

$$F_{Z1} = \frac{1}{2\pi R_{C1}C_{C1}} \tag{2-16}$$

$$F_{Z2} = \frac{1}{2\pi C_{f3}\left(R_{f1} + R_{f3}\right)} \tag{2-17}$$

$$F_{p1} = 0 \tag{2-18}$$

$$F_{p2} = \frac{1}{2\pi R_{f3}C_{f3}} \tag{2-19}$$

$$F_{p3} = \frac{1}{2\pi R_{C1}C_{C2}} \tag{2-20}$$

Finally, the transfer function of the whole loop gain of the buck converter depicted in Fig. 2.2 is given below.

$$M(s) = \frac{1}{k} \times H(s) \times \frac{1}{V_{osc}} \times G_p(s) = \frac{1}{k} \times H(s) \times G(s) \tag{2-21}$$

where $1/k$ represents the gain of the resistor divider that is used in the feedback loop when $V_{out} > V_{ref}$. Note that the effect of this term $1/k$ is considered in Eq. (2-12), and the term is canceled.

III. MLCC Capacitor

MLCC (Multi Layer Ceramic Capacitor) capacitors are a kind of output capacitors [5], [33]-[35]. They are used in the buck DC-DC converters using the type III-B compensator [1], [3], [4].

The MLCC capacitor is modeled as a serial connection that is composed of an effective capacitance and a stray resistance called ESR (equivalent series resistance). This model is an equivalent circuit depicted in Fig. 3.1. The gain of the loop compensation is largely dependent upon the effective

capacitance. And the phase margin is largely dependent upon the ESR. Therefore, in the circuit design of DC/DC converters, an optimal output capacitor is needed in order to stabilize the loop [5], [33]-[35].

In the following discussion, for simplification, we assume that the characteristics of MLCC capacitor do not depend on its operating condition such as frequency, temperature, and voltage.

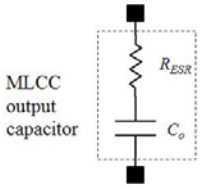


Fig. 3.1: Equivalent circuit model of the MLCC capacitor.

IV. Implementation

We implement the above derived transfer functions (Eqs. (2-7), (2-10), (2-11), (2-15), (2-21)), the frequencies of zeros (Eqs. (2-9), (2-16), (2-17)), and the frequencies of poles (Eqs. (2-8), (2-18), (2-19), (2-20)) into Scilab. Similarly, we implement Eq. (2-23). Scilab is free and open source software for numerical computation providing a powerful computing environment for engineering and scientific applications [30]. In the implementation, we use the transfer function representations of Scilab.

The main purpose of this work is to find an optimal MLCC capacitor that satisfies the circuit design specification of DC/DC converter. First we check the characteristic listed in the data sheet of the MLCC used in the circuit design. Next we sweep the value of effective capacitance of MLCC capacitor, and obtain the corresponding value of ESR. At each combination of ESR and effective capacitance, we calculated the transfer functions mentioned above and obtain the corresponding frequency response in the form of Bode Plot. We repeat this calculation process, and obtain an optimal MLCC capacitor finally. Thus our optimization technique is very simple.

V. Experimental Results

As described above, we derived the system of transfer functions. We develop a source code and implement it into Scilab. The values of main parameters are set in the following: V_{in}=12 [V], V_{out}=1.8 [V], V_{ref}=0.7 [V], V_{osc}=1.8 [V], L_o=1.5e-6 [H], C_o=4×10.8e-6=43.2e-6 [F], R_{ESR}=3e-3/4=0.75e-3 [Ohm], F_s=600e3 [Hz], I_o=4.0 [A], R_{Load}=1.0 [Ohm].

Furthermore, the value of each design parameter in the system of transfer functions is set based on the datasheet and application note [1], which are indicated by International Rectifier [28]. We determine the design parameters in the following procedure.

The poles and zeros of the power stage are calculated by using Eqs. (2-8) and (2-9):

$$F_{LC} = \frac{1}{2\pi\sqrt{43.2\text{e}-6\times 1.5\text{e}-6}} = 19.7\text{e}3\,[\text{Hz}] \tag{3-1}$$

$$F_{ESR} = \frac{1}{2\pi\times 43.2\text{e}-6\times 0.75\text{e}-3} = 4.9\text{e}6[\text{Hz}] \tag{3-2}$$

The zero cross frequency is set to 1/6 of the switching frequency:

$$F_0 = \frac{F_s}{6} = \frac{600\text{e}3}{6} = 100\text{e}3[\text{Hz}] \tag{3-3}$$

Therefore, the frequency condition of type III-B compensator [1] is satisfied as depicted in Eq. (3-4).

$$F_{LC} < F_0 < F_s/2 < F_{ESR} \tag{3-4}$$

The poles and zeros of the compensator are calculated as given below [1]. Note that the maximum phase lead (Θ) of the compensator is set to 70 degree.

$$F_{p3} = \frac{F_s}{2} = 300\text{e}3[\text{Hz}] \tag{3-5}$$

$$F_{Z2} = F_0\times\sqrt{\frac{1-Sin\theta}{1+Sin\theta}} = F_0\times\sqrt{\frac{1-Sin(70)}{1+Sin(70)}} = 17.6\text{e}3[\text{Hz}] \tag{3-6}$$

$$F_{P2} = F_0\times\sqrt{\frac{1+Sin\theta}{1-Sin\theta}} = F_0\times\sqrt{\frac{1+Sin(70)}{1-Sin(70)}} = 567\text{e}3[Hz] \tag{3-7}$$

$$F_{Z1} = \frac{F_{Z2}}{2} = 8.8\text{e}3[\text{Hz}] \tag{3-8}$$

Under the frequency condition mentioned above, we calculate the values of the design parameters of the compensator. First we set the value of parameter C_{f3} to 2.2e-9 farad. The value of parameter R_{f3} is calculated as given below by using Eq. (2-19).

$$R_{f3} = \frac{1}{2\pi C_{f3}F_{P2}} = \frac{1}{2\pi\times 2.2\text{e}-9\times 567\text{e}3} = 127.6[\text{Ohm}] \tag{3-9}$$

We choose $R_{f3} = 127[\text{Ohm}]$. The value of parameter R_{f3} is calculated as given below by using Eq. (2-17).

$$R_{f1} = \frac{1}{2\pi C_{f3}F_{z2}} - R_{f3} = \frac{1}{2\pi\times 2.2\text{e}-9\times 17.6\text{e}3} - 127 = 3.98e3[\text{Ohm}] \tag{3-10}$$

We select $R_{f1} = 4.02\text{e}3[\text{Ohm}]$. The value of parameter R_{f2} is calculated as given below by using Eq. (3-11) [1].

$$R_{f2} = \frac{R_{f1} \times V_{ref}}{V_{out} - V_{ref}} = \frac{4.02e3 \times 0.7}{(1.8 - 0.7)} = 2.56e3[\text{Ohm}] \quad (3\text{-}11)$$

We choose $R_{f2} = 2.55e3[\text{Ohm}]$. The value of parameter R_{c1} is calculated as given below by using Eq. (3-12) [1].

$$R_{c1} = \frac{2\pi \times F_0 \times L_o \times C_o \times V_{osc}}{V_{in} \times C_{f3}} = \frac{2\pi \times 100e3 \times 1.5e-6 \times 43.2e-6 \times 1.8}{12.0 \times 2.2e-9} = 2.77e3[\text{Ohm}] \quad (3\text{-}12)$$

We choose $R_{c1} = 2.74e3[\text{Ohm}]$. The value of parameter C_{c1} is calculated as given below by using Eq. (2-16).

$$C_{c1} = \frac{1}{2\pi \times R_{c1} \times F_{z1}} = \frac{1}{2\pi \times 2.74e3 \times 8.8e3} = 6.6e-9[\text{F}] \quad (3\text{-}13)$$

We choose $C_{c1} = 6.8e-9[\text{F}]$. The value of parameter C_{c2} is calculated as given below by using Eq. (2-20).

$$C_{c2} = \frac{1}{2\pi \times R_{c1} \times F_{p3}} = \frac{1}{2\pi \times 2.74e3 \times 300e3} = 193e-12[\text{F}] \quad (3\text{-}14)$$

Finally we choose $C_{c2} = 180e-12[\text{F}]$.

Figure 5.1 show an example of our implementation using the transfer function representations of Scilab. Figure 5.1 (a) depicts the source code.

As our experimental verification, we ran the simulation source code with Scilab on HP dv9700 (OS Windows 7, CPU Intel(R) Core(TM) 2.5GHz, RAM 8.00 GB). It run time (CPU time) is 2.1 second. Figure 5.1 (b) depicts the simulation results in the frequency domain. The zero crossover frequency is about 105e3 Hz. The gain margin is 18.759 degree. The phase margin is 50.474 degree.

As other reference, we ran frequency-domain simulation in netlist-level on a power electronics circuit simulator, which is called as SIMPLIS [27]. The simulated the circuit of a buck DC/DC converter is depicted in Fig. 5.2 (a). Note that this circuit is equivalent to the system of transfer functions described above. In this case, the run time with the same computer mentioned above is 150.9 second. Figure 5.2 (b) depicts the circuit simulation results obtained by SIMPLIS. The zero crossover frequency is about 113e3 Hz. The gain margin is 13.461 degree. The phase margin is 49.595 degree. Thus the simulation results of our equation-based modeling are almost consistent with those of SIMPLIS. Hence it demonstrates the adequacy of our equation-based circuit design technique. And our technique is 70 times faster than SIMPLIS.

Table I demonstrates the simulation results in the various cases of the combination of ESR and effective capacitance of the MLCC capacitor based on the datasheet [5], which are indicated by TDK-EPC Corporation. Particularly, in the case of (1), the power electronics circuit simulator SIMPLIS is not able to simulate it (no-convergence). On the other hand, our technique can deal with the same case.

The results reveal the superiority of our technique. They also demonstrate that our technique is able to be applied to industrial design of DC/DC converter.

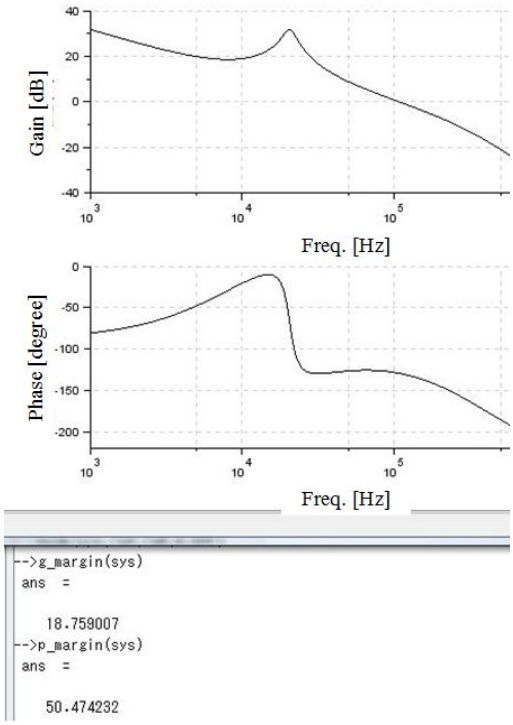
VI. Conclusions

We have proposed a new technique of equation-based circuit design for DC/DC converters. It starts with the modeling of the frequency response of a buck DC/DC converter with a loop compensation, and derive the governing equation of ESR. It then determines the optimal MLCC capacitor that satisfies the design specification of the converter. Furthermore, we applied the technique into the circuit design of a practical industrial buck DC/DC converter. Our technique was demonstrated by experimental results. They also revealed that the technique has the capacity of dealing with the practical industrial design/analysis, and its performance is comparable to that of a power electronics circuit simulator.

In the future work, we have a plan to extend the technique in order to be able to deal with the characteristics on time domain such as output voltage ripple, transient response.

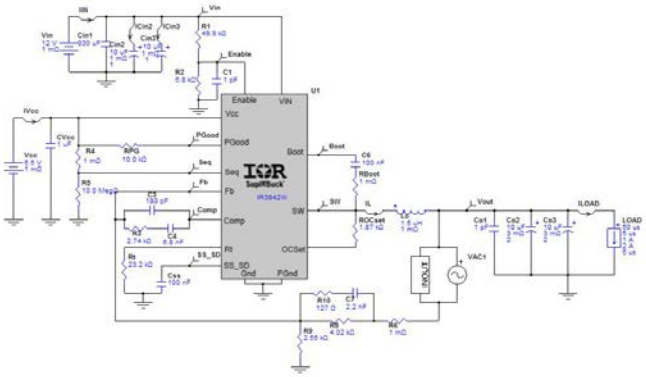
```
//-
// Circuit Parameters
//-
L0=1.5e-6 //[H]
C0=43.2e-6 //[F]
ESR=0.75e-3 //[Ohm]
RLOAD=1.0 //[]
VIN=12.0 //[V]
VOSC=1.8 //[V]
//-
Cf3=2.2e-9 //[F]
Rf3=127.0 //[Ohm]
Rf1=4.02e3 //[Ohm]
Rf2=2.55e3 //[Ohm]
RC1=2.74e3 //[Ohm]
CC1=6.8e-9 //[F]
CC2=180e-12 //[F]
//
// Transfer Funtion
//
s=poly(0,'s');
//Gp: transfer function of a power stage and PWM control
Gp=(RLOAD*(C0*ESR*s+1)*VIN)/(L0*C0*s*s*(RLOAD+ESR)+s*(L0+RLOAD*C0*ESR)+RLOAD) //Gp(s)
//H: transfer function of a type-III-A compensator
H=(1.0+s*RC1*CC1)*(1.0+s*Cf3*(Rf1+Rf3))/(s*Rf1*CC1*(RC1*CC2*s+1.0)*(1.0+s*Rf3*Cf3))
//G: transfer function of a switiching feedback loop
G=H*(Gp/VOSC)
sys=syslin('c',G);
//
// Transient Analysis
//
t=linspace(0,1.0e-3,10000);
y=csim('step',t,sys);
//
// ac analysis
//
xgrid()
xtitle('Freq. Respons','freq(Hz)','Gain/Phase')
bode(sys,1e3,1e8,0.001)
g_margin(sys)
p_margin(sys)
//
```

(a) Simulation source code

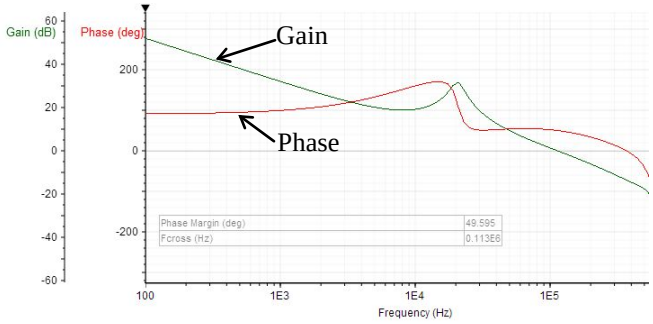


(b) Simulation result

Fig. 5.1: Our implementation using the transfer function representation of Scilab



(a) Schematic



(b) Simulation result

Fig. 5.2: Simulation using SIMPLIS

Table I: The simulation results in the various cases of the combination of ESR and effective capacitance

Case	C_o [μF]	R_{ESR} [mOhm]	Scilab			SIMPLIS		
			Crossover frequency [Hz]	Gain margin [degree]	Phase margin [degree]	Crossover frequency [Hz]	Gain margin [degree]	Phase margin [degree]
(1)	3.0	6.0	2.50E+05	8.044	25.020	NG	NG	NG
(2)	8.0	4.5	1.50E+05	17.219	47.857	1.390E+05	10.825	45.666
(3)	10.0	3.0	1.05E+05	18.759	50.474	1.130E+05	13.461	49.595
(4)	30.0	1.5	4.00E+04	29.076	47.473	4.200E+04	25.558	48.977

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