Modelling and Performance Analysis of Asymmetric Double Gate Stack-Oxide Junctionless FET in Subthreshold Region

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***Abstract*— A modified analytical model for asymmetric Double Gate Stack-Oxide Junctionless Field Effect Transistor (DGS-JLFET) in subthreshold region is presented in this paper. The simulation results obtained from this model are used to make a performance analysis for the described device. The potential distribution and some short channel effects such as on-off ratio (I_{on}/I_{off}), threshold voltage roll-off (TVRO), subthreshold swing (SS) for asymmetric DGS-JLFET in subthreshold region has been observed. Comparative analysis shows that this asymmetric device has better performance than symmetric ones.**

Keywords-Double Gate Stack-Oxide Junctionless Field Effect Transistor (DGS-JLFET), on-off ratio (I_{on}/I_{off}), subthreshold swing (SS), Threshold Voltage Roll-Off (TVRO), Short Channel Effect (SCE).

I. INTRODUCTION

Today's Integrated Circuit (IC) technology is the result of excessive down-scaling of transistor dimension which has been carried out successfully over the last 30 years. But the formation of ultra shallow junctions (USJ) and abrupt junctions which requires novel doping and special annealing techniques, further minimization of device size has become quite challenging. The convention to reduce MOSFET feature size continuously has imposed challenges on device performances. Various short channel effects (SCE) like hot carrier injection, oxide leakage, drain induced barrier lowering (DIBL), subthreshold swing (SS) cause unwanted effects in MOSFET characteristics with the decreasing dimension size [1-5]. So, various non-planar structures with multiple gates and alternate channel materials have been proposed to overcome these problems [6]. Recently Junctionless Field Effect Transistors (JLFETs) have become a better solution for this problem as they need no lateral doping and no concentration gradient which makes fabrication easier. JLFETs provide reduced SCEs like excellent SS, very low leakage current, low DIBL, low TVRO and high I_{on}/I_{off} ratio [7-8] as well, compared to conventional MOSFETs. Several researches have been done on different structures of JLFET like Dual Material Double Gate Stack-Oxide Junctionless Transistor (DM-DGS-JLT), Dual Material Double Gate Junctionless Transistor (DM-DGJLT) and Single Material Double Gate Junctionless Transistor (SM-DGJLT) [9-10]. A junctionless architecture called single material double gate along with stack-oxide junctionless transistor (SM-DGS-JLT) with asymmetric configuration has been proposed is this paper. Here a comparative analysis of the proposed device in subthreshold region has been done using device simulator (COMSOL Multiphysics) and MATLAB. We observed the SCE performance of the proposed structure by taking different combination of high-*k* oxide and changing oxide thickness.

II. MODEL DEVELOPMENT

The structure of the proposed device is shown in Fig. 1.

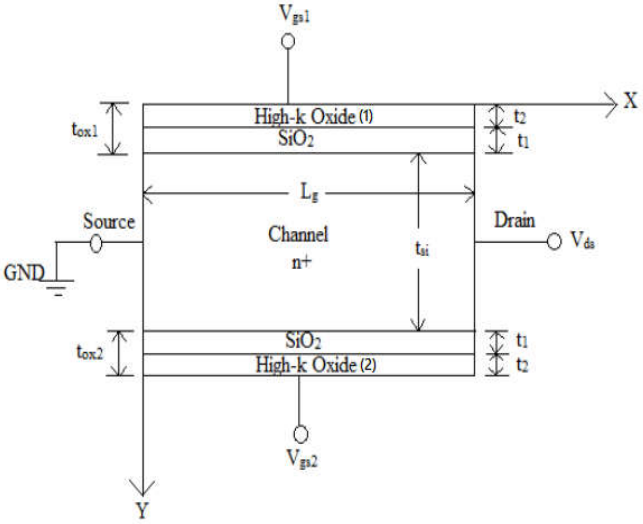

Fig. 1. Structural cross-section of an asymmetric DGS-JLFET

The model has been derived by solving a 2-D Poisson's equation along the channel.

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=-\frac{qN_d}{\epsilon_{si}},\quad \begin{matrix}0\le x\le L_g\\ 0\le y\le t_{si}\end{matrix} \tag{1}$$

where $\phi(x,y)$ is the 2-D channel potential, q is the elementary charge, N_d is the uniform doping concentration in the channel region and ϵ_{si} is the dielectric constant of silicon.

We have neglected fixed oxide charges at oxide/silicon interfaces and the impact of mobile charge on the channel potential for making the model simpler. For developing an equation for channel potential we have assumed cubic potential distribution along the top to bottom gate direction and used appropriate boundary conditions. 1-D capacitance model and 1-D potential line along the source to drain direction at an arbitrary depth are used to make the 2-D Poisson's equation into a simple 1-D second order non-homogeneous differential equation for the potential distribution. Finally, solving for the general solution of ordinary differential equation, we get the equation for surface potential for DGS-JLFET as,

$$\phi(x,y)=\frac{(V_{ds}-\gamma_y)\sinh\left(\frac{x}{\lambda_y}\right)-\gamma_y\sinh\left(\frac{L_g-x}{\lambda_y}\right)}{\sinh\left(\frac{L_g}{\lambda_y}\right)}+\gamma_y \tag{2}$$

Where,

$$\gamma_Y=\alpha_Y+\beta_Y\lambda_Y^2 \tag{3}$$

$$\lambda_Y=\sqrt{\frac{1+\frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}Y-\frac{1}{\epsilon_{si}t_{si}}\left(\frac{2\epsilon_{ox1}}{t_{ox1}}-\frac{\epsilon_{ox2}}{t_{ox2}}\right)Y^2+\frac{1}{\epsilon_{si}t_{si}^2}\left(\frac{\epsilon_{ox1}}{t_{ox1}}-\frac{\epsilon_{ox2}}{t_{ox2}}\right)Y^3}{\frac{2}{\epsilon_{si}t_{si}}\left(\frac{2\epsilon_{ox1}}{t_{ox1}}-\frac{\epsilon_{ox2}}{t_{ox2}}\right)-\frac{6}{\epsilon_{si}t_{si}^2}\left(\frac{\epsilon_{ox1}}{t_{ox1}}-\frac{\epsilon_{ox2}}{t_{ox2}}\right)Y}} \tag{4}$$

$$\alpha_Y=-\frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}V'_{gs1}Y+\left[\frac{1}{\epsilon_{si}t_{si}}\left(\frac{2\epsilon_{ox1}}{t_{ox1}}V'_{gs1}-\frac{\epsilon_{ox2}}{t_{ox2}}V'_{gs2}\right)-\frac{\epsilon_1{\epsilon_2}^2{\epsilon_3}^2(V'_{gs1}-V'_{gs2})(3\epsilon_{si}t_{ox2}+\epsilon_{ox2}t_{si})}{\epsilon_{si}t_{ox2}t_{si}[t_{si}\epsilon_1{\epsilon_2}^2{\epsilon_3}^2+{\epsilon_3}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_2}^2t_1)+{\epsilon_2}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_3}^2t_1)]}\right]Y^2-\left[\frac{1}{\epsilon_{si}{t_{si}}^2}\left(\frac{\epsilon_{ox1}}{t_{ox1}}V'_{gs1}-\frac{\epsilon_{ox2}}{t_{ox2}}V'_{gs2}\right)-\frac{\epsilon_1{\epsilon_2}^2{\epsilon_3}^2(V'_{gs1}-V'_{gs2})(2\epsilon_{si}t_{ox2}+\epsilon_{ox2}t_{si})}{\epsilon_{si}t_{ox2}{t_{si}}^2[t_{si}\epsilon_1{\epsilon_2}^2{\epsilon_3}^2+{\epsilon_3}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_2}^2t_1)+{\epsilon_2}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_3}^2t_1)]}\right]Y^3 \tag{5}$$

$$\beta_Y=\frac{2}{\epsilon_{si}t_{si}}\left(\frac{2\epsilon_{ox1}}{t_{ox1}}V'_{gs1}-\frac{\epsilon_{ox2}}{t_{ox2}}V'_{gs2}\right)-\frac{2\epsilon_1{\epsilon_2}^2{\epsilon_3}^2(V'_{gs1}-V'_{gs2})(3\epsilon_{si}t_{ox2}+\epsilon_{ox2}t_{si})}{\epsilon_{si}t_{ox2}t_{si}[t_{si}\epsilon_1{\epsilon_2}^2{\epsilon_3}^2+{\epsilon_3}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_2}^2t_1)+{\epsilon_2}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_3}^2t_1)]}+\frac{qN_d}{\epsilon_{si}}-\left[\frac{6}{\epsilon_{si}{t_{si}}^2}\left(\frac{\epsilon_{ox1}}{t_{ox1}}V'_{gs1}-\frac{\epsilon_{ox2}}{t_{ox2}}V'_{gs2}\right)-\frac{6\epsilon_1{\epsilon_2}^2{\epsilon_3}^2(V'_{gs1}-V'_{gs2})(2\epsilon_{si}t_{ox2}+\epsilon_{ox2}t_{si})}{\epsilon_{si}t_{ox2}{t_{si}}^2[t_{si}\epsilon_1{\epsilon_2}^2{\epsilon_3}^2+{\epsilon_3}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_2}^2t_1)+{\epsilon_2}^2\epsilon_{si}(\epsilon_1{}^2t_2+{\epsilon_3}^2t_1)]}\right]Y \tag{6}$$

III. Simulation Results And Discussions

Different device parameters for the proposed structure were set at V_{ds} = 0.1V, Gate length, L_g = 50nm, channel thickness, t_{si} = 10nm, and channel doping, N_d = 10^{19}cm^{-3}. The top and bottom gate electrodes were p+ polysilicon for n-type doping, oxide thickness for both SiO_2 and high-k dielectric was 1nm. As this model is asymmetric, the dielectric constants of top and bottom gates are different. The dielectric constant combinations used here are 7-20/7-9/9-20 (k1-k2). The short channel effects have been observed with channel lengths ranging from 20 nm to 60 nm by using different stack oxide thickness and changing dielectric constant combination of stack-oxides using the value of potential distribution from COMSOL.

A. Surface potential distribution

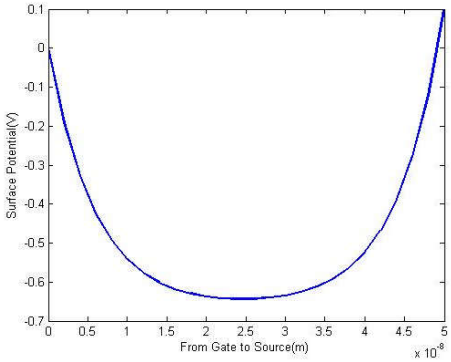

Fig. 2(a). Surface Potential from gate to source with V_{ds}=0.1V, V_{gs}=0V (Asymmetric DGS-JLFET)

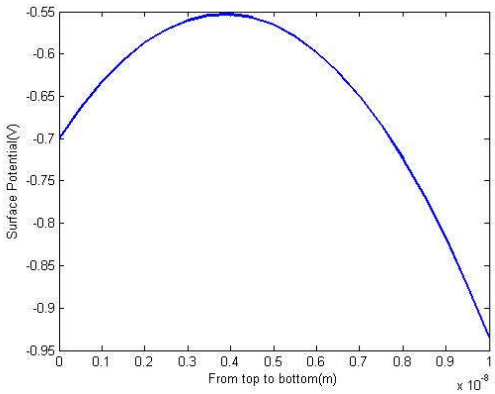

Fig. 2(b). Surface Potential from top to bottom gate with V_{ds}=0.1V, V_{gs}=0V (Asymmetric DGS-JLFET)

Fig. 2(a) and Fig. 2(b) show the potential distributions of asymmetric DGS-JLFET. The potential distribution along source to drain for asymmetric DGS-JLFET shows that it has a minima along the channel. The minima is found at the midpoint of the channel along source to drain. Now, by varying the gate voltage, the minimum potential of channel becomes zero at one value of gate voltage. This voltage is called threshold voltage, V_{th}.

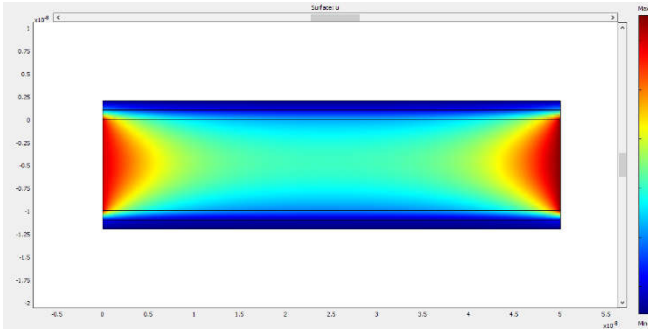

Fig. 3. Surface Potential of Asymmetric DGS-JLFET (V_{gs}=0V, V_{ds}=0.1V)

Fig. 3 shows the surface potential distribution of asymmetric DGS-JLFET simulated by COMSOL Multiphysics.

B. I_{on}/I_{off} ratio

For drain current calculation, the Equation (7) is used [11] as,

$$I_{ds} = \frac{q\mu_n W V_t \left(1 - e^{\frac{V_{ds}}{V_t}}\right)}{\int_0^{L_g} \frac{dx}{\int_0^{t_{si}} n_i e^{\frac{\phi(x,y)}{V_t}} dy}} \quad (7)$$

Fig. 4(a) shows that I_{on}/I_{off} ratio increases with the increase the dielectric constant combination of high-k oxide. Fig. 4(b) shows that I_{on}/I_{off} ratio increases significantly as we decrease the oxide thickness. By decreasing oxide thickness from 1nm to 0.5nm, I_{on}/I_{off} ratio can be improved by more than 10 times.

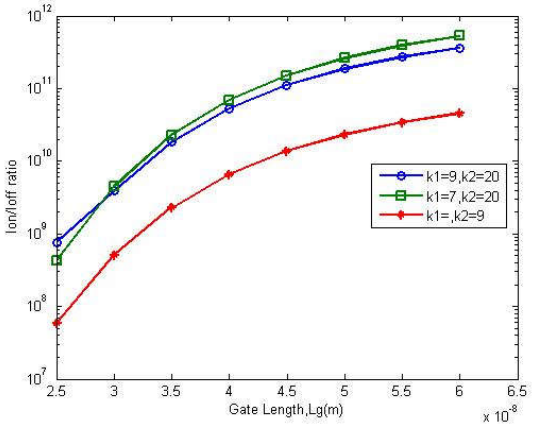

Fig. 4(a).Change in I_{on}/I_{off} ratio of asymmetric DGS-JLFET by changing high-k oxide combination (V_{ds}=0.1 V)

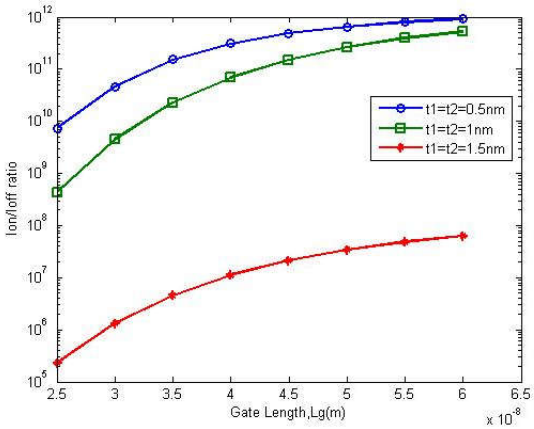

Fig. 4(b). Change in I_{on}/I_{off} ratio of asymmetric DGS-JLFET by changing oxide thickness (V_{ds}=0.1 V)

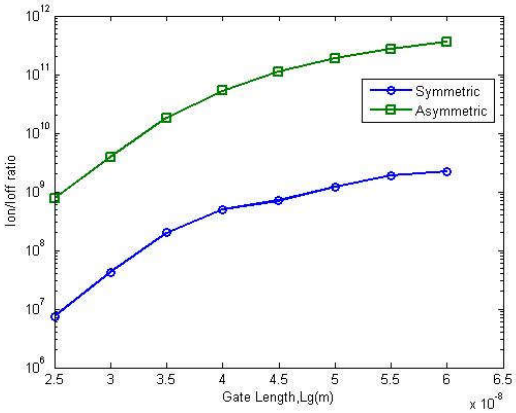

Fig. 4(c). Comparison of I_{on}/I_{off} ratio between symmetric and asymmetric DGS-JLFET (V_{ds}=0.1 V)

Fig. 4(c) compares the I_{on}/I_{off} ratio between symmetric and asymmetric DGS-JLFET. It can be seen that asymmetric DGS-JLFET shows 10^2 times higher I_{on}/I_{off} ratio than symmetric DGS-JLFET.

C. Subthreshold Swing (SS)

It is expected that low gate voltage should be applied in order to have large change in the output current. So, subthreshold swing should be smaller. Less leakage current and less energy is always expected which is obtained by small subthreshold swing. It means improved I_{on}/I_{off} ratio. Subthreshold swing is calculated from [11] as,

$$SS = \frac{\partial V_{gs}}{\partial \log_{10}(I_{ds})} = \frac{V_{th} - 0}{\log_{10}(I_{on} - I_{off})} \quad (8)$$

When dielectric constant k is increased, I_{off} decreases and hence SS decreases too. Fig. 5(a) shows that as the dielectric constant of high-k oxide combination is increased, SS decreases slightly. Now if oxide thickness is increased, I_{off} increases and so similarly SS increases too. Fig. 5(b) shows if the oxide thickness is increased from 1nm to 1.5nm, SS increases. So smaller oxide thickness is preferable.

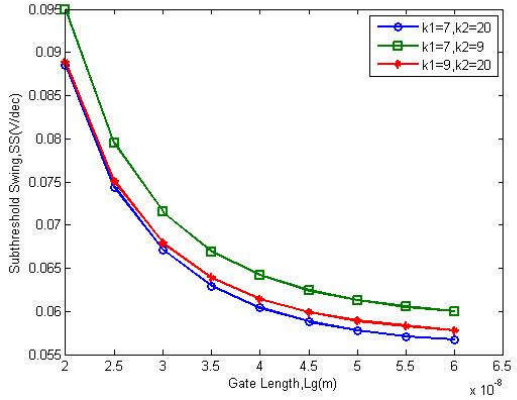

Fig. 5(a).Change in *SS* of asymmetric DGS-JLFET by changing high-k oxide combination (V_{ds}=0.1V)

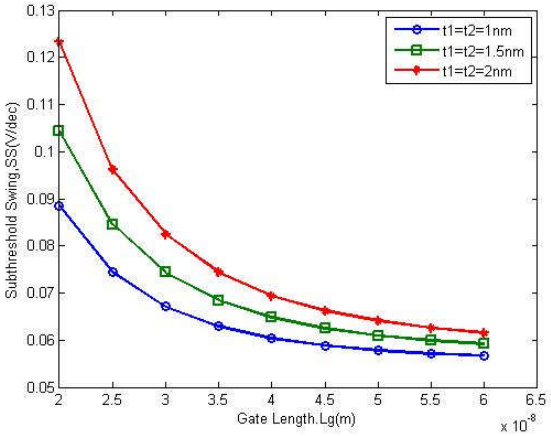

Fig. 5(b).Change in *SS* of asymmetric DGS-JLFET by changing oxide thickness (V_{ds}=0.1V)

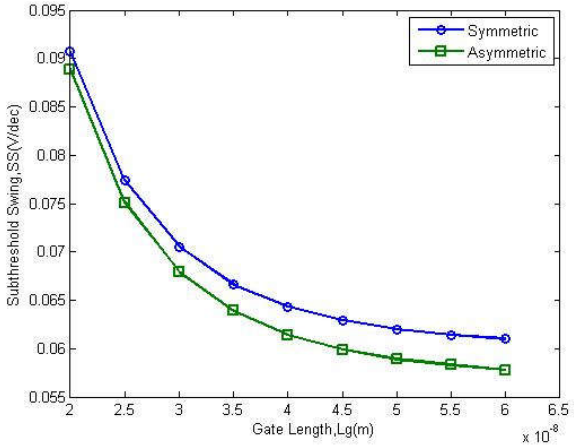

Fig. 5(c). Comparison of *SS* between symmetric and asymmetric DGS-JLFET (V_{ds}=0.1 V)

Fig. 5(c) shows that asymmetric transistor shows less SS.

D. Threshold Voltage Roll-Off (TVRO)

The decrease of threshold voltage with decreased gate length is a well-known short-channel effect called the "threshold voltage roll-off (TVRO)''.

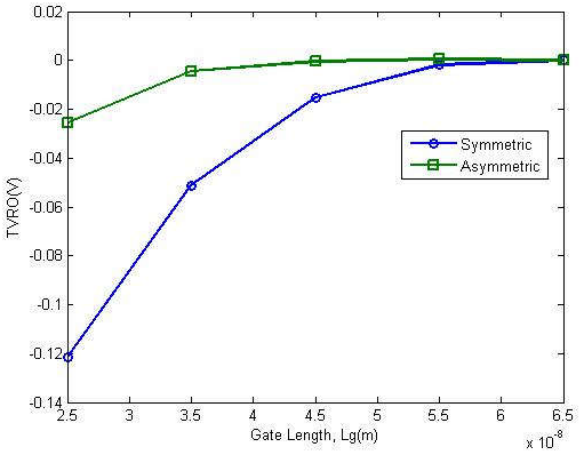

Fig. 6(a). Comparison of TVRO between symmetric and asymmetric DGS-JLFET (V_{ds}=1V)

Fig. 6(a) shows that symmetric DGS-JLFET shows larger TVRO than asymmetric DGS-JLFET especially for shorter gate length. Fig. 6(b) shows that TVRO is less for lower oxide thickness for short channel. But it gives less TVRO at 1nm channel length.

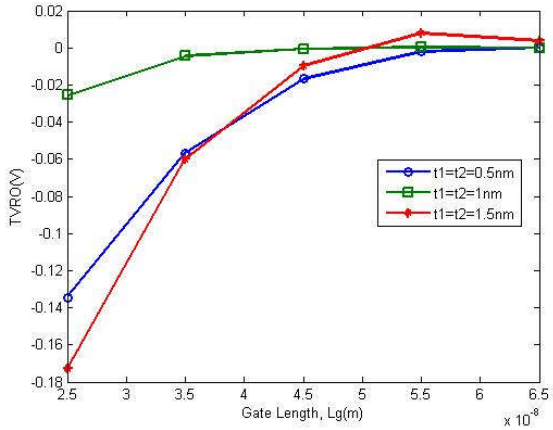

Fig. 6(b). Change in TVRO of asymmetric DGS-JLFET by changing oxide thickness (V_{ds}=1 V)

IV. Conclusions

In this work, we have provided a model that can be used for any combination of high-*k* stack-oxide. Equations derived from the model have been used to observe short channel effects of double gate stack-oxide JLFET by taking different combination of high-*k* oxide and oxide thickness of stack gate. Simulation results show that asymmetric devices have higher threshold voltage, lower off state current, higher

I_{on}/I_{off} ratio, lower SS and lower TVRO compared to symmetric devices. Therefore, asymmetric DGS JLFETs show improved performance values compared to symmetric DGS-JLFET. Also performance comparison of subthreshold behavior between asymmetric devices for different combinations of high-*k* stack oxide has been made. Devices with stack oxide using higher *k* values have shown better performance. Asymmetric DGS JLFETs could be potential devices for future applications.

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