High-phase Resolution Architecture for Phased Array Transmitters

F. Cannone, G. Avitabile, G. Coviello

***Abstract*—** The paper describes a frequency independent phase shifting technique suitable for applications wherein a high-phase resolution at RF frequencies is required. For instance the propose approach is useful both for advanced measurements systems and for RADAR, satellite and wireless telecommunications systems. The proposed phased array transmitter is based on an innovative technique using the cascade of two blocks: an advanced digital block named Phase Control Block and an up-converter block containing integer-PLLs. The first digital block assures a high phase resolution comparable with the precision achievable by using a Direct Digital Synthesizer. The second block allows the up conversion at microwaves frequencies without a significant decrease of the phase-shift precisions. In fact, thanks to the described technique, the phase resolution is limited only by the rms phase error introduced by the integer-PLLs. The theory governing the design of the phase shifter is thoroughly discussed and three prototypes operating in different bands reporting an rms phase error lower than 0.4 degrees are reported. The measurements are compared with theoretical results showing a perfect agreement.

***Keywords*—** Phase shifter, Microwave circuits, Antennae array, Phase Locked Loop (PLL).

I. Introduction

ELECTRONIC phase shifters are employed in several ways in advanced measurements systems, RADAR, satellite and wireless communication applications [1]-[4], mostly for antennae array design. The main advantages of commonly used structures are high directivity, interference rejection, fast scanning rate and signal to noise ratio improvement. The higher is the number of elements combined in the array the more evident are the advantages of phased arrays. Moreover, the modern radar and communications transceivers have to provide multi-mode and multi-band operations. In phased array systems this means for instance, to have the possibility to track multiple targets in electronic countermeasure and radar systems or multi-point communications. All these requirements place an increasing interest in phase shifters.

The recent literature presents various techniques for phase shifter structure [5]. The use of transmission lines or metamaterial transmission lines with distributed loads gives rise to distributed-type phase shifters (DTPSs) which have as an alternative the approach based on a vector sum of two or more orthogonal-phased signals and the phase shifters based on an all-pass network [5]-[11].

A second classification can be made depending on the position of the phase shifters in the Tx/Rx module: LO, IF, RF or base band phase-shifting architecture are possible [4]. Several solutions have been proposed, each one suitable for a specific application. Recently both for RADAR, satellite and wireless communication applications, the demand of programmable and reconfigurable Tx/Rx modules has been increasingly pushed by the advances in the field of software radio architectures. This calls for novel topologies and solutions.

In [12] it is described a programmable phase shifter based on a Direct Digital Synthesizer (DDS). In this approach the RF digital phase shifter in the transmitter path has been substituted by the phase shift function of a DDS followed by a mixer for the up conversion. The LO-path phase shifting technique is an alternative approach that has produced interesting phased array systems [13[-[15]. These reported LO phased array transmitters are based on the heterodyne architecture.

In the case of modulation schemes based on the PSK or FSK, an alternative architecture is that based on the PLLs used in the transmitter path. The Sigma-Delta fractional-PLLs are the classical implementation that allows to achieve good performances and high data rates limited mostly by the band of the PLL. Moreover, different solutions to overcome this band limit are possible [16]-[18].

In [19]-[22] are presented some techniques to use a PLL in the phase shifter architecture.

The architecture described in this paper, is based on the phased array transmitter described in [23]-[25] and investigates the possibility to use the LO phase shifting technique along with the PLL based transmitter. This novel topology has been introduced as an alternative to very high phase resolution architectures, such as those based on the DDS, with the additional feature of frequency scalability.

The main achievement is a very high phase resolution available for different ranges of frequencies. Indeed the rms phase error is limited only by the rms phase error of the PLLs. It is also important to highlight two other features. First, the number of bit is easily scalable since a higher phase resolution is achieved simply by modifying the digital part of the

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architecture. Second, the phase steps are controlled by the digital block and therefore the architecture is capable to be used for every digital beam-forming and calibration technique. In general, a lot of error sources exist in the front end which motivate the adoption of a calibration technique. For instance, [26] demonstrates that the calibration is a good solution to reduce the phase deviation due to the changes in the power supply and the deviation across different prototypes due to process variations.

The paper reports the measurements of three prototypes operating in three different bands showing a similar rms phase and errors lower than 0.4 degrees. The paper is organized as follows: section II briefly introduces and discusses qualitatively the proposed transmitter; section III describes in details its operations. Finally, the three prototypes are described and experimentally validated in section IV.

II. PHASE SHIFTER ARCHITECTURE

A. Current architecture overview

An ideal phased array transmitter consists of several signal paths each one connected to different antennas. The beam forming is achieved by varying the relative time delay between the signals feeding each single element of the antenna. The beam forming does not depend from the frequency and the bandwidth of the signal when governed by true time delays. In practical phased arrays, it is difficult to design tunable, broad-band delay blocks but it is possible to approximate the uniform delay with a constant phase shift over a moderate signal bandwidth. This approximation, even maintaining the wanted coherence for the carriers, introduces a distortion of the baseband modulation signals that depends on the signal bandwidth. The higher is the ratio between the bandwidth and the carrier, the higher is the baseband time incoherence, which means a degradation of the error vector magnitude (EVM), which is also a function of the incidence angle at the receiver. In narrow band applications, the constant phase shift approximation is a viable solution. Moreover, unlike the wideband case, the phase shift technique in the case of narrow-band signals can be implemented at RF, LO, IF, baseband level or, even, in digital domain. Each of the previous possibilities corresponds to a different phase shifter architecture. In Fig.1 these classical architecture of phased array transmitter are reported.

As stated before, in narrow band applications the constant phase shift approximation is a viable solution at RF, LO, IF, baseband or digital domain level [13]. The RF phase shifting technique is considered the most cost-effective solutions mostly for systems requiring a big number of elements [4].

A low-loss RF phase shifter is a challenging building block at high frequencies, and it is difficult in practical implementations to achieve low losses joint to uniform performances for the different phase shifts. In spite of these difficulties, good results in terms of phase variations have been reported for medium phase resolution systems.

For instance, in [27] a phase variation less than 8.8 degrees for all the 4-bit phase states at 35-50 GHz is shown.

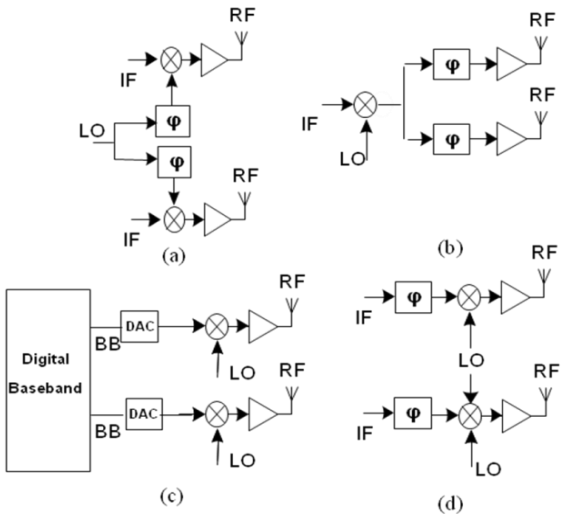

Fig. 1 Phase shifting architectures: (a) LO path phase shifting ; (b) RF phase shifting; (c) base band phase shifting; (d) IF phase shifting.

The LO-path phase shifting technique requires more components than an all-RF architecture but introduces several advantages relaxing, for instance, the impact of the insertion losses variations on the system's performances. Phased array systems adopting this approach and achieving interesting results are described in [13]-[15].

Digital array architectures are very flexible but in general lead to expensive and not power-efficient solutions for a given phase resolution and band of frequencies. The higher is the frequency the less the DDS is feasible in terms of power consumption.

The proposed architecture, is different in that it gives the possibility to use the LO phase shifting idea along with the PLL based architecture in order to obtain higher phase resolution.

B. The proposed architecture basics

The core of the proposed transmitter is a PLL configuration that is able to perform simultaneously the LO phase shifting and the up conversion. The LO phase shifting is achieved by controlling the signal used as references for the PLLs. Two basic blocks for the proposed approach are depicted in Fig. 2.

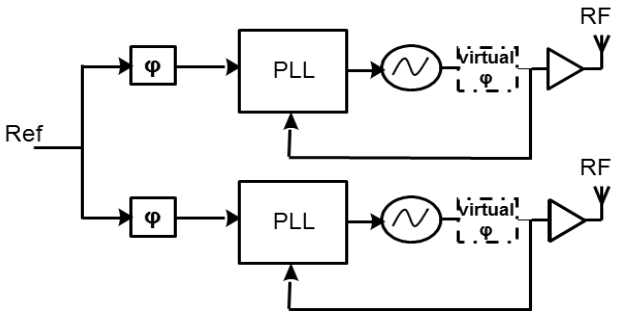

Fig. 2 Proposed phase shifting architecture.

The phase shifting is introduced on the signal used as references for the PLLs and, thanks to the techniques explained in the next sections, it implements a virtual LO phase shifting. Since the phase shifting is implemented at high frequencies but is controlled at low frequencies, it is easier to achieve the desired high phase resolution for a given band of frequencies if compared with traditional approaches.

Among the reported phased array transmitters based on a PLL, in [22] an interesting architecture that uses a variable-phase ring oscillator (VPRO) was presented. This solution reduces the area and power requirements by eliminating a number of key building blocks. The architecture does not aim to a high phase resolution and a 3-bit operation is reported. Even though the principles underneath such transmitter are quite different, also the proposed approach allows to eliminate a number of key building blocks. Nevertheless, the proposed solution reaches its outstanding high phase shift resolution at the expense of more components than the architecture in [22], therefore it is more suitable in those applications where the key issue is the phase resolution while the complexity and power consumption are less crucial.

The proposed approach seems to be to the authors one of the best reported solution for improving the phase shift resolution; looking at the complexity, integration and power consumption, this architecture is comparable to those adopting the LO-path phase shifting. This means that it is not the most cost-effective solution if compared to the all-RF architectures.

In particular, for what concerns the integration, it is possible to make some considerations from a system level point of view. Assuming to use a silicon RFIC process, the proposed architecture is suitable for integrating on the same chip a smaller number of modules than an all-RF phase shifter architecture like the architecture based on IF, LO or Base Band. Since the all-RF approach allows to simplify the control routing in a large array is therefore the more suitable solution from a scalability point of view.

Similar considerations can be made for the power consumption. The main drawbacks in this case derives from the presence of a VCO and a divider in each branch, which are the more power consuming components. The proposed architecture can provide the same phase resolution of a DDS phase shifter with the important advantage of moving in the RF domain such capability. In those applications where a very high phase resolution is necessary, for instance a single phase shifter for instrumentation at high frequencies, the proposed architecture can be considered a low-power solution when compared to the high-frequency DDS mandatory needed due to the fact that the up converter mixer otherwise would deteriorate the DDS phase shift resolution.

The proposed approach if compared with the classical LO-path phase shifting based on the heterodyne architecture evidences analogies and differences. The losses and the amplitude mismatches introduced by phase shifters controlling the reference signals do not affect the phased array transmitter performances, similarly to the case of phased array in [13]-[15], since the digital phase and frequency detector (PFD) works independently from the amplitude level of its inputs, following theirs rising (falling) edges. In heterodyne architectures, the LO signals are in RF domain. This means that the phase shifters used to achieve the LO-path phase shifting, even if, have relaxed constraints, are designed to operates at RF. Although good design approaches are possible to achieve high-resolution RF phase shifters [15], it still remains a challenging task. The proposed topology does not rely on these blocks. Indeed, exploiting the lock mechanism of the PLLs, the LO phase shifting is achieved directly managing the reference signals. Moreover, since the up conversion is performed contextually at the phase shifting of the LO, any mismatch introduced by the up converter is cancelled by the closed loop operation. Finally, one of the main challenge which limits the phase resolution achievable by a classical LO-path phase shifter is the design of the LO distribution network [4],[26]. The proposed approach strongly relaxes this problem because the LOs are present in each module and the signals that need to be routed are in the baseband or IF domain.

C. Open questions: the bandwidth and the receiver structure

The main open questions among the others that need attention are the channel bandwidth and a proposal on the receiver side. This paragraph reports some qualitative considerations.

A limit to the channel bandwidth is imposed by the cut off frequency of the PLL loop filter. This problem could be overcome by using techniques like the on-channel and two-point modulation. As an alternative, in applications which require wider bandwidths, it is possible to use the proposed phase shifter not as the complete phased array transmitter, but as the sub-block which implements the local LO-path phase shifting [28] at the expense of adding a mixer in each branch. Indeed, in this assumption the channel bandwidth is still not linked to the one of the PLL.

This latter solution is at the same time the more direct way to use the proposed transmitter into the receiver path. In this case the analysis of the expected performances of the receiver module is similar to that described in the papers reporting those architectures.

III. PHASE SHIFTER OPERATIONS

The simplified block diagram of the proposed architecture, is depicted in Fig.3. This advanced Phase Control Block(PCB)-PLLs phase shifter has two main blocks: the PCB and the PLLs block. The PCB is a digital block which provides the phase-shifted squared waves with a phase-shift precision equal to $360°/2^k$ being k the number of bits of the PCB. The number of squared waves, P, corresponds to the number of paths or channels to the antennas. The inputs to the PCB are the PLL reference clock and the P input phase words. These latter can be provided to the PCB by using a DSP or a microcontroller; these words set for each path to the antennas the desired phase shifts. The second block contains P integer-PLLs which up-convert to the microwaves frequencies the

phase-shifted squared waves provided by the PCB. The process of up conversion occurs without a significant decrease of the phase-shift precisions.

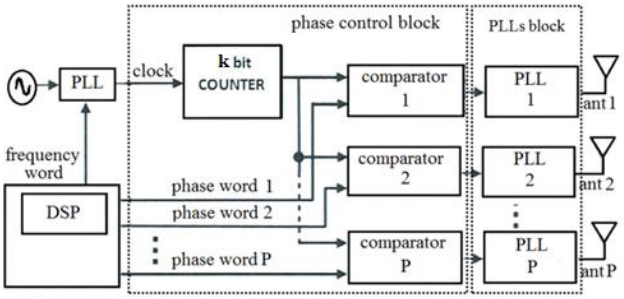

Fig. 3 Phase Control Block-PLLs Phase Shifter Architecture.

The proposed solution has the evident advantage that allows to reach the wanted phase resolution (for instance, the resolution wanted for implementing a calibration technique) without impacting the complexity of the overall architecture. The basic idea is to use the Phase Control Block to reach the high phase resolution and the PLLs to up convert the signals without compromising the signal integrity and phase resolution. It is possible in the digital world to design a low power and high performances PCB with a big number of bits for the wanted very high phase resolution (to a feasible 14-bit PCB correspond a phase steps equal to about 0.02°). Nevertheless, it is not possible to use directly such a digital block with an up converter. In fact, the multiplication using PLLs compromises the signal integrity and the phase resolution, while the up-conversion using a mixer may in addition require difficult or impossible output filtering.

A. PCB-PLLs phase shifting techniques

A first way to deal with the degradation of phase resolution using a PLL as up-converter, is to use an offset-PLL, i.e. a PLL with a mixer in the feedback path instead of the divider. As demonstrate in [23], the mixer in the feedback path of the offset-PLLs shifts the RF VCO output to an IF frequency, so that no phase degradation occurs. This approach provides the capability to take advantage of the digital block at microwave frequencies. A key point of this topology is the design of the local oscillator that drives the mixers. Indeed, when this architecture is used to generate high frequency signals, the LO is a microwave oscillator. Taking into account that the transfer function between the LO input of the mixer and the PLL output has a low-pass nature, it is necessary to design a low phase noise VCO in order to not increase the rms phase error of the PLL.

A second way has been presented in [24],[25]. Under rigorous condition, it is possible to use a divider into the feedback path of the PLL, as alternative or joint to the mixer, without deteriorating the phase resolution. In fact, for using a M divider in the feedback loop is sufficient to link the choice of M to the reference frequency, to the wanted output frequency and the number of bit, k, of the accumulator.

In Fig. 4 the operating condition is exemplified. Let $REF^0(t)$ be the reference signal for the other shifted signals provided by the phase control block, $REF^{\Delta\varphi RES}(t)$ the reference signal for the PLL which has a minimum phase shift equal to $\Delta\varphi_{RES\text{-}IN}$ with respect to $REF^0(t)$ and VCO(t) the squared output of this PLL. When the PLL, which has as input $REF^{\Delta\varphi RES}(t)$, is locked, then its squared output VCO(t), has the rising edges aligned with the rising edge of its input, while the squared output of the PLL used as reference has the rising edges aligned with the rising edges of $REF^0(t)$.

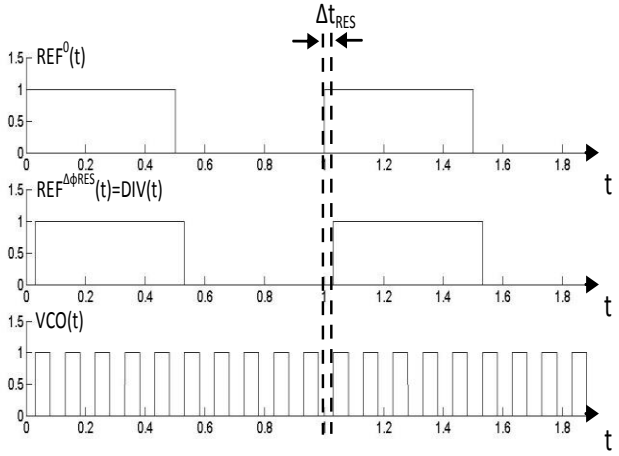

Fig. 4 Exemplification of the operating condition.

In such an operating condition, the two inputs and the two outputs of the two considered PLLs are delayed of the same amount of time, equal to Δt_{RES}. In particular, being $\Delta\varphi_{RES\text{-}IN}$ the minimum achievable phase shift, then Δt_{RES} represents the minimum time delay between the signals that drive the PLLs. The relation between $\Delta\varphi_{RES\text{-}IN}$ and Δt_{RES} is expressed in (1)

$$\Delta t_{RES} \rightarrow \Delta\varphi_{RES-IN} = \frac{\Delta t_{RES}}{T_{IN}} \cdot 2\pi \quad (1)$$

where T_{IN} is the reference period at the input of the PLL. At the output of the PLL occurs the same time delay, Δt_{RES}, to which corresponds a phase shift, $\Delta\varphi_{RES\text{-}OUT}$, equal to $M \cdot \Delta\varphi_{RES\_IN}$

$$\Delta t_{RES} \rightarrow \Delta\varphi_{RES-OUT} = \frac{\Delta t_{RES}}{T_{OUT}} \cdot 2\pi = M \cdot \Delta\varphi_{RES-IN} \quad (2)$$

where, $T_{OUT} = T_{IN} / M$, is the period at the output of the PLL. Therefore, when a division by a factor M is inserted in the loop, the phase is divided by M considerably decreasing the phase resolution (when a M divider is used, the minimum output phase step becomes $(360/2^k)$ x M degrees). Actually, considering that $\Delta\varphi=\Delta\varphi+m\cdot 2\pi$, with m integer and that the relation between ΔtRES and k is given by TIN/ΔtRES = 2k, it is possible to choose M in order to have at the output the same resolution achievable at the input

$$\Delta\varphi_{RES-OUT} = \Delta\varphi_{RES-IN} + m \cdot 2\pi \quad (3).$$

The value of M that allows to fulfill (3) is

$$M = m \cdot 2^k + 1 \quad (4).$$

If (4) is respected, it is therefore possible to maintain at the output of the PLLs the same phase resolution imposed at the input by the digital block. Even though the M divider into the feedback path contributes to the overall phase noise of the PLL, the possibility to use this block with or without a mixer extends the applicability of the topology in different ranges of frequencies relaxing the design of the single blocks.

A further important step ahead in using the M divider instead of a mixer in the PLL is possible. The relation stated in (4) allows the use of an M divider but still imposes an important constraint on the choice of M and consequently, places some limitations in dimensioning the reference frequency given a wanted range of output frequencies. Actually, it is possible to overcome this problem. The basic idea is to use an odd value of M. Making this choice, it is possible to obtain at the output the same number of input phase shifts, that is the same phase resolution. The assumption generalizes the expression of M used in (2) as follows

$$M = m \cdot 2^k + n \quad (5)$$

with m and n integer numbers, with such a value of M, (2) can be rewritten as follows

$$\Delta\varphi_{RES-OUT} = (m \cdot 2^k + n) \cdot \Delta\varphi_{RES-IN} = n \cdot \Delta\varphi_{RES-IN} \quad (6)$$

being $\Delta\varphi_{RES\text{-}IN}$ equal to $2\pi/2^k$, with

$$n = M \bmod 2^k \quad (7).$$

The relation expressed in (6) states that the phase resolution at the output is n times the phase resolution at the input. Apparently (6) defines a coarse output resolution but this is not true. In fact, $\Delta\varphi_{RES\text{-}OUT}$ indicates only the output shift obtained relatively to the minimum input phase shift. Indeed, in this way the achievable 2^k phase shifts are not still organized so that to the i-th input phase shift , $i*\Delta\varphi_{RES\text{-}IN}$, corresponds the i-th output phase shift, $i*\Delta\varphi_{RES\text{-}OUT}$, but if M is odd, then the output phase shifts are still equal to 2^k solely, they are ordered in a different way. Assuming, L, the shift position, with $0< L < 2^k - 1$, then results

$$\Delta\varphi_{OUT} = n \cdot \Delta\varphi_{IN} = (n \cdot L_{IN} \cdot \Delta\varphi_{RES-IN}) \bmod 2\pi \quad (8)$$

where L_{IN} is the input position. It is possible to use the following relation

$$L_{OUT} = (n \cdot L_{IN}) \bmod 2^k \quad (9),$$

in order to know the output position L_{OUT} related to the input phase shift position.

The number of the output position, N_{OUT} , is the ratio between 2^k and the Maximum Common Divisor (MCD) between M and 2^k, denoted MDC(M,2k) as expressed in (10)

$$L_{OUT} = (n \cdot L_{IN}) \bmod 2^k \quad (10).$$

As a consequence, it is clear that if M is an even number, some input positions are lost. Thus, the output phase resolution is coarser than the input phase resolution. On the contrary, if M is an odd number the phase positions are preserved and the phase resolution is maintained because the MCD between an odd number and a number that is a power of 2 is always 1.

It is possible to visualize what happens when M is an odd number by using the phase wheel. In Fig. 5 on the phase wheel, the phase steps at the output (outside of the wheel) related to the phase steps at the input (inside of the wheel) assuming M equal to 19 and k equal to 4 (n=3) are reported. It is evident that the output phase steps are still 16 but distributed in a different way.

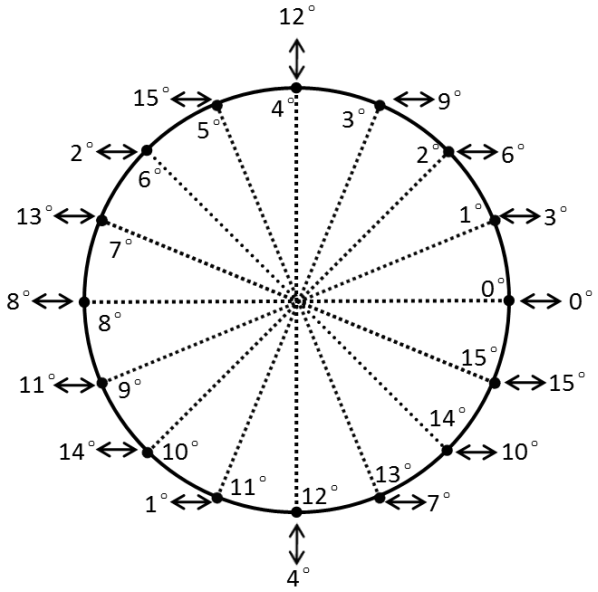

Fig. 5 The input (interior) and relative output (exterior) phase steps.

A first way to control the output phase position is to populate a Look Up Table (LUT) whose dimension must be N_{OUT} using (9) as follows

$$LUT(L_{OUT}) = (n \cdot L_{IN}) \bmod 2^k, \ 0 < L_{IN} < 2^k - 1 \quad (11).$$

Another solution inverts (9) implementing a simple algorithm which uses as input the factor used to know the output phase resolution in relation to the input phase resolution, n, the number of bit, k, the desired output resolution related to the input resolution, n'. The relation gives the multiplicative number, n'', used to determine which input position has to be imposed to obtain the desired output phase shift position. Such

relation is:

$$n' = (n'' \cdot n) \bmod 2^k,\ 0 < n'' < 2^k - 1 \quad (12)$$

and the input position, L_{IN}, to be imposed is given by the following relation

$$L_{IN} = (n' \cdot L_{OUT}) \bmod 2^k \quad 0 < L_{OUT} < 2^k - 1 \quad (13)$$

A practical example is discussed in the section 4.

B. *The novel Phase Control Block*

The proposed Phase Control Block is sketched in Fig. 3. This block has P outputs (the phase-shifted squared waves) and two inputs (the clock and the phase control words). It has two main sub-blocks: the counter and the bank of P comparators. The novel proposed PCB uses a counter as first sub-block instead of an accumulator unlike those reported in [24] and [25]. The use of an accumulator allows to change the frequency of the phase-shifted squared waves, thanks to an extra input called input word. However when the input word is greater than the unity the achievable phase-shift precision decreases and therefore to maximize the precision the input word should be set equal to one.

Actually since the output frequency is set by the PLLs, then the PCB can control the phase shifting independently from the output frequency. It is possible to maximize the phase-shift precision relaxing simultaneously the PCB in terms of complexity, and power consumption, by renouncing to the change of the frequency of the phase-shifted squared waves. The simple idea is to use the counter instead of the accumulator. Moreover the clock to the counter is provided by a PLL, then it is possible to recover the frequency variation of the phase-shifted squared waves by exploiting this PLL.

IV. Prototypes and Measurements

In order to validate the previous discussed advantages, a set of three prototypes has been built and measured. Each prototype is composed by two integer PLLs, a FPGA and a PC which handles the automatic phase and frequency switching of the prototype and the automatic measurements on the oscilloscope (Fig.6). The phase control block embedding the k-bit accumulator has been implemented on the FPGA, that provides the phase shifted signals to the inputs of the PLLs and the input phase words to the comparators, while the PLLs synthesize the desired outputs.

The external reference provided by a frequency generator, furnishes the clock for the phase control block and an oscilloscope has been used to measure the relative phase shifts between the PLLs. The PC governs the entire measurement setup. It is connected to the FPGA board and controls when the phase shift has to be changed. The PC is connected also to the PLLs and to the frequency generator in order to reprogram the PLLs when the reference frequency is changed, for the measurement on the entire VCOs bands. Finally, the PC controls the oscilloscope for the automatic measurement of the phase shifts. In detail the characteristics of the three prototypes are:

1. 1st prototype: center frequency= 290MHz, bit number=7, minimum phase shift = $360°/2^7$ =2.8125°;
2. 2nd prototype: center frequency=2.45GHz, bit number = 7, minimum phase shift = 2.8125°;
3. 3rd prototype: center frequency=3.825GHz, bit number = 6, minimum phase shift = 5.625°.

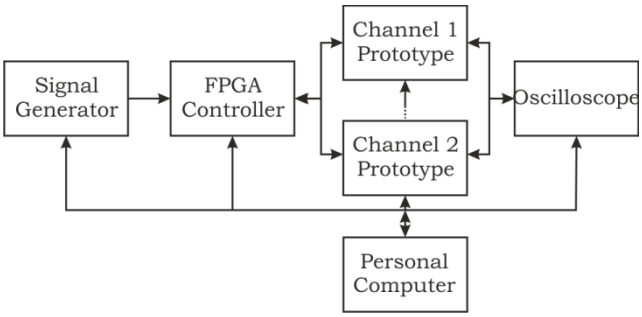

Fig. 6 Experimental setup used for prototypes measurements.

The overall bands of synthesis of the prototypes have been covered only by varying the external reference and reprogramming the PLLs.

The description of the three prototypes is similar, therefore, excluding the measurements, for reasons of space, only the case of the third prototype is reported in details. The value of M chosen is 2001, respecting (7) and (10); n is equal to 17 and N_{OUT} is equal to 64. Being n different from the unity, it is necessary to ordinate the 64 output phase positions, then the algorithm previously described has been adopted using in (12) n'=1 and consequently n''=49. Thus, for example, to an output phase shift equal to 28.125°, respecting (9), the input position has to be 53. The entire PLL band has been characterized, starting from 3.77GHz to 3.88GHz with a step frequency of 0.733MHz. For each frequency, all the 64 positions have been measured and the results stored on the PC. Furthermore, the measures have been repeated, in different days, for ten times in order to test the repeatability and the reliability of the architecture.

The results are very good with a maximum absolute difference less than 0.4° between different measures. Fig. 7 shows the rms phase error calculated for each measured frequency in the VCO band and to facilitate the comparison also the rms phase error of the two other prototypes are shown. The third prototype exhibits a maximum rms phase error equal to 0.3194°, demonstrating the good phase accuracy over the entire measured band. In fact, thanks to the lock mechanism of the PLL the performances are uniform in the entire band of the VCO not only at its center band.

This feature is clearly shown by the results reported in Fig. 8(a), (b), (c) and (d) where the frequency responses of the phase shifter determined by the 6-bit digital input codes are shown. It's important to note the almost perfect parallelism of the curves, that demonstrates the frequency-independence of

the proposed architecture. The maximum peak-to-peak insertion phase calculated is about 0.0979°.

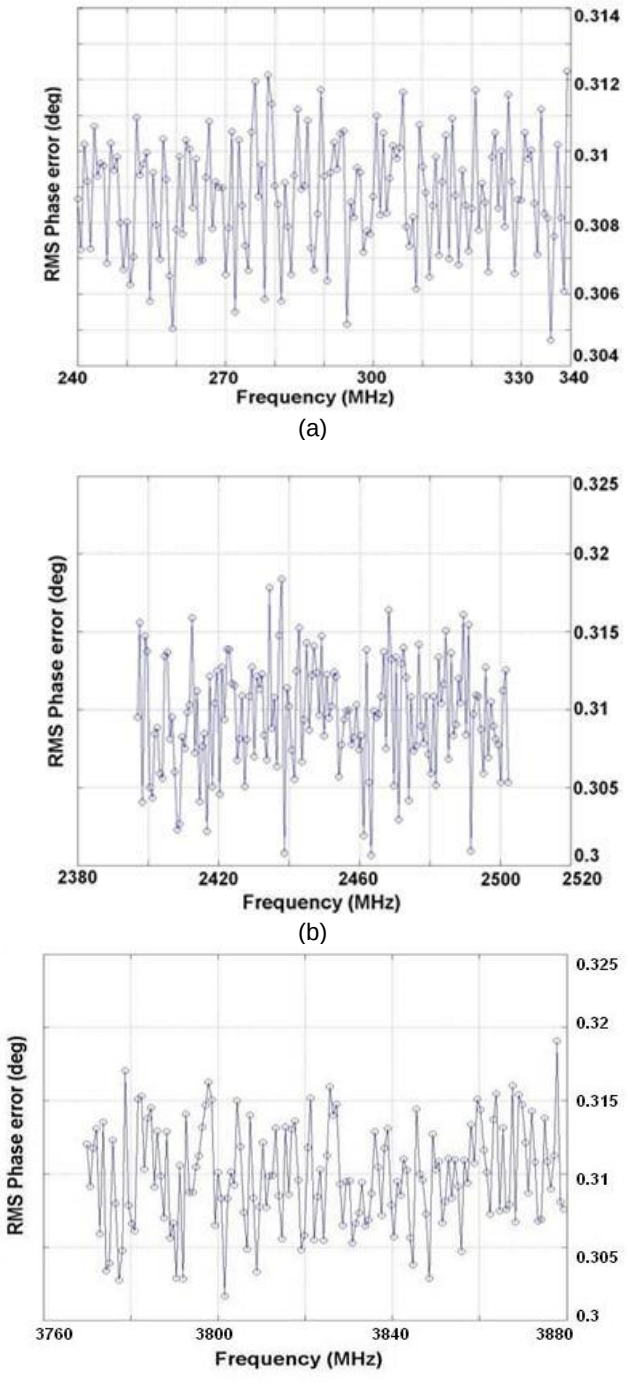

Fig. 7 RMS phase error for (a) 7-bit 290MHz Phase Shifter; (b) 7-bit 2.45GHz Phase Shifter; (c) 6-bit 3.8 GHz Phase Shifter.

In order to underline the importance of the high resolution capability in different applications, in Fig. 9 are reported two cases of synthesized beam patterns (with an assumption of standard linear array with isotropic radiators and λ/2 spacing between 16 elements). The radiation pattern related to the prototype has been evaluated using the measured 64 phase shifts at 3.8 GHz in Simulink®.

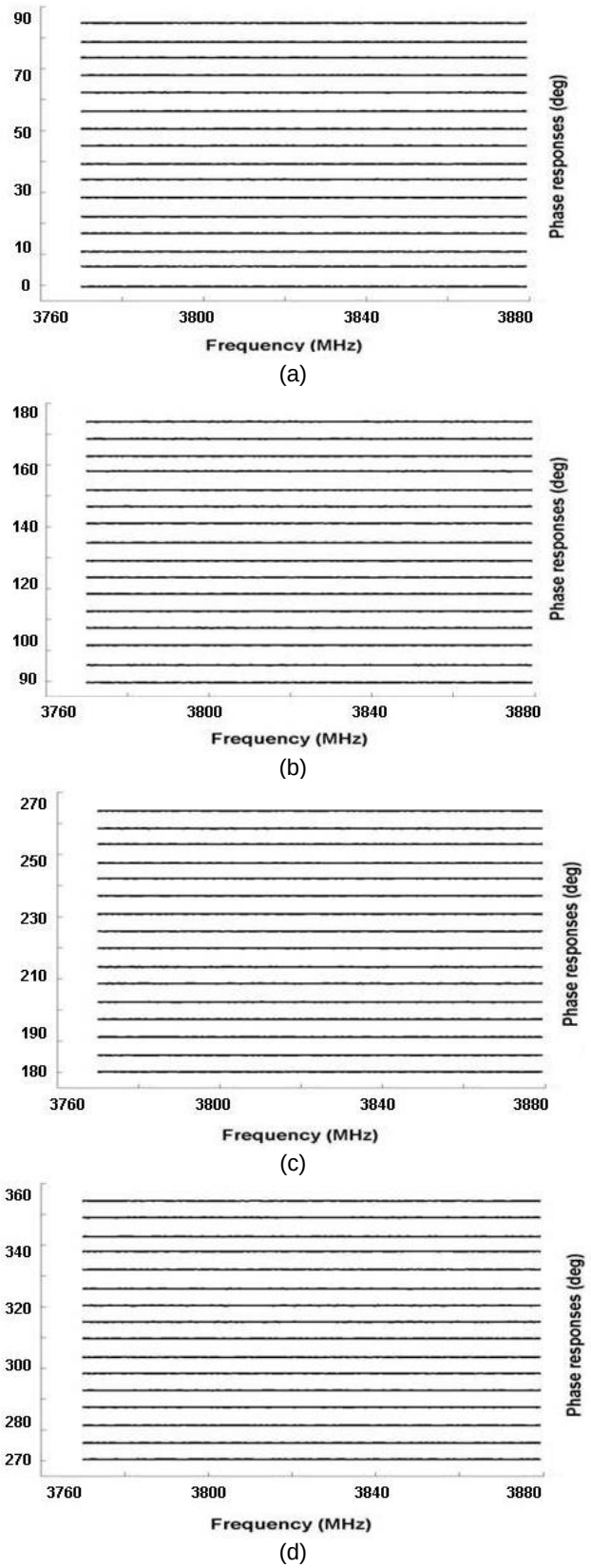

Fig. 8 Measured insertion phase of the 6-bit PS: (a) from 0° to 84.375°; (b) from 90° to 174.375°; (c) from 180° to 264.375°;(d) from 270° to 354.375°.

The ideal radiation pattern has been achieved considering an

ideal phase shifters. In both cases an assumption of the same power gain for all of the 16 elements has been made. It is possible to note the correct operation of the prototype. Moreover, it is evident that the reduction of the phase quantization error allows a reduction of the sidelobes, approaching the ideal case. This makes the proposed phased array transmitter suitable for instance to implement every technique of beamforming.

The rms phase errors of the other two prototypes have been also reported in Fig. 7. The achievable phase resolution basically depends on the rms phase error of the used PLL itself making the proposed architecture easily scalable in frequency. It is possible to note that the results are quite similar, showing better performances around 290 MHz. The measurements uncertainty has to be considered since the oscilloscope sampling rate has an important rule on this type of measurements in time domain. The lower is the output frequency of the PLLs, the better are the measurements and as a consequence the phase shift error evaluation. At the moment only for reason related on the measurement capabilities it is not possible to show prototypes working at higher frequencies.

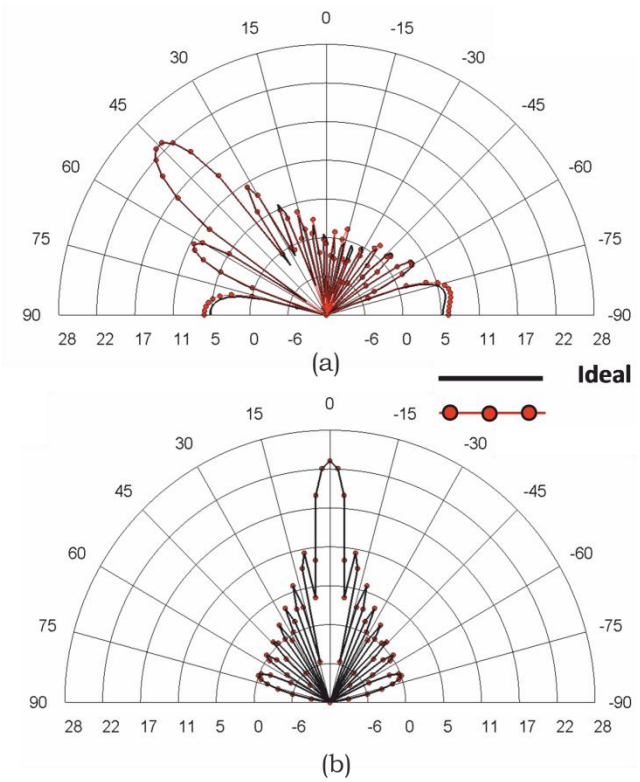

Fig. 9 Array beam scanning characteristics: (a) 45° scan angle, (b) broadside scan at 3.8 GHz.

V. Conclusion

An innovative phase shifter for high-resolution, continuous programmable phase shifts with the introduction of new concepts on using the M divider in the feedback loop of the PLL instead of the offset configuration has been discussed and experimentally validated. The prototypes reported have confirmed the outstanding results in terms of phase resolution and the scalability in frequency of the phase shifter. Due to the fact that they use as phase control block the FPGA it is not easy to quantify the equivalent power consumption imputable to the phase control block and therefore the prototypes cannot be used to estimate the power consumption.

The great flexibility of the proposed architecture grants that the frequency scalability is simply achieved by using a suitable PLL and the phase resolution is demanded to a very simple digital circuit.

The proposed topology is suitable for the implementation of any kind of digital beam forming and calibration technique in those applications which require continuous phase shifting, high resolution, and flexible and reprogrammable features.

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