# Reconfigurable Cost Effective Design of Digital up Converter for Mobile Communication

Rajesh Mehra, S S Pattnaik

***Abstract*—** In this paper cost effective reconfigurable WCDMA DUC design has been presented for mobile communication base stations. The WCDMA DUC has been designed and implemented by combining the multiplier less and multiplier based techniques to achieve an optimized hybridized solution for mobile applications. The different sections of DUC have been optimized separately and then combined together. The Park McClellan algorithm has been used for optimal filter length to reduce hardware requirements along with computationally efficient polyphase decomposition technique to optimize both speed and area. The embedded multipliers and LUTs of target FPGA are efficiently utilized to enhance the system performance. The proposed DUC has been designed with Matlab, synthesized with Xilinx Synthesis Tool (XST) and implemented on Virtex-II Pro based xc2vp30-7ff896 FPGA device. The developed DUC can operate at a maximum frequency of 147 MHz by efficiently utilizing the resources available on target FPGA to provide cost effective solution for SDR based wireless applications.

***Keywords*—**3G Mobile Communication, Base Stations, Radio Transceivers, Reconfigurable Logic, Software Radio.

## I. Introduction

The digital industry is dynamically growing and the development of digitally based products is rising. Various industries such as audio, video, and cellular industry depend heavily on digital technology. A great part of this deals with digital signal processing. This aspect in engineering has gained increasing interest, especially with much of the world now turning to wireless technology and its applications to keep businesses and industries connected. The world of digital technology is certainly one that will play vital role for many years to come. Digital Signal Processors (DSPs) are specialized devices designed to implement digital signal processing algorithms on stream of digitized signals. DSPs are widely used in wireless systems to perform various filtering, encoding, decoding and transform functions.

The highly competitive nature of the wireless communications market and constantly evolving communication standards have resulted in short design cycles and product lifetimes. This environment has led to the emergence of a new class of configurable DSPs, which can leverage hardware flexibility, programmability, and reusability, to provide highly customizable DSP solutions [1]. DSPs can broadly be divided into two classes: ASIC and Programmable DSP. ASICs implement complex algorithms in hardware and are used in applications that demand high computational performance. Programmable DSPs on the other hand are used to implement low to medium-complexity algorithms in software, and are mainly used in applications that require good performance at low system costs. For this reason, programmable DSPs are widely used in wireless handsets to perform various baseband processing functions such as filtering, equalization, and echo cancellation [2].

As communication standard evolve and time-to-market pressures yield shorter design cycles, programmable DSPs become more appealing than ASICs due to the ease with which their functions can be modified. However when hardware acceleration is the only approach for satisfying the computational demands of an applications, ASICs maintain their advantage. For high end digital signal processing where the highest possible performance is needed at low power consumption, ASICs are still the processors of choice. However, ASICs require very long design and development times and are very expensive to design and manufacture. Moreover, ASICs are inherently rigid and are not very well suited to applications that are constantly evolving. For these reasons, Programmable Logic Device like Field Programmable Gate Arrays (FPGAs) have emerged as an alternative to ASICs in wireless communication systems. FPGAs are mainly used for the flexibility they provide. Like programmable DSPs, FPGAs are programmed and configured in software. This makes it very easy to upgrade or add functionality to an FPGA, even if it is already deployed in the field. Like ASICs, FPGAs achieve high levels of performance by implementing complex algorithms in hardware. FPGAs are particularly well suite for accelerating algorithms that exhibit a high degree of data flow parallelism. The FPGAs suffer from the drawbacks of inefficient resource utilization, high cost and power consumption [3].

The cost factor can be improved by using less expensive FPGAs for system design and by efficient utilization of FPGA resources. The power factor can be improved by using less number of SRAM based programming interconnections. With increasing demand of battery dependent devices, methods for reduction of the power consumption of the memory blocks have received significant interest. Six transistor SRAM cells are preferred for many applications because of its high speed and robustness. In SRAM enriched FPGAs, SRAM consumes more power during write operation which can be taken care during FPGA manufacturing by using various techniques.

## II. Software Defined Radios

Software defined radios are beginning to find also commercial potential. When the software defined radio becomes main stream, the full potential of adaptability may create possibilities for new kind of services. From the users' point of view, seamless operation across networks, without caring about the underlying technology, would be a very desirable feature. The Second Generation (2G) and Third Generation (3G) systems differ mainly in the channel access technique. The 2G or GSM is basically a TDMA oriented system and 3G is strongly based on CDMA. According to an increasing demand for simultaneous global roaming and all-in-one wireless phones, the interest in the development of the so-called multi-standard radio transceivers was fostered. One leading solution is the dynamic reconfiguration of the different modules in the system to suit the specifications of as many standards as possible so, the system should be capable of dynamically reconfiguring itself to the environment as needed [4].In this scenario the availability of reconfigurable platforms both for the base stations and mobile terminals will be of great concern. This will enable the possibility to reconfigure the receiver while the user is moving, leading to ubiquitous access to services.

Software defined radio (SDR) is a rapidly evolving technology that is receiving enormous recognition and generating widespread interest in the telecommunication industry. Software Defined Radio involves a software implementation of user terminal functions to enable the terminal to dynamically adapt to the radio environment in which it is located. SDR also enables wireless operators to introduce new services independent of the wireless standard used. It also enables subscribers to benefit from new or customized services and truly global connectivity. The development of system on-chip (SoC) design has led to integration of analog RF, analog baseband and digital signal processors on the same chip. This has resulted in low power devices with multi-purpose functionality [5].

The second generation of DVB specs, DVB-S2, was developed for satisfying the today's needs for reliable and effective broadband satellite communication services even under 'hostile' conditions. This is achieved by exploiting the new advances in the fields of coding and modulation. Software defined radio proves to be an enabling technology for future multimode and reconfigurable satellite receivers [6]. To make the transition from one standard to another as smoother as possible, the common and effective domain for the implementation of new system architectures is the Software Defined Radio paradigm. SDR platforms rely heavily on reconfigurable logic to realize complex architectures and evolving standards. Although cost is a major motivating factor in pursuing this technology, the flexibility of accommodating multiple standards under a single hardware "umbrella" is of particular importance to emergency responders (ER) who are often forced to function in environments where wireless coverage is limited or altogether non-existent. In such an environment, ER personnel must have access to radios which can operate not only as common wireless communication devices, but also as push-to-talk P25- compatible radios [7].

A successful implementation of SDR depends on the feasibility of implementing various blocks within the communication chain for multiple standards. Wireless is a continuously changing environment, wherein the innovation rate is very high. It requires as much flexibility as possible by exploiting software solutions. In fact, observing the past years, software platforms have proved superior scalability capabilities with respect to completely hardware solutions. However, the rates involved in mobile wireless communications and the bandwidth requirements cannot be faced yet only resorting to software. SDRs use a single hardware front end but can change their frequency of operation, occupied bandwidth, and adherence to various wireless standards by calling various software algorithms. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands [8]. The hardware reconfiguration feature of a software defined radio (SDR) architecture can support multiple modes of a digital beam former (DBF) striving for compactness and efficient processing power, which are important issues for microsatellite synthetic aperture radar (SAR) systems [9].

A variety of communication systems, which carry massive amounts of data between terminals and end users of many kinds, exist today. Necessitated by the global compliant requisition, original equipment manufacturers are expected to provide convergent solutions that accommodate various standards within a single embodiment. Such systems, however, achieve the desired convergence with the least expendable resources: hardware silicon real estate and product turn over time. This necessity represents a major bottleneck in attempting to achieve higher levels of integration in broadband communication systems. The multi-chip solutions often result in higher integration overhead that translates into higher capital expenses. In contrast, reconfigurable architectures provide flexible and integrated system-on-chip solutions that accommodate smooth migration from archaic to innovative designs, allowing recycling of hardware resources across multiple generations of the standards [10]. Moreover, using this topology, the network providers have the ability to configure the digital front-end based on demand and integrate all the transmit/receive functionalities into a unified and custom-built hardware platform.

As opposed to the application-specific integrated circuits or application-specific standard products (ASSP) solutions with fixed support for the carriers per chip-set, users can configure the field-programmable gate array (FPGA) platforms to accommodate arbitrary number of carriers based on demand, reducing the cost per carrier metric. These requirements have created a surge in the development of radio architectures and

reconfigurable platforms that support multiple standards for the digital front-end of wireless BSs. Future wireless devices will need to support multiple air-interfaces and modulation formats. Software defined radio (SDR) technology enables such functionality in wireless devices by using a reconfigurable hardware platform across multiple standards. With FPGA and data converter technology continuously evolving, the SDR concept is increasingly becoming a reality. Digital up-converters (DUCs) and digital down-converters (DDCs) are important components of every modern wireless base station design.

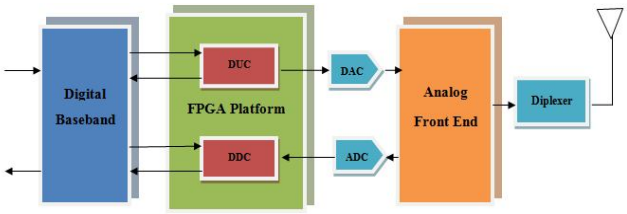


Fig. 1. DDC & DUC in SDR

DUCs are typically used in digital transmitters to filter up-sample and modulate signals from baseband to the carrier frequency. DDCs, on the other hand, reside in the digital receivers to demodulate, filter, and down-sample the signal to baseband so that further processing on the received signal can be done at lower sampling frequencies [11]. The block diagram of software radio architecture has been shown in Fig.1 where the first reconfigurable block for a Software Defined Radio implementation is the Digital IF which consists of Digital down convertor (DDC) to decimate and Digital up convertor (DUC) to interpolate the signal. They are more popular than their analogue counterparts because of small size, low power consumption and accurate performance [12]-[14]. The digital receiver, which performs the digital conversion process close to the antenna and carries out various functions by changing the software on a universal hardware platform, is a typical application of software radio [15]. The digital signal processing application by using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates [16].

## III. WCDMA DUC Specifications

The DUC provides pulse shaping, interpolation, and frequency translation to the single-carrier baseband WCDMA signal from 0 Hz to a set of specified centre frequencies to meet the 3rd Generation Partnership Project (3GPP) TS 25.104 specification, which defines the transmission and reception requirements for the base station radio. The WCDMA DUC design parameters are shown in Table 1. The designed DUC should be optimal in both the system performance and the hardware resource usage. The interpolation filter chain in the DUC needs to pulse-shape and up sample the baseband data by a factor of 61.44/3.84=16.There are several options to perform the specific rate change. First option is design an interpolator with up sample factor of 16 having pulse shaping capability in one shot. This is impractical as it is often difficult to design such a filter to meet the required spectral mask within a reasonable filter length. Even such design will result in extremely high computational complexity.

TABLE I
WCDMA DUC DESIGN PARAMETERS [17]

| | **Parameter** | **Value** |
|---|---|---|
| 1. | Carrier Bandwidth | 5.0 MHz |
| 2. | Number of Carriers | 1 carrier |
| 3. | Baseband Chip Rate | 3.84 MCPS |
| 4. | IF Sample Rate | 61.44 MSPS(16×3.84 MSPS) |
| 5. | Input Signal Quantization | 16-bit I and Q (Complex) |
| 6. | Output Signal Quantization | 16-bit I and Q (Complex) |
| 7. | Mixer Properties | Tunability: Variable<br>Resolution: ~0.25 Hz<br>SFDR: up to 115 dB |

Second option is to decompose the rate conversion into multiple interpolation stages. It is practical to design an RRC channel filter with up sampling factor of 2 and lower order which can meet the system performance requirement. After the channel filter, the signal still needs to be up sampled by 8 with aliasing effects removed in this process. Four possible configurations have been shown in Table 2.

TABLE 2
WCDMA DUC FILTER CONFIGURATIONS [17]

| **Anti-Aliasing Filter Configurations** | **Filter Length & Sample Rate for 1st Filter** | **Filter Length & Sample Rate for 2nd Filter (if any)** | **Filter Length & Sample Rate for 3rd Filter (if any)** |
|---|---|---|---|
| 1 | 91 taps (↑8)<br>61.44 MSPS | - | |
| 2 | 47 taps (↑4)<br>30.72 MSPS | 11 taps (↑2)<br>61.44 MSPS | |
| 3 | 23 taps (↑2)<br>15.38 MSPS | 25 taps (↑4)<br>61.44 MSPS | |
| 4 | 23 taps (↑2)<br>15.38 MSPS | 11 taps (↑2)<br>30.72 MSPS | 11 taps (↑2)<br>61.44 MSPS |

The last configuration will result in cost effective solution because its hardware implementation will require less number of multipliers [17] as compared to others whose block diagram is shown in Fig.2.


Fig. 2. Hardware Efficient DUC

The WCDMA DUC designs [17]-[19] have been developed using readily available FIR compiler blocks of System Generator and Core generator supported by Virtex4, Virtex5 and Spartan DSP FPGA to improve the time to market factor and to enhance the speed. The Virtex-5 based design based can provide maximum operating frequency of 368.64 MHz and Spartan-DSP FPGA based designs can provide maximum operating frequency of 122.88 MHz, respectively. The existing designs suffer from the limitation that their implementation based on Xilinx FIR compiler blocks and DDS compiler blocks. These compiler blocks consist of DSP 48 slices. Due to this fact these WCDMA DUC designs are not economical because their implementation include DSP 48 slice based costly FPGAs. So there was great necessity to implement WCDMA DUC design on low cost multiplier based FPGA to provide optimized solution in terms of area and speed. So in this paper a Digital up Converter (DUC) has been designed and implemented on Virtex II Pro based xc2vp30-7ff896 FPGA device that meets all the WCDMA specifications using a multistage half band decimator along with Park McClellan algorithm.

## IV. DUC Design & Simulation

An optimized Digital up Converter is designed to meet the WCDMA specifications using a multistage half band interpolator along with Park McCelellan algorithm. The in-phase and quadrature phase components were first time division multiplexed into a single stream before being processed by the interpolation filters. The first stage RRC filter has been designed with roll-off factor of $\alpha = 0.22$. When it convolves with the matched RRC filter, the overall raised-cosine response has no inter-chip interference (ICI) because the zero crossings occur at chip intervals. A 45-tap symmetric RRC filter in transposed form with Chebyshev window has been designed to meet all of the requirements. The cascaded adder is used in the transposed structure to eliminate routing bottlenecks of designed RRC filter and to provide area efficiency and enhanced speed. The Chebyshev windowing provides better side lobe suppression than a rectangular window at the expense of some widening of the main lobe. This window results in lower filter order to achieve similar performance as compared to other windows like Hann, Blackman, and Hamming.

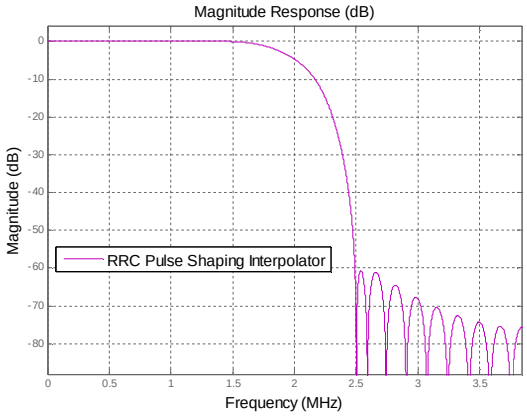


Fig.3. RRC Interpolator Response

The frequency response of the RRC filter with an interpolation factor of two is shown in Fig.3. After the channel filter, a cascade of interpolation filters follows to remove the aliasing effect produced by up sampling. The signal is first up sampled by two using a half band interpolator. Half band filters are a type of FIR filter where its transition region is centred at one quarter of the sampling rate, Fs/4. The end of its pass band and the beginning of the stop band are equally spaced on either side of Fs/4.The output sample rate of the filter is four times the chip rate, i.e. Fs = 3.84*4 =15.36 MSPS. The pass band was set to 3.84*1.22/2 = 2.34 MHz and the pass band ripple is chosen to be 0.002 dB. An equiripple half band filter was obtained with order of 22. The magnitude response of the filter is shown in Fig.4.

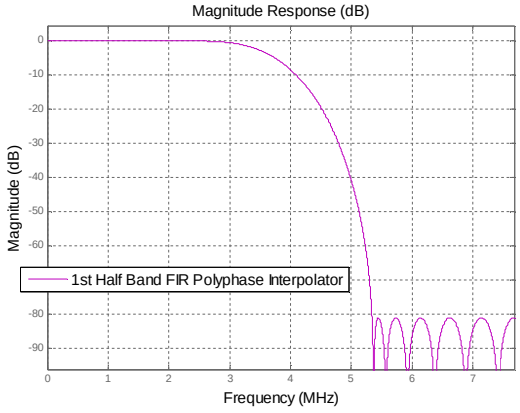


Fig.4. First Half Band Interpolator Response

In the next stage, the signal is again up sampled by a factor of two using a half band interpolator. The output sample rate of the filter is eight times the chip rate, i.e. 3.84*8 = 30.72 MSPS. The pass band is set to 2.34 MHz along with pass band ripple factor of 0.002 dB. A filter with order of 10 has been obtained whose magnitude response is shown in Fig.5.

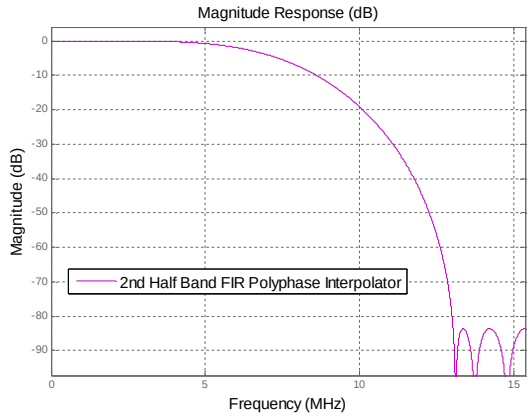


Fig. 5 Second Half Band Interpolator Response

The last half band interpolator provides an output sample rate of 61.44 MSPS. The pass band has been set to 2.34 MHz with pass band ripple factor of 0.001 dB. A filter order of 10 is obtained whose magnitude response is shown in Fig.6. The coefficients precision has been selected as 16 bits each to meet the WCDMA requirements. Finally all filters are cascaded to get final output response of WCDMA digital up converter which is shown in Fig.7.

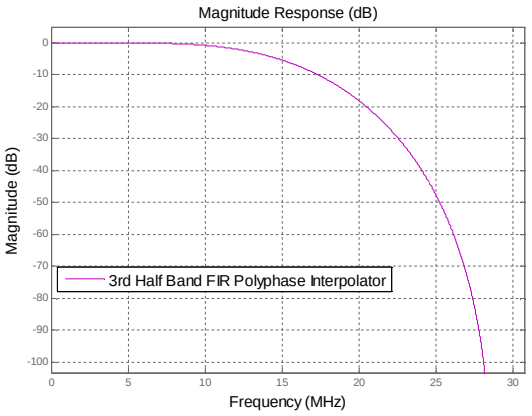


Fig. 6. Third Half Band Interpolator Response

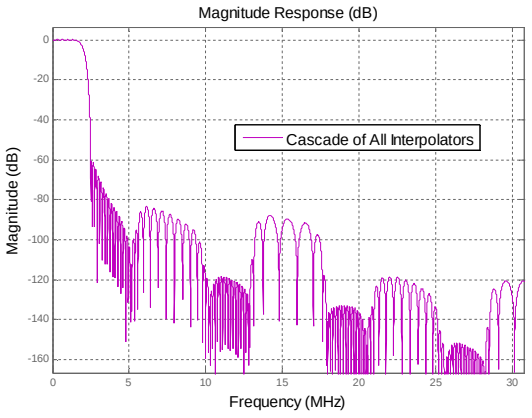


Fig. 7. WCDMA DUC Response

## V. FPGA Implementation

Figures and The WCDMA DUC designs of have been developed using readily available FIR compiler blocks of System Generator and Core generator which are supported by Virtex4, Virtex5 and Spartan DSP FPGA. The System Generator based Implementation of the WCDMA DUC [17] has been shown in Fig.8. The four stage interpolators are implemented using Xilinx Finite Impulse Response (FIR) Compiler block [13]. These FIR compiler blocks are used to provide common interface to generate a parameterizable, area-efficient, and high-performance filter module utilizing Multiply-Accumulate (MAC) architecture. Multiple MACs are used to achieving higher performance filter requirements, such as longer filter coefficients, higher throughput, or support for more channels.

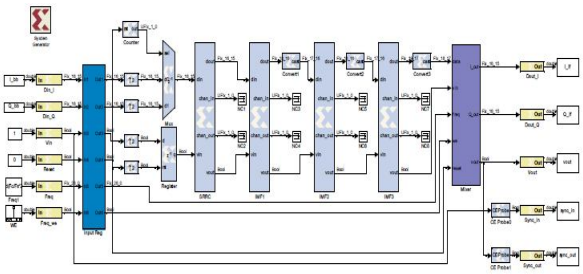

Fig. 8. System Generator Based WCDMA DUC [17]

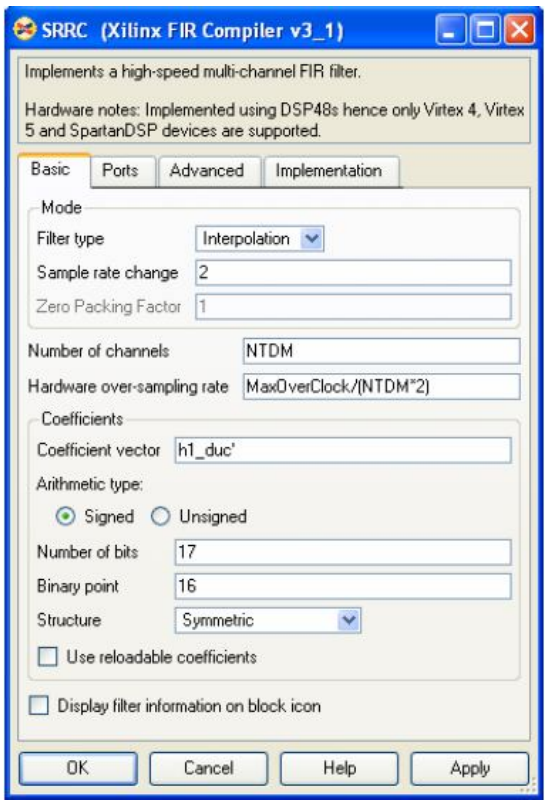


Fig.9. System Generator FIR Compiler Block [17]

The limitation of system generator based design is that its implementation is not possible on low cost FPGA like Virtex 2 Pro. This is due to the use of Xilinx FIR compiler blocks and DDS compiler blocks for its implementation which are based on DSP 48 slices. The system generator based Xilinx FIR Compiler block is shown in Fig.9. In proposed optimized DUC design, RRC filter has been optimized by efficiently implementing the AND and OR logic with LUTs and slices of target FPGA. The RRC filter [20] has been designed and implemented using MAC algorithm by using embedded multipliers. The Virtex-II Pro FPGA slices contain a dedicated two-input multiplexer (MUXCY) and a two-input OR gate (ORCY) to perform AND and OR gates operations. These combine the four-input LUT outputs. These gates have been cascaded in a chain to provide the wide AND functionality across slices [21]. The output from the cascaded AND gates has been combined with the dedicated ORCY to produce the Sum of Products (SOP) as shown Fig.10.

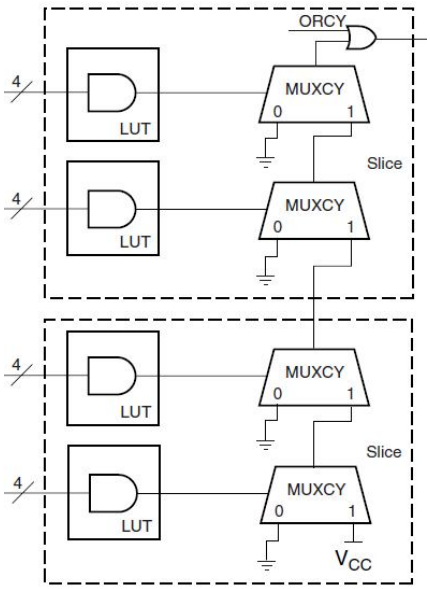


Fig.10. Efficient AND OR Logic Implementation

The three interpolators for next stages have been designed using Park McClellan algorithm to provide optimized filter order. When it comes to implementing an interpolation filter with a rate of two, the half band filter is more suitable as it requires much less hardware which in turn reduces the hardware complexity along with enhanced speed. The hardware reduction results from the fact that every odd indexed coefficient in the time domain is zero except the centre tap and even indexed coefficients are symmetric. Same half band concept is also used to implement the last three interpolators. All the interpolators are further supported by the concept of polyphase decomposition. Finally MAC algorithm is used to implement all four interpolators along with pipelined registers to enhance the speed performance of optimized WCDMA DUC.

The CORDIC algorithm based optimized DDS design has been used in place of DDS compiler block to generate sinusoidal waveform needed for frequency translation [22]. The developed DDS has been designed by efficiently utilizing the FPGA slice and its resources to implement efficient carry logic. The additional features of a slice, such as the wide multiplexers, carry logic, and arithmetic gates are efficiently utilized to enhance the performance. The Look-Up Table has been used as main resource for implementing logic functions of proposed DDS. Furthermore, the LUTs of each slice pair have been used as Distributed RAM to store data and 16-bit shift register to implement the DDS efficiently. The output of the LUT has been connected to the wide multiplexer logic, the carry and arithmetic logic to perform more complex logic operations of DDS. The carry chain, along with dedicated arithmetic logic gates has been used to support fast and efficient implementations of math operations used in CORDIC algorithm based DDS. The gates and multiplexers of the carry and arithmetic logic are further used for general-purpose logic, including simple wide Boolean functions. The embedded multipliers have been used to implement the complex multiplication to generate real and imaginary mixer outputs.

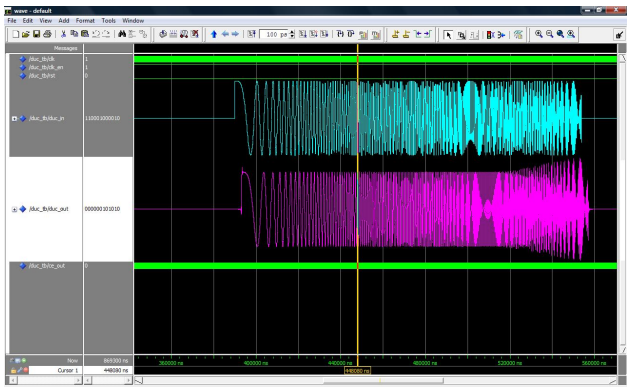

Fig. 11. Modelsim Based Optimized WCDMA DUC Response

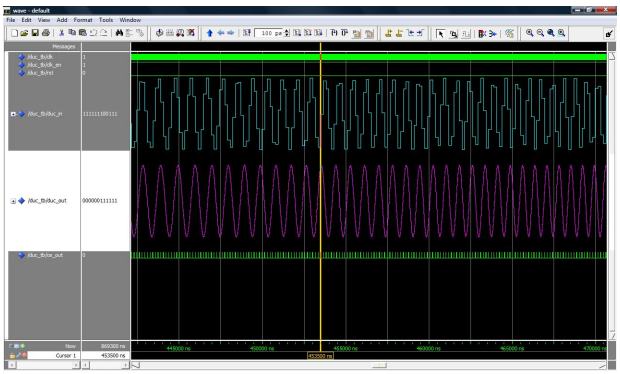

Fig. 12 Optimized WCDMA DUC Zoomed in Response

Finally optimized VHDL code is developed and synthesized on Virtex-II Pro based xc2vp30-7ff896 target device using Xilinx Integrated Software Environment (ISE) tool. The developed VHDL is simulated using Modelsim Simulator whose output response is shown in Fig.11 and its equivalent zoomed in output response is shown in Fig.12. To achieve optimized logic synthesis, the RTL level design has been partitioned in such a way that the critical timing paths are confined to individual modules because critical paths that span large numbers of hierarchical modules can be difficult to floor plan. The RTL view of Proposed Optimized DUC has been shown Fig.13.

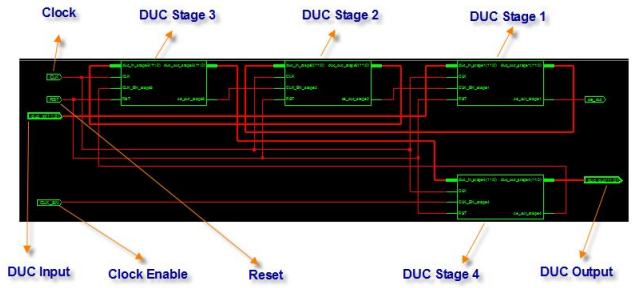


Fig.13. RTL view of Optimized Proposed WCDMA DUC

The internal RTL view of DUC stage has been shown in Fig.14. The outputs of all the modules have been stored in output register to limit the number of modules involved in a critical path. Long paths in single large hierarchical block have been avoided for simple and efficient floor planning. The large hierarchical blocks in the RTL have been divided in sub blocks.

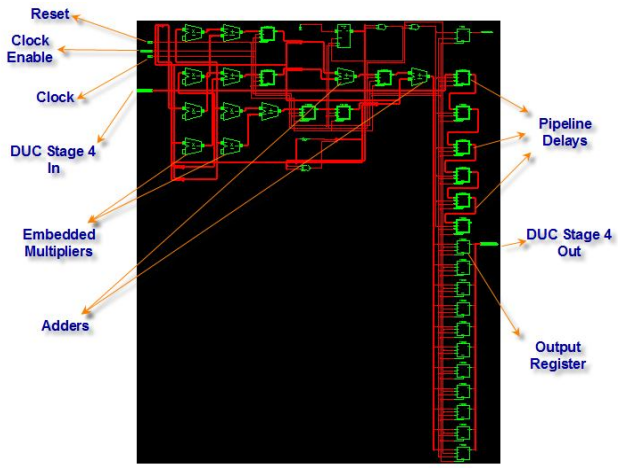


Fig.14. Internal RTL View of DUC Stages

The I/O package pin assignments has been done dragging and dropping groups of ports with semi automatic package pin placement algorithm. Ports have been assigned semi automatically by selecting the ports in the I/O Ports view, and by dragging them onto valid package pins in the Package view. Groups of pins or interfaces have been placed together by selecting multiple pins and dragging them onto valid site locations as shown in Fig. 15. Once the design I/O ports have been placed, DRC is performed to ensure legal placement. To improve the performance of design the route delay has been reduced in the design through floor planning.

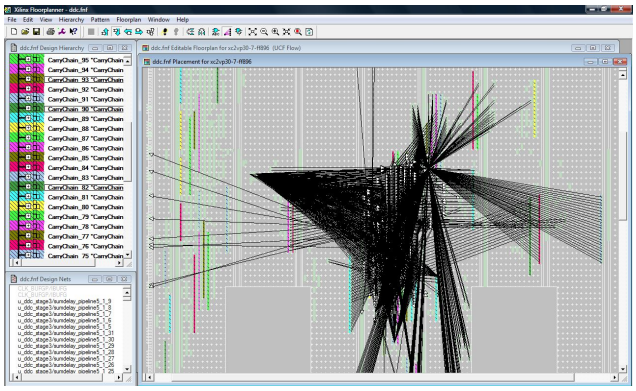

Fig.15. DUC Floorplanning

Logic delay limits the amount of performance gain that can be achieved. This logic delay is modified by DCM phase shifts for paths at an I/O. The top-level floor planning technique is used for analysis as it tends to isolate all modules leading to poor implementation results.

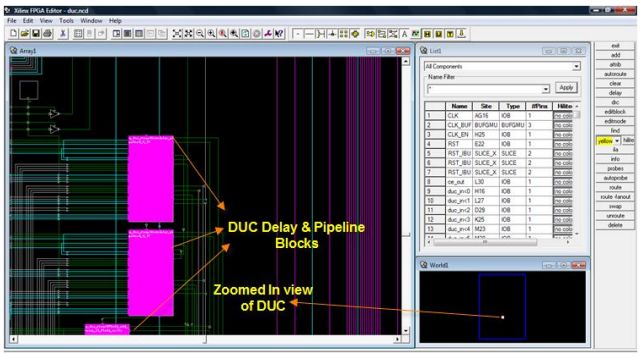


Fig.16. WCDMA DUC Routing

In floor planning only the hierarchies that contain the critical path have been constrained for improved performance. In some places, the hierarchy that is connected to fixed silicon resources like I/Os has also been floor planned. This optimized floor planning results in improved placement and routing of the developed WCDMA DUC design. After final floor planning

netlist has been developed for efficient placement that meets the required timing constraints. Then the optimized ncd file is created for optimal routing of proposed DUC design. The routed design shown in Fig. 16 is finally mapped on the target FPGA for implementation. Finally the developed WCDMA DUC design has been synthesised on Virtex-II Pro based xc2vp30-7ff896 target device. The resource consumption of proposed design on specified target device is shown in Table 3.

TABLE 3
WCDMA DUC RESOURCE UTILIZATION

| Logic Utilization | Used | Available |
|---|---|---|
| Number of Slices | 918 | 13696 |
| Number of Flip Flops | 1673 | 27392 |
| Number of LUTs | 1078 | 27392 |
| Number of MULTs | 47 | 136 |

The proposed optimized WCDMA design can operate at a maximum frequency of 147 MHz as compared to 122.88 MHz in case of [17]. The developed WCDMA DDC design has consumed 918 slices, 1673 flip flops, 1078 LUTs and 47 multipliers available on target FPGA device.

## VI. CONCLUSION

In this paper speed efficient and cost effective design of digital up converter has been presented. The existing designs suffer from the drawback of cost effectiveness because of their implementation on DSP 48E slice based Virtex 4 and Virtex 5 FPGAs. The WCDMA DUC design has been developed and implemented on multiplier based Virtex II Pro target FPGA. In developed WCDMA DUC, pulse shaping filters and other interpolators have been optimized separately and then cascaded together. The optimized VHDL code has been developed by combining multiplier less and multiplier based techniques using pipelined approach which is then converted into its equivalent register transfer level (RTL) logic. The developed RTL logic has been efficiently floor planned for optimal routing of the developed WCDMA DUC to achieve the desired timing constraints. The developed WCDMA DUC has shown improved speed performance and resource utilization to provide cost effective solution for SDR based mobile communication applications.

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## BIOGRAPHIES

**Rajesh Mehra** is currently Associate Professor in Electronics & Communication Engineering Department at National Institute of Technical Teachers' Training & Research, Chandigarh, India. He is pursuing his PhD from Panjab University, Chandigarh, India. He has completed his M.E. from NITTTR, Chandigarh, India and B.Tech. from NIT, Jalandhar, India.

He has 17 years of academic experience. He has authored 100 research papers out of which more than 50 are in reputed International Journals and more than 50 are in National and International conferences. His Current research and teaching interest are VLSI Design, Embedded System Design, Advanced Digital Signal Processing, Wireless & Mobile Communication, Digital and Embedded System Design.

Mr. Mehra has Guided more than 30 ME thesis and authored one book on PLC and SCADA. Mr. Mehra is member of IEEE and ISTE.

**S S Pattnaik** has received Doctor of Philosophy degree in Engineering. He is Professor & Head with the Department of Education & Television,, National Institute of Technical Teachers' Training & Research, Ministry of Human Resource Development, Chandigarh, India.

He has more than 20 years of teaching experience and 3 years of research experience. His current research and teaching interests are in Digital Signal Processing; Artificial Neural Networks; and Antenna & Radar Engineering.

Dr. Pattnaik has guided 35 ME thesis and 05 PhD thesis. He has more than 150 Journal and Conference publications. Dr. Dr. S S Pattnaik is senior member IEEE and life member of ISTE and IETE.