Calibration of Nonlinear Radix in Pipelined Analog-to-Digital Converters Using a Correlation Algorithm

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***Abstract*—The devices used in current integrated circuits technology are mostly non-linear. This issue makes the matching between such devices almost impossible. In pipelined analog-to-digital converters (ADC), this implies that achieving to the accuracies more than those allowable by the error sources is impossible without using an effective calibration technique. It can be shown by simulations that the number of the front-end stages that should be calibrated is larger than the difference of the maximum achievable bits without calibration and the required bits of the converter. In this paper, a discussion is provided on the modeling of the important error sources of the pipelined ADC in gain of the stages, and then, a novel approach is proposed for the non-linear calibration of the ADC stages.**

***Index Terms*—pipelined analog-to-digital converters, Digital calibration.**

I. Introduction

Fig. 1 shows the block diagram of a conventional pipelined ADC. It is composed of N consecutive stages, each of which is comprised of a $k-$bit sub-analog-to-digital converter (sub-ADC), a $k-$bit sub-digital-to-analog converter (sub-DAC), an analog differentiator, an amplifier and a sampler. To implement this architecture, the $k-$bit sub-DAC, analog subtractor, amplifier and sampler are all implemented by a basic block named MDAC. The MDAC consists of an op-amp, and a number of capacitors and switches. The sub-ADCs at the input of the stages are realized by some comparators, which can be designed using an arrangement of some transistors. At each stage, an estimate of the input is converted to digital codes by the sub-ADC with a low accuracy, and the result is converted back to an analog signal by the sub-DAC. This converted signal is then subtracted from the input signal by the subtractor. The residue signal is equivalent to the quantization noise resulting from analog to digital conversion at that stage. This residual noise is then amplified and transferred to the next stage to be processed further for more accuracy. The main advantage of pipelined ADCs is their ability for sequential analysis of the different data samples at different stages. In other words, when the MDAC of one particular stage is amplifying the residual noise of a sample, the MDAC at previous stage is sampling the same sample. This increases the conversion rate to a limiting factor based on the time required for each stage to propagate the analog signal.

The comparators have a large offset, leading to missing of some information due to output saturation. To avoid this drawback, two semi-calibration methods are used in practice: analog error correction and digital error correction. In the former, the gain of the stages is reduced in order to avoid the saturation of the MDAC stages due to the false decision of the comparators, and some stages are added at the output of the converter to compensate the gain reduction. In the latter, the number of the comparators is increased at each of the stages [1], [2].

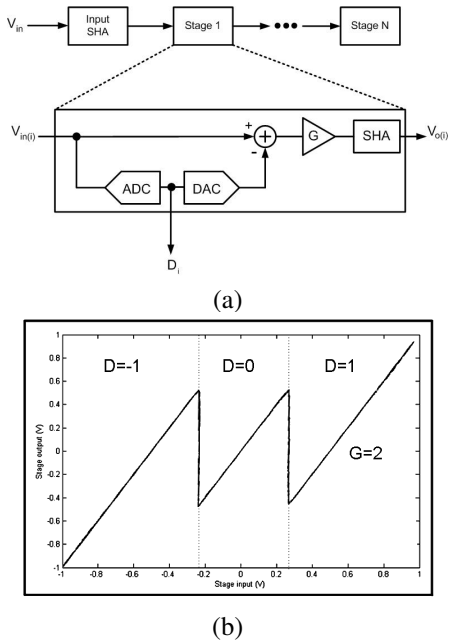

Fig. 1. Block diagram of a conventional pipelined ADC and its transfer function (a) Block diagram, (b) 1.5-bit transfer function.

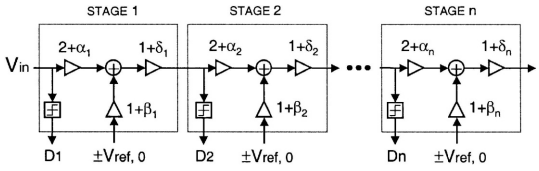

Fig. 2. Block diagram of a functional pipelined ADC [3]

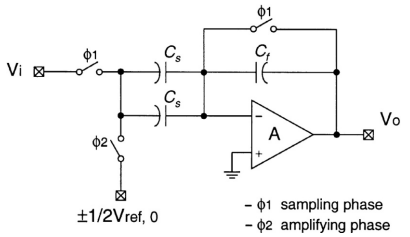

Fig. 3. The employed MDAC suited for the proposed calibration algorithm.

II. Modeling the Error of the Stages

The ideal characteristic of each 1.5-bit stage is as follows:

$$V_O = 2.V_i - D.V_{REF} = 2.(V_i - D.V_{REF}/2) \quad (1)$$

In the implementation of the ADC, the MDAC of the stages has non-ideal effects at the transistor level such as: poor matching between the capacitors and limited gain of the amplifiers, which causes error in processing of the analog signal. Fig.2 shows the functional block diagram of a pipelined ADC, where α_i ,β_i and γ_i are the errors caused by imperfect matching of the capacitors and the limited gain of the amplifiers. According to this figure, the non-ideal analog output of the MDAC at each stage is:

$$V_O = (1+\gamma).(2+\alpha).(V_i - D_i.\frac{1+\beta}{2+\alpha}.V_{REF}) \quad (2)$$

Comparing (2) with (1), it can be seen that by considering $ra = (1+\gamma).(2+\alpha)$ as the non-ideal radix of the 1.5-bit stages (instead of 2), and by considering $2(1+\beta)/(2+\alpha).V_{REF}$ (instead of the voltage V_{REF}) as the non-ideal reference voltage in each stage, the corrected digital output can be derived from the analog input as:

$$\begin{aligned} D_{out} &= D_n + D_{n-1}.ra_{n-1} + D_{n-2}.(ra_{n-1})(ra_{n-2}) \\ &\quad +... + D_1.(ra_{n-1})(ra_{n-2})...(ra_2)(ra_1) \end{aligned} \quad (3)$$

It is worth mentioning that the above modeling is correct only when the MDAC is implemented by using the architecture presented in Fig.3, because the non-ideal reference voltages are different in different stages. More specifically, in this structure, both the analog input and the reference voltage see the same error from the output, and the effect of this error can be included in radixes.

Compared to the Capacitor Flip-over structure, this architecture is favorable in terms of error modeling. Nonetheless, a capacitor filip-over MDAC has the advantage of a higher feedback factor at the amplification phase. So, it can be implemented with a higher bandwidth and, accordingly, lower power consumption. To employ the Capacitor Flip-over technique on one hand, and utilize the modeling given in (4) for calibration on the other hand, the analysis presented in [3] is of great importance. Using the systematic analysis and changing the usual locations of input and output nodes, the modified radix of the stages is obtained as [3]:

$$ra_i = (1+\beta_i).(1+\gamma_i).(\frac{2+\alpha_{i+1}}{1+\beta_{i+1}}) \quad (4)$$

where α_i ,β_i are the error sources of the stage $i = 1$. It is clear that for the modeling in [3], the Capacitor Flip-over structure is used in the analog stages. When we combine (3) and (4) to correct the error due to the limited gain of the amplifiers and the capacitors mismatch by the calibration, just one point remains: the time-varying offset resulted from changing the conventional input and output of the stages, which is completely eliminated by the digital correction of the error in the pipelined analog-to-digital converters. According to this modeling, the employed structure for implementing the stages in the analog domain is not the concerning issue and it suffices to only calculate the unknown coefficients ra in the digital domain by the calibration. Modeling the transfer function by considering a constant number as the radix of the stages is effective on the correction of the converter error and increase of its effective bits; however, the increase in the effective bits is upper-limited because the gain of MDAC depends on its output voltage. Generally, the non-linearity of the radix of the MDAC stage has different reasons. The most important reasons are the limitation of the cycling rate and the non-linearity of the amplifier. The effect of cycling rate limitation can be modeled in the steady state gain as follows:

$$V_O = (G + B.(\frac{V_O}{V_{REF}})^2 + C(\frac{V_O}{V_{REF}})^4 + ...).(V_i - D.\frac{V_{REF}}{2}) \quad (5)$$

where G is the gain factor of MDAC. In this expression, by omitting the terms with the orders greater than 2, the non-linear radix of the stages can be modeled as follows:

$$ra = G + B.(\frac{V_O}{V_{REF}})^2 \quad (6)$$

The use of this relation as the radix of the stages and finding the unknown coefficients B and G in digital domain, especially for the first stages, is very important. These two factors can decrease the conversion error and increase the number of effective bits, SNDR and SFDR. Fig. 4 shows the frequency spectrum of a pipelined analog-to-digital converter with a sampling rate of 65 MS/s, when the extraction of the output bits are performed for the three different cases of no calibration with assumed gain of 2, the calibration with the equal gains, and the calibration with the non-linear gain, as given in (6), for the first stage. The first stage of this converter is simulated by using the industrial models of the 0.18 μm in HSpice. As it is seen, the use of the non-linear gain instead of the linear gain increases SNDR by about 3 dB and SFDR by about 8 dB. This modeling is used for the calibration of radix of the first stage, and the unknown coefficients B and G are obtained by the proposed algorithm. However, for those stages placed after the first stage, which are less important, a constant radix is used.

III. The Proposed Method To Find The Non-Linear Radix Of The Stages

As stated in the previous section, modeling the radix of stages with a constant coefficient is not precise and limits the upper effective number of bits. Therefore, the model in (6)

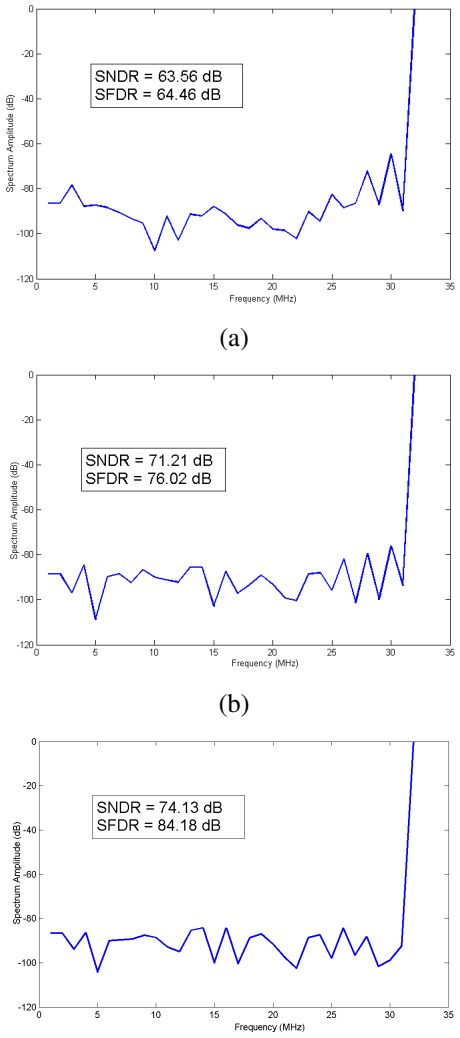

Fig. 4. The output frequency spectrum of a pipelined analog-to-digital converter, (a) without calibration, (b) with calibration with constant radix, and (c) with calibration with variable radix.

should be used for the first stages which are more important. When using this model, it is important to develop a simple algorithm to calibrate the parameters B and G. By implementing these methods in the background, the information is not destroyed, and the calibrations at different frequencies are processed simultaneously because of the statistical nature of the calibration signal.

Fig. 5 shows the proposed method for finding B and G by means of the correlation algorithm when all the voltages are normalized to V_{REF}. Moreover, the parameters $\bar{B}$ and $\bar{G}$ are the estimations of B and G in the digital domain which converge to their actual values by calibration. In this structure, the random sequence P_N is used as the calibration signal. This signal has the values ± 1, which after being multiplied with $\frac{1}{4}$, enters the sub-ADC. This signal passes through the amplifier block which contains the actual radix of the stage. This is quantized by the previous stage, and is converted to digital with the main signal. As it is clear, the digital output equals

$$\begin{aligned} D_O &= (V_i + Q_N + \frac{1}{4}P_N).(\bar{G} + \bar{B}.V_O^2) \\ &\quad -(Q_N + (\frac{1}{4}P_N)).(G + B.V_O^2) + O_N \\ &= V_i.(\bar{G} + \bar{B}.V_O^2) + Q_N.((\bar{G} - G) + (\bar{B} - B).V_O^2) \\ &\quad + \frac{1}{4}P_N.((\bar{G} - G) + (\bar{B} - B).V_O^2) + O_N \end{aligned} \quad (7)$$

If the correlation between this output and the random sequence is calculated, the following relation will be obtained for the instantaneous gain error (e_G):

$$e_G = \frac{1}{4}((\bar{G} - G) + (\bar{B} - B).V_O^2) \quad (8)$$

As it can be seen, this relation depends on the output voltage of the stage. Therefore, the obtained precision is limited when trying to minimize the correlation error. It is important to note that the current approaches for calculating the non-linear radix coefficients are rather complicated, and cannot be used in all possible architectures proposed so far. In [4], two possible statistical levels are used within the MDAC input-output transfer function to generate a random sequence for calibration. It is, however, only applicable to the 1 bit/stage structure with open-loop operational amplifiers. In [5], by using the model in (6), a decision/forced algorithm is utilized to obtain the non-linear coefficient. The deficiency of this method is the use of the queue structure in the converter input to free the timing slots for the calibration, which applies a lot of noise to the converter input as well as extra power and area.

In this paper, the correlation of P_N and the digital output $\frac{D_o}{V_o^2}$ is used to obtain the coefficient B. According to (7), $\frac{D_o}{V_o^2}$ is equal to:

$$\frac{D_O}{V_O^2} = (V_i + Q_N + \frac{1}{4}P_N)(\frac{\bar{G}}{V_O^2} + \bar{B}) - (Q_N + \frac{1}{4}P_N)(\frac{\bar{G}}{V_O^2} + \bar{B}) \quad (9)$$

Therefore, the correlation of $\frac{D_o}{V_o^2}$ with P_N can be written as:

$$e_B = \frac{1}{4}(\frac{\bar{G} - G}{V_O^2} + (\bar{B} - B)) = \frac{1}{4}(\bar{B} - B). \quad (10)$$

In (10), it is assumed that $\bar{G}$ converges G. So, we have

$$B = \bar{B} - 4e_B. \quad (11)$$

The following relations can be therefore used to calibrate B and G:

$$G[n+1] = G[n] - \Delta_G(D_O \otimes P_N) \quad (12)$$

$$B[n+1] = B[n] - \Delta_B(\frac{D_O}{V_O^2} \otimes P_N) \quad (13)$$

where Δ_B and Δ_G are the updating steps to update B and G, respectively. Note that if $\bar{G}$ is not converged to G, error occurs in (15). However, as the error due to B is smaller than the error due to G, after allowing G to be converged

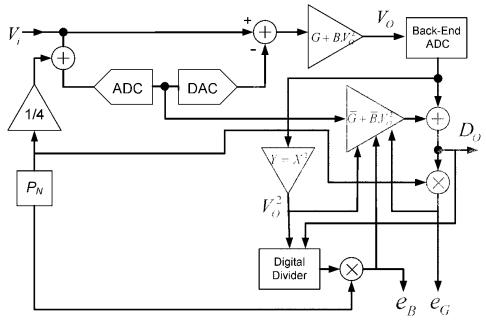

Fig. 5. The proposed structure for extracting the parameters B and G.

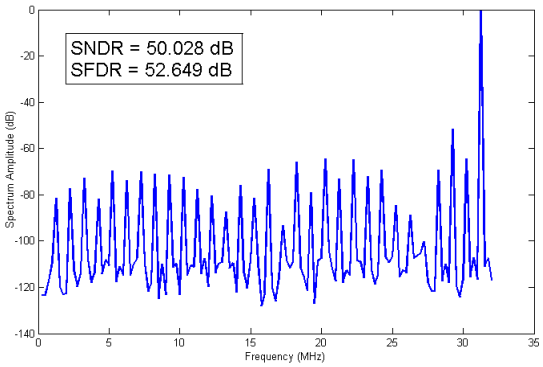

Fig. 6. The frequency spectrum of the converter output after non-linearization of the radix of the first stage

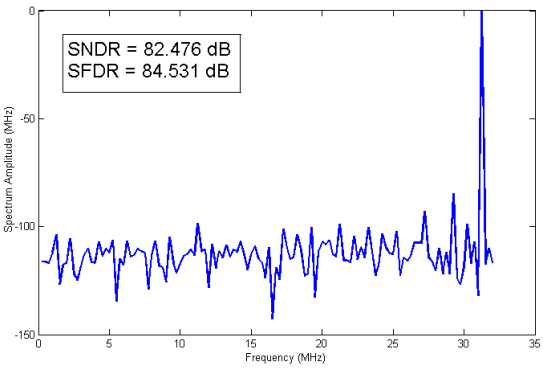

Fig. 7. Frequency spectrum after calibrating the first stage

as accurate as possible, the relation (13) is used to make the value of B converge, and then, G is calculated again according to the updated value of B. This procedure continues until achieving the required accuracy. By looking at (10), another problem of this algorithm is revealed for the convergence of B. If G is not converged to its final value, the first term of this relation can become so large for small input amplitudes, leading to the divergence of B. When implementing this method in the background for updating B, the solution to this problem is the elimination of the effect of the inputs with the amplitudes below a threshold which, however, slows down the calibration. This problem does not exist in the foreground, and the amplitude of the stage input can be considered to be constant, and equal to the decision point of one of the comparators, e.g. $\frac{V_{REF}}{4}$.

IV. Numerical Results

In this section, the performance of the proposed calibration algorithm is studied by simulations. MATLAB software is used for the simulation of the pipelined analog-to-digital converter. The simulated pipelined analog-to-digital converter is 14-bit with the sampling frequency of 65 MS/s with the calibration. To demonstrate the accuracy of the proposed algorithm, radix of the first stage is assumed non-linear and dependent on the output voltage. The constant radix of the stage, G, is considered to be 1.98 instead of its ideal value, i.e. 2, and also the non-linear coefficient of radix, B, is considered to be –0.01 instead of the ideal value 0.

Considering the extracted bits of the converter, the number of effective bits showed to be 14.08 for the ideal case with Nyquist input. In Fig. 6, the 256-point frequency spectrum of the digital output of the converter is shown for the Nyquist input after non-linearizing the radix of the first stage. From obtained SNDR, it is seen that the maximum attainable number of effective bits is 8.1 bits for Nyquist input. However, by applying the proposed algorithm to the converter in the background and finding the constant gain of the first stage, G, and non-linear gain, B, the performance of the converter is corrected. To do so, the constant gain is updated for 5000 iterations with the average of the multiplication of every 64 samples and the calibration signal. At this stage, the non-linear gain factor, B, is considered to be constant. After that, G is considered to be constant, and B is updated in 5000 iterations. This procedure is repeated until the required accuracy of the ADC is met. In our simulations, the procedure is repeated two-times to reach to the accuracy of 14 bits.

Finally, the frequency spectrum of the output signal in the Nyquist frequency is shown in Fig. 7 after applying the proposed calibration algorithm. As it can be seen, the SNDR increases after the calibration considerably, and the number of effective bits increases from 8.1 to 13.4 bits in the input Nyquist frequency.

V. Conclusion

In this paper, the modeling of the important sources of error in the pipelined analog-to-digital converters has been addressed. A novel algorithm is proposed for the calibration of the non-linear radix of the stages based on the correlation algorithms. The simulation results have shown the ability of this algorithm for the non-linear calibration of the non-linear gain of the stages.

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