Analytical Modelling and Performance Analysis for Symmetric Double Gate Stack-Oxide Junctionless FET in Subthreshold Region

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***Abstract*—In this paper, we propose a two-dimensional analytical model of single material symmetric Double Gate Stack-Oxide Junctionless Field Effect Transistor (DGS-JLFET) for subthreshold region. This model has been investigated and expected to improve subthreshold characteristics and minimize short channel effects. The characteristics of DGS-JLFET are compared with those of the single material symmetric Double Gate Junctionless Field Effect Transistor (DG-JLFET). Our proposed DGS-JLFET exhibits higher I_{on}/I_{off} ratio, less subthreshold swing (SS) and less drain induced barrier lowering (DIBL) when compared to DG-JLFET.**

Keywords-Double Gate Stack-Oxide Junctionless Field Effect Transistor (DGS-JLFET), Double Gate Junctionless Field Effect Transistor (DG-JLFET), short channel effect (SCE), on-off ratio (I_{on}/I_{off}), subthreshold swing (SS), drain induced barrier lowering (DIBL).

I. INTRODUCTION

With the decreasing dimension, various Short Channel Effects (SCE) like hot carrier injection, oxide leakage, Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS) cause unwanted effects in MOSFET characteristics [1]-[3]. Junctionless transistor shows improved electrostatic characteristics like low DIBL, low leakage current, low SS, high I_{on}/I_{off} ratio [4]-[7]. Several researches have been done on different structures of Junctionless Field Effect Transistors [8]-[11]. But no established research has been done on single material symmetric Double Gate Stack-Oxide Junctionless Field Effect Transistor (DGS-JLFET). This work proposes a physics based 2-D electrostatic potential model in subthreshold region for DGS-JLFET structure. The performance analysis of subthreshold behavior (DIBL, SS and I_{on}/I_{off} ratio) has been made between our proposed model and DG-JLFET.

II. MODEL DEVELOPMENT

The cross-sectional view of an n-type DGS-JLFET used for our analytical modeling is shown in Fig. 1 where X-axis indicates the source to drain and Y-axis indicates top to bottom gate direction. The thickness of the source and drain regions are assumed to be zero to simplify our analytical model. The silicon substrate is heavily doped with n-type

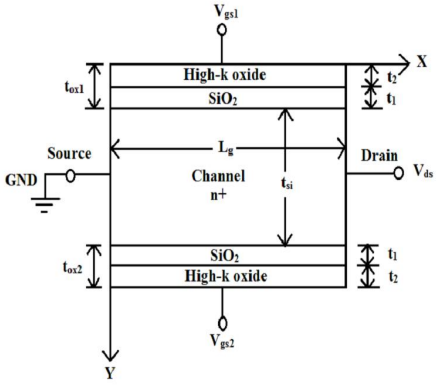


Figure 1. Cross-sectional view of DGS-JLFET

impurity. L_g is the channel length, t_{si} is the channel thickness, t_{ox1} and t_{ox2} are respectively the top and bottom gate oxide thickness, V_{gs1} and V_{gs2} are respectively the top and bottom gate bias. The source is connected to ground and V_{ds} is applied to the drain.

2-D Poisson's equation for n-channel DGS-JLFET can be expressed as,

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=-\frac{qN_d}{\varepsilon_{si}}, \quad \begin{matrix}0\le x\le L_g\\ 0\le y\le t_{si}\end{matrix} \tag{1}$$

where $\Phi(x,y)$ is the 2-D channel potential, q is the elementary charge, N_d is the uniform doping concentration in the channel region and ε_{si} is the dielectric constant of silicon. Assuming cubic potential distribution along the top to bottom gate direction, we can write

$$\phi(x,y)=c_o(x)+c_1(x)y+c_2(x)y^2+c_3(x)y^3 \tag{2}$$

where, $\begin{matrix}0\le x\le L_g\\ 0\le y\le t_{si}\end{matrix}$

The coefficients $c_o(x)$, $c_1(x)$, $c_2(x)$ and $c_3(x)$ are solved using the appropriate boundary conditions.

Boundary conditions at the top/bottom gate oxide and silicon channel interface are given by,

$$\phi(x,y)\Big|_{y=0} = \phi_{s1}(x) \tag{3}$$

$$\phi(x,y)\Big|_{y=t_{si}} = \phi_{S2}(x) \tag{4}$$

According to Gauss's law, the electrical flux between the silicon channel and gate oxide must be continuous. The electric fields at the top/bottom gate oxide and channel interface are given as:

$$\left.\frac{\partial\phi(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox1}}{\varepsilon_{si}}\cdot\frac{\phi_{S1}(x)-V_{gs1}+V_{fb1}}{t_{ox1}} = \frac{\varepsilon_{ox1}}{\varepsilon_{si}}\cdot\frac{\phi_{S1}(x)-V'_{gs1}}{t_{ox1}} \tag{5}$$

$$\left.\frac{\partial\phi(x,y)}{\partial y}\right|_{y=t_{si}} = \frac{\varepsilon_{ox2}}{\varepsilon_{si}}\cdot\frac{V_{gs2}-V_{fb2}-\phi_{S2}(x)}{t_{ox2}} = \frac{\varepsilon_{ox2}}{\varepsilon_{si}}\cdot\frac{V'_{gs2}-\phi_{S2}(x)}{t_{ox2}} \tag{6}$$

Here, ε_{ox1} and ε_{ox2} are the permittivity of the top and bottom gate oxide, respectively. The effective top and bottom gate biases are $V'_{gs1} = V_{gs1}-V_{fb1}$ and $V'_{gs2} = V_{gs2}-V_{fb2}$ respectively. The flat-band voltages V_{fb1} and V_{fb2} are written as, $V_{fb1} = \phi_{m1} - \phi_s$ and $V_{fb2} = \phi_{m2} - \phi_s$ where ϕ_{m1} and ϕ_{m2} are the work functions of the top and bottom gate electrodes respectively and ϕ_s is the work function of silicon which can be written as,

$$\phi_s = \chi_s + \frac{E_g}{2q} - V_t \ln\left(\frac{N_d}{n_i}\right) \tag{7}$$

Where V_t is the thermal voltage, χ_s is the electron affinity, E_g is the bandgap energy and n_i is the intrinsic carrier concentration of silicon.

In the case of stack oxide, a gate dielectric with a dielectric constant ε which is higher than that of SiO_2 (ε_{ox}) will achieve a smaller equivalent electrical thickness (t_{eq}) than the SiO_2, even with a physical thickness (t_{phys}) larger than that of the SiO_2 (t_{ox}) [12]:

$$t_{eq} = \left(\frac{\varepsilon_{ox}}{\varepsilon}\right) t_{phys} \tag{8}$$

For this reason, we can write,

$$t_{ox1} = t_{ox2} = t_1 + \frac{\varepsilon_1}{\varepsilon_2}\cdot t_2 \tag{9}$$

Here, t_{ox1} and t_{ox2} are respectively the top and bottom gate oxide thickness and t_1 and t_2 are respectively the physical thickness of SiO_2 and high-k oxide layer.

The boundary conditions of potential at the source and drain terminal of the device are as follows:

$$\phi(x,y)\Big|_{x=0} = 0 \tag{10}$$

$$\phi(x,y)\Big|_{x=L_g} = V_{ds} \tag{11}$$

Now, using 1-D capacitance model, assuming 1-D potential line along the source to drain direction [13] and finally solving for the general solution of ordinary differential equation, we get the equation for surface potential for single material double gate stack-oxide JLFET,

$$\phi(x,y) = \frac{(V_{ds}-\gamma_Y)\sinh\left(\frac{x}{\lambda_Y}\right) - \gamma_Y \sinh\left(\frac{L_g-x}{\lambda_Y}\right)}{\sinh\left(\frac{L_g}{\lambda_Y}\right)} + \gamma_Y \tag{12}$$

where,

$$\gamma_Y = \alpha_Y + \beta_Y \lambda_Y^2 \tag{13}$$

$$\lambda_Y = \sqrt{\frac{1+\frac{\varepsilon_{ox1}}{\varepsilon_{si}t_{ox1}}\cdot Y - \frac{1}{\varepsilon_{si}t_{si}}\left(\frac{2\varepsilon_{ox1}}{t_{ox1}}-\frac{\varepsilon_{ox2}}{t_{ox2}}\right)Y^2 + \frac{1}{\varepsilon_{si}t_{si}^2}\left(\frac{\varepsilon_{ox1}}{t_{ox1}}-\frac{\varepsilon_{ox2}}{t_{ox2}}\right)Y^3}{\frac{2}{\varepsilon_{si}t_{si}}\left(\frac{2\varepsilon_{ox1}}{t_{ox1}}-\frac{\varepsilon_{ox2}}{t_{ox2}}\right) - \frac{6}{\varepsilon_{si}t_{si}^2}\left(\frac{\varepsilon_{ox1}}{t_{ox1}}-\frac{\varepsilon_{ox2}}{t_{ox2}}\right)Y}} \tag{14}$$

$$\alpha_Y = -\frac{\varepsilon_{ox1}}{\varepsilon_{si}t_{ox1}}V'_{gs1}.Y + \left[\frac{1}{\varepsilon_{si}t_{si}}\left(\frac{2\varepsilon_{ox1}}{t_{ox1}}V'_{gs1}-\frac{\varepsilon_{ox2}}{t_{ox2}}V'_{gs2}\right) - \frac{(\varepsilon_1\varepsilon_2^2)^2(V'_{gs1}-V'_{gs2})(3\varepsilon_{si}t_{ox2}+\varepsilon_{ox2}t_{si})}{\varepsilon_{si}t_{ox2}t_{si}\left[t_{si}(\varepsilon_1\varepsilon_2^2)^2+2\varepsilon_1\varepsilon_2^2\varepsilon_{si}(\varepsilon_1^2t_2+\varepsilon_2^2t_1)\right]}\right]Y^2 - \left[\frac{1}{\varepsilon_{si}t_{si}^2}\left(\frac{\varepsilon_{ox1}}{t_{ox1}}V'_{gs1}-\frac{\varepsilon_{ox2}}{t_{ox2}}V'_{gs2}\right) - \frac{(\varepsilon_1\varepsilon_2^2)^2(V'_{gs1}-V'_{gs2})(2\varepsilon_{si}t_{ox2}+\varepsilon_{ox2}t_{si})}{\varepsilon_{si}t_{ox2}t_{si}^2\left[t_{si}(\varepsilon_1\varepsilon_2^2)^2+2\varepsilon_1\varepsilon_2^2\varepsilon_{si}(\varepsilon_1^2t_2+\varepsilon_2^2t_1)\right]}\right]Y^3 \tag{15}$$

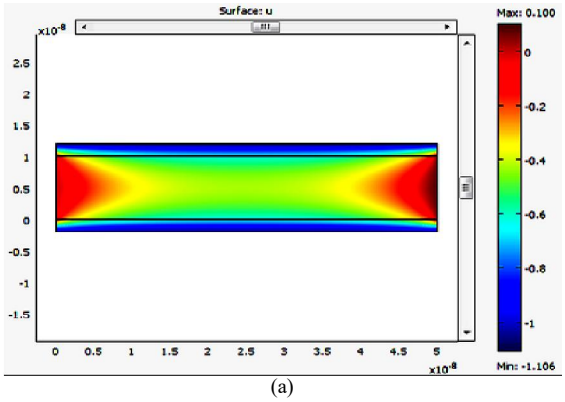
$$\beta_Y = \frac{2}{\varepsilon_{si}t_{si}}\left(\frac{2\varepsilon_{ox1}}{t_{ox1}}V'_{gs1} - \frac{\varepsilon_{ox2}}{t_{ox2}}V'_{gs2}\right) - \frac{2(\varepsilon_1\varepsilon_2^2)^2(V'_{gs1}-V'_{gs2})(3\varepsilon_{si}t_{ox2}+\varepsilon_{ox2}t_{si})}{\varepsilon_{si}t_{ox2}t_{si}\left[t_{si}(\varepsilon_1\varepsilon_2^2)^2 + 2\varepsilon_1\varepsilon_2^2\varepsilon_{si}(\varepsilon_1^2t_2+\varepsilon_2^2t_1)\right]}$$

$$+\frac{qN_d}{\varepsilon_{si}} - \left[\frac{\frac{6}{\varepsilon_{si}t_{si}^2}\left(\frac{\varepsilon_{ox1}}{t_{ox1}}V'_{gs1} - \frac{\varepsilon_{ox2}}{t_{ox2}}V'_{gs2}\right) - \frac{6(\varepsilon_1\varepsilon_2^2)^2(V'_{gs1}-V'_{gs2})(2\varepsilon_{si}t_{ox2}+\varepsilon_{ox2}t_{si})}{\varepsilon_{si}t_{ox2}t_{si}^2\left[t_{si}(\varepsilon_1\varepsilon_2^2)^2 + 2\varepsilon_1\varepsilon_2^2\varepsilon_{si}(\varepsilon_1^2t_2+\varepsilon_2^2t_1)\right]}}{}\right]Y \quad (16)$$

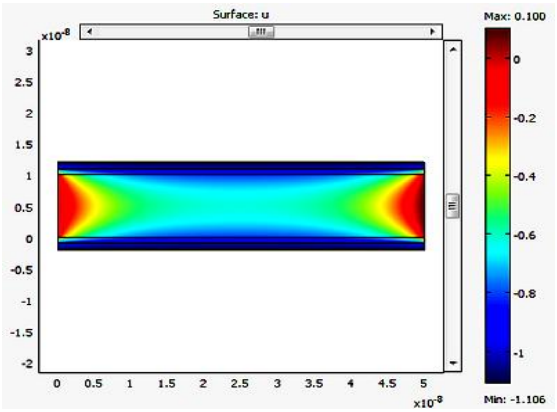
III. Simulation Results

A. Surface Potential Distribution and Model Verification

COMSOL Multiphysics is used to verify our model in which Poisson's equation with same boundary conditions is solved and the obtained results are matched with our model.



(a)

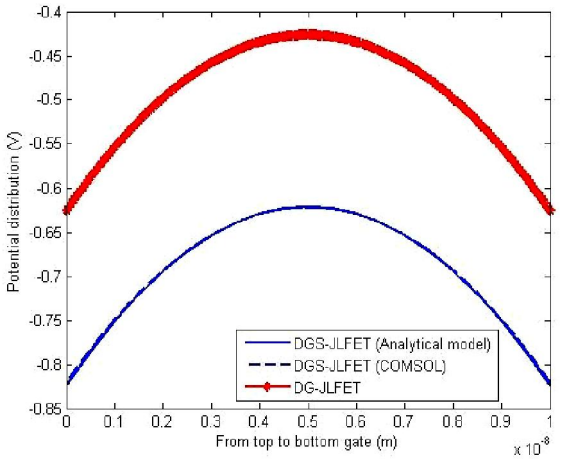


(b)

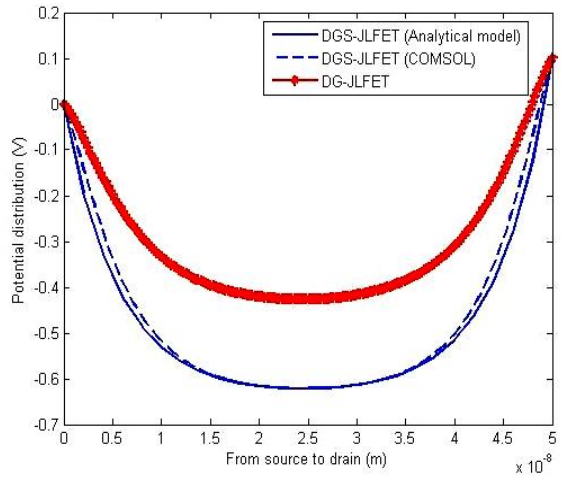
Figure 2. Surface potential distribution of (a) DG-JLFET and (b) DGS-JLFET (V_{gs} = 0) at V_{ds} = 0.1 V

For simulation, we used the parameters, t_{si} =10 nm, L_g = 50nm. For DGS-JLFET, t_1 = 1nm, t_2 = 1 nm, ε_1 = 3.9 (SiO_2), ε_2 = 20 (HfO_2) and for DG-JLFET, t_{ox1} = 2 nm, t_{ox2} = 2 nm, $\varepsilon_{ox1} = \varepsilon_{ox2}$ = 3.9 (SiO_2).

From Fig. 2(a) and 2(b), it can be seen that the central body potential is higher in DG-JLFET compared to DGS-JLFET. Fig. 3(a) and 3(b) show that potential profiles of our analytical model matched with those in COMSOL simulation and hence our analytical electrostatic potential model is verified. These two figures also compare the top to bottom gate and source to drain potential between DGS-JLFET and DG-JLFET. Both figures show higher potential in DG-JLFET compared to DGS-JLFET. As a result, more subthreshold current flows through DG-JLFET at off state compared to DGS-JLFET.



(a)



(b)

Figure 3. Comparison of I_{ds} vs V_{gs} characteristic between DGS-JLFET and DG-JLFET at V_{ds} = 0.1 V

B. *Drain Current versus Gate Potential (I_{ds} vs V_{gs})*

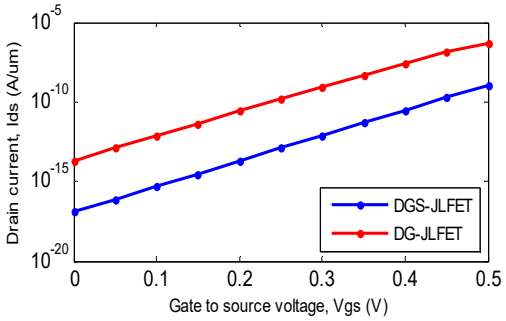


Figure 4. Comparison of I_{ds} vs V_{gs} characteristic between DGS-JLFET and DG-JLFET at V_{ds} = 0.1 V

Subthreshold current can be calculated as [14],

$$I_{ds} = \frac{q\mu_n W V_t \left(1 - e^{-\frac{V_{ds}}{V_t}}\right)}{\int_0^{L_g} \frac{dx}{\int_0^{t_{si}} n_i e^{\frac{\phi(x,y)}{V_t}} dy}} \quad (17)$$

Here, μ_n is effective mobility of silicon and W is the channel width. Surface potential $\phi(x,y)$ is calculated from Eq. (12) which we derived in the analytical 2-D model. For double gate junctionless FET (DG-JLFET), $\phi(x,y)$ is calculated from [13]. Subthreshold current has been plotted by numerical integration in MATLAB.

Fig. 4 shows the comparison of I_{ds} vs V_{gs} characteristic between DG-JLFET and DGS-JLFET. It can be seen that less subthreshold current flows through DGS-JLFET in off state.

C. *I_{on}/I_{off} Ratio*

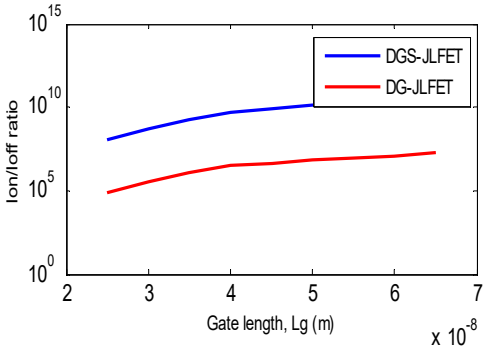


Figure 5. Comparison of I_{on}/I_{off} ratio between DGS-JLFET and DG-JLFET at V_{ds} = 0.1 V

Fig. 5 compares the I_{on}/I_{off} ratio between DG-JLFET and DGS-JLFET. It can be seen that DGS-JLFET shows 10^3 higher I_{on}/I_{off} ratio than DG-JLFET. That's why, DGS-JLFET gives better performance like low power consumption in off state and high current in on state.

D. *Subthreshold Swing (SS)*

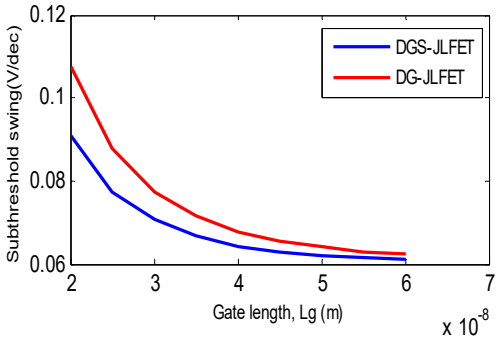


Figure 6. Comparison of SS between DGS-JLFET and DG-JLFET at V_{ds}=0.1V

Subthreshold swing is calculated from [14] as,

$$SS = \frac{\partial V_{gs}}{\partial \log_{10}(I_{ds})} \quad (18)$$

From Fig. 6, we can see that, as gate length increases to around 50 nm and above, the curve converges to 60 mV/decade [15]. For shorter gate length, this swing increases but DGS-JLFET always gives smaller subthreshold swing than DG-JLFET. For L_g = 20 nm, SS of DGS-JLFET is 17.5 mV/dec less than DG-JLFET.

E. *Drain Induced Barrier Lowering (DIBL)*

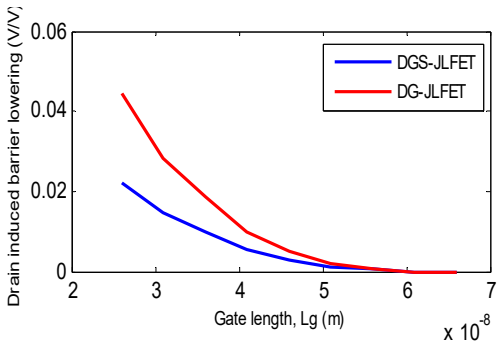


Figure 7. Comparison of DIBL between DGS-JLFET and DG-JLFET at V_{ds} = 0.1 V

DIBL is calculated from [14] as,

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = \frac{V_{th_L} - V_{th_H}}{V_{ds_H} - V_{ds_L}} \qquad (19)$$

Here, we have chosen V_{ds_L} = 0.1 V, V_{ds_H} = 1V, V_{th_L} is calculated at V_{ds_L} = 0.1 V and V_{th_H} is calculated at V_{ds_H} = 1 V. Fig. 7 compares DIBL between DG-JLFET and DGS-JLFET. When gate length gets shorter (35 nm or less), DGS-JLFET gives much lower DIBL compared to DG-JLFET. For L_g = 26 nm, DGS-JLFET shows 20 mV/V less DIBL than DG-JLFET.

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