Ternary CMOS Standard Cell Design

N.Khairudin, A.Abdul Aziz, M.T.A.Mohd Mabror

Abstract—In this paper a circuit design of ternary based on the multi-valued logic (MVL) is presented. Another alternative way to use ternary rather than binary it because of the complexity, delay and power consumption. Implementation of the MVL in logic design is better in data transfer rate compared to the binary interconnection system. Binary systems in field programmable gate array (FPGA) tend to dominate the delay, power and area. In ternary system, it has 3 different logic values 0, 1 and 2, whereas the binary logic it has 0 and 1. In this project the ternary standard cell circuit is introduced such as Ternary Inverter, Ternary NAND and Ternary NOR. The suggested design is synthesized using Cadence Software and the comparison is done in term of delay, number of interconnection and power.

Keywords- Ternary inverter; ternary NAND; ternary NOR; power consumption.

I. INTRODUCTION

In digital era, binary used to perform two valued logic. It is a conventional method because it only used two values. Multi valued-logic is a way to replace the conventional methods use by the binary. The main disadvantages of binary integration are the pin number and number of interconnection; because the limitation for each connection is vital and increasing. It also has more function than other MVL which in term of size and the performance for the chip. One of the example of the MVL usage is in Ternary logic [1]. The usage of the ternary logic is important to establish the good result for the ternary in term of complexity, number of interconnection and power consumption. One of the ultimate goal of multi-valued logic study is to enhance the design and fabrication of the MVL circuit application. In theory, multi-valued logic circuit have more advantages than the binary logic listed as following [2]: 1. MVL can transmit more data (bps) than binary, hence the connection inside the logic circuit can be reduced. 2. Complexity for MVL is less than binary application. 3. MVL use less number of pin in and pin out to reduce the pin-out difficulties. 4. MVL have great speed for the transmission of the serial information.

The authors are with the Faculty of Electrical Engineering Universiti of Teknologi Mara, 40450 Shah Alam, Selangor, Malaysia. hazlinkuth@gmail.com, anees.aziz@gmail.com, taufiq0703@gmail.com

In ternary system, three logic values are used which are 0, 1 and 2. As the reference, a basic CMOS ternary inverter schematic circuit is designed with three level of input and three level of output. Figure 1.0 shown the Ternary references voltage used for switching in three different values compare to binary.

Application of the MVL is to reduce the number of interconnection in the design. By reducing the number of interconnection, the parameter like the delay and size of the chip can be reduced. Designing the small and limited interconnection for the design can help increase the performance efficiency for the MVL rather than using binary logic design [3]. Hence, Ternary logic is developing to enhance the MVL application.

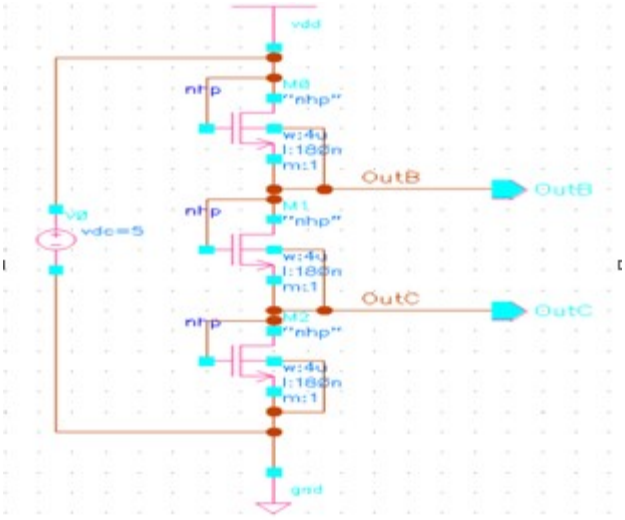


Figure 1.0: Ternary references voltage level

Ternary are represented by several digits which higher radices than the binary number system, hence it requires less logic digits data to establish and store data than using the binary.

Moreover, ternary device requires simple circuit combination to evaluate the data rather than using binary logic configuration.

The ternary standard cell CMOS are importance as the basic element for designing the ternary power comparison. In this paper, it is represented by the basic CMOS ternary standard cell and analysis have been done in Silterra 180nm Process Technology.

In order to develop the Ternary standard cell such as the inverter, NAND and NOR, Cadence software has been used. Some objectives have been set; to design Ternary standard cell with less interconnection and power consumption comparison for Ternary and Binary.

II. Methodology

In this project, all the design has been implemented by using the Cadence tool and Silterra 180nm process technology. Figure 2.0 shown the bottom level design process flow. The schematic design has been developed using Cadence Schematic Entry Environment and simulations on schematic have been done using Analog Design Environment tool in order to accomplish the simulation work. All the result produced will be used for analysis.

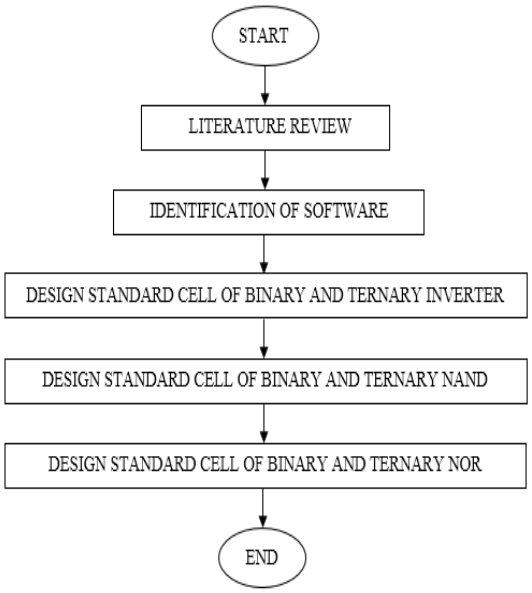


Figure 2.0: Bottom design process flow.

Based on the flowchart in Figure 2.0 is the process of collecting relevant data and information from the previous work that have been reported by other researches.

The next step is to design the standard cell for the Ternary CMOS inverter, Nand (TNAND) and Nor (TNOR). Next, it followed by simulating all the schematic design on Electronic Design Automation (EDA) tool. Truth table for all the ternary design circuit will be tabulated and recorded as the schematic is successful. From the results, the comparison can be made between the binary and ternary respectively.

III. Results and Discussion

Figure 3.0 shown the Ternary inverter (TINV) schematic design which has the combination of the inverter with three different switching threshold level.

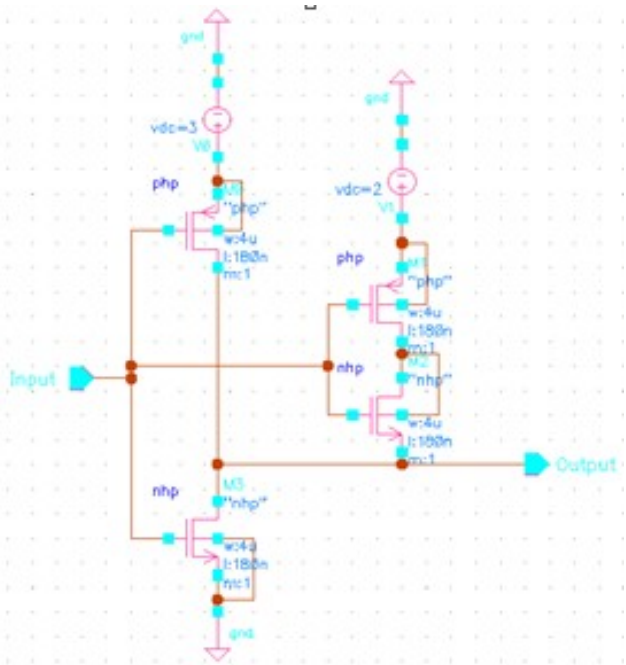
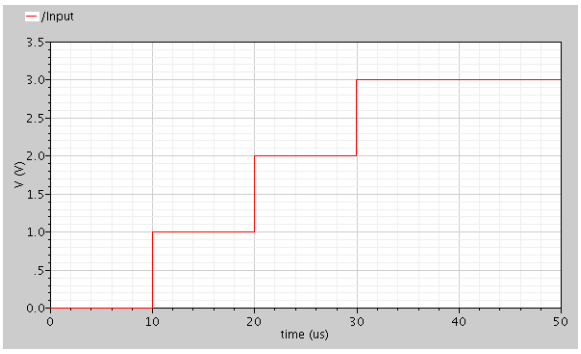
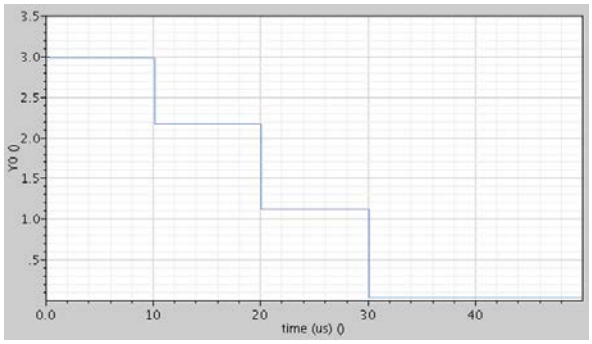


Figure 3.0: Ternary inverter

The schematic design circuit is supplied with different V_{DD} which is 2V and 3V. Then, at least 2 different threshold voltage (Vth) is used, for example 2 V and 3 V. This Vth is required in order to detect 3 different logic which is 0, 1 and 2 for the input signal. If the detection of the thresholds of the logic gate Pmos and logic gate Nmos are simulated at the same time, the output for the transistor is off for input 1 [4]. The traditional binary complementary metal oxide semiconductor (CMOS), it only can only handle pair of MOS enhancement [5]. If these both of the threshold voltage is changed, the transistor will turn off for the input 1.



(a)



(b)

Figure 4.0: (a)Ternary inverter input. (b) Ternary output simulation.

Based on the simulation result in Figure 4.0, the graph of voltage versus time in microsecond unit is presented. For every step of the input for each of interval is set at 10us. The graph produces in red line indicated as an input; for the first interval between 0 to 10us the input is 0 V then it is followed by the second interval between 10.001us to 20us as the input is 1 V. Then, the last interval is between 20.001us to 30us as the input voltage is 2 V.

Next, the graph produced in blue line indicate as the output for the ternary inverter. The result produced follow as the ternary inverter truth table tabulated in Table 1.0.

Table 1.0: Ternary inverter truth table

INPUT	OUTPUT
0	2
1	1
2	0

Based on the Figure 5.0, it shown the combination of the CMOS Ternary NAND with two input value and one output value.

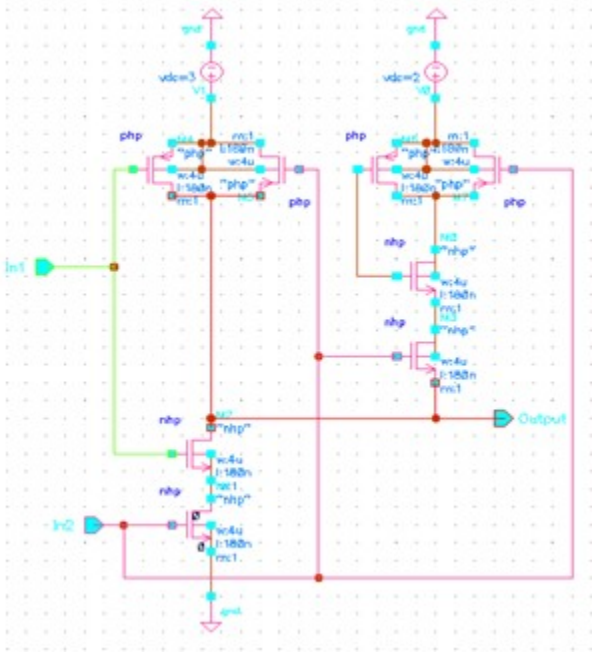
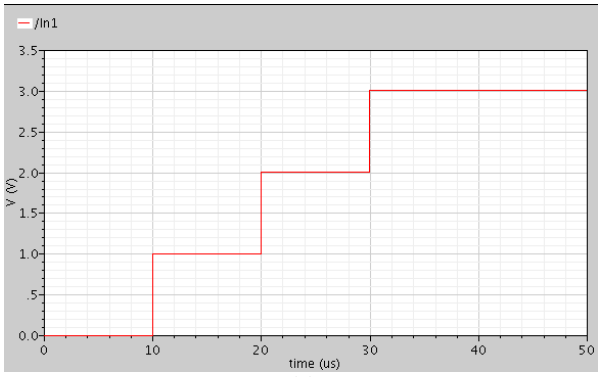
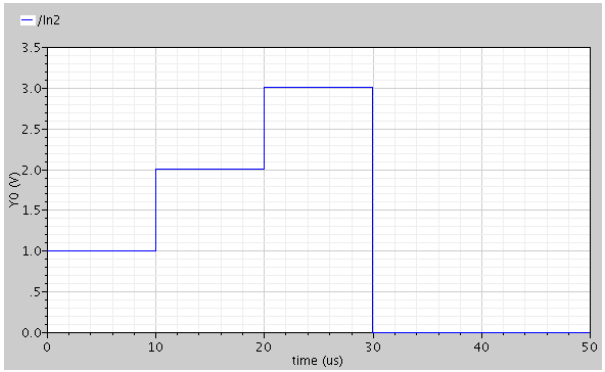


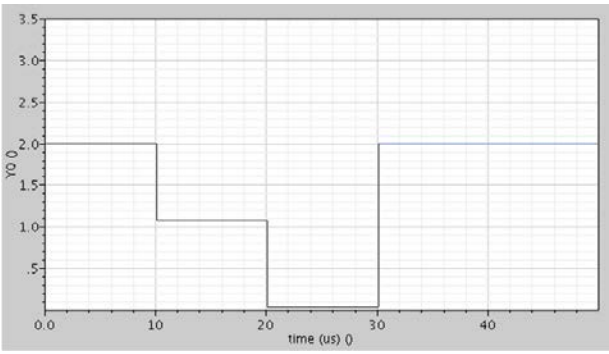
Figure 5.0: Ternary NAND (TNAND)



(a)



(b)



(c)

Figure 6.0: (a)Ternary Nand input 1. (b) Ternary Nand input 2. (c) Ternary Nand output simulation.

Based on the Ternary Nand output simulation on Figure 6.0, the first two graph represent the input of the Ternary Nand; for the first interval between 0 to 10us is 1 V thein it followed by second interval between 10.001us to 20 us as the input is 2 V. Then the last interval is between 20.001us to 30us, the input voltage is 3 The range for the transient response is 50us with the 10 us interval for each step.

These two inputs for the TNAND produced the output as highlighted in black line. The output generated is tabulated on the TNAND truth table in Table 2.0.

Table 2.0: Ternary NAND truth table

In 2	In 1	0	1	2
0		2	2	2
1		2	1	1
2		2	1	0

Based on the schematic shown in Figure 7.0, the Ternary Nor (TNOR) is the combination of NOR binary with two inputs and one output. the schematic is design based on the requirement which to reduce the number of interconnections.

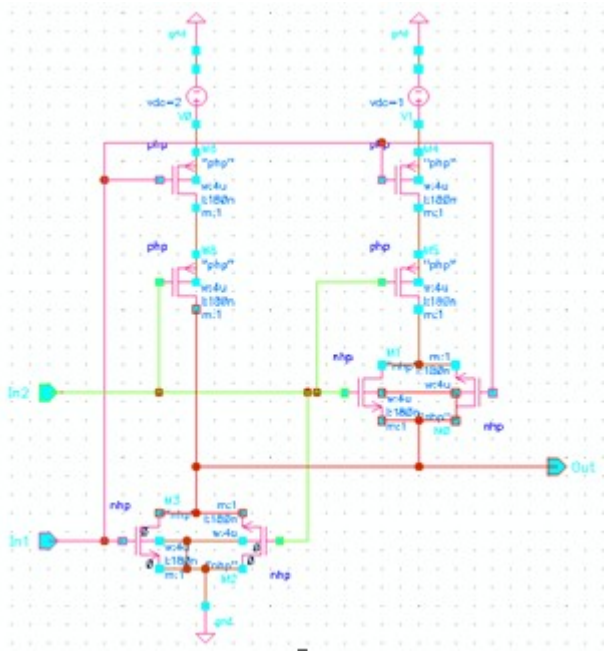
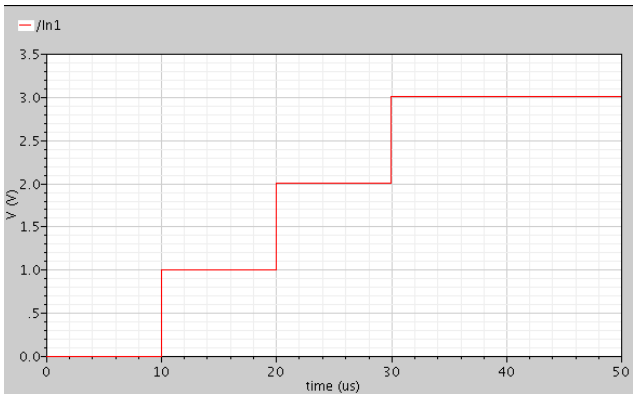
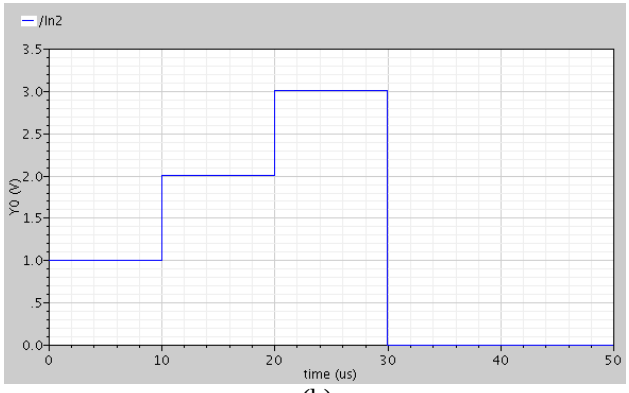


Figure 7.0: Ternary NOR

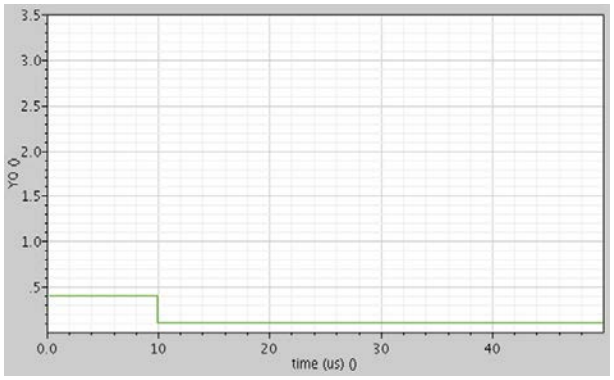
Next, the output produced from the schematic is stated in Figure 8.0. Based on the Figure 8.0, the first two graph in red line represent the input of TNOR; for the first interval between 0 to 10us the input is 1 V then it followed by the second interval between 10.001us to 20us the input is 2 V. then, the last interval is between 20.001us to 30 us. The next time intervals are for transient time. Hence, the second input values are given range start from 0 V, 1 V and 2 V in the range between 50us in transient response with 10us interval for every threshold steps.



(a)



(b)



(c)

Figure 8.0: (a) Ternary Nor input 1. (b) Ternary Nor input 2. (c)Ternary Nor simulation output.

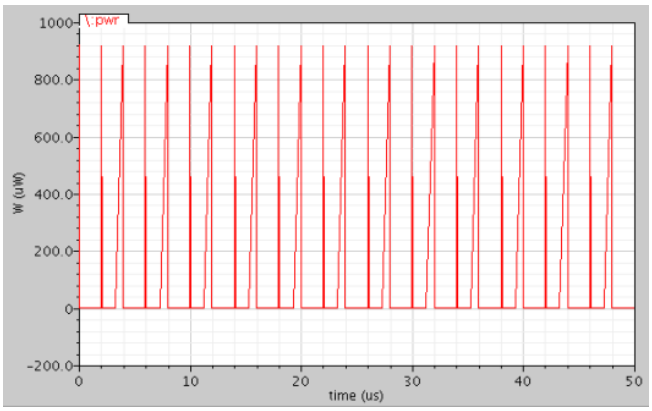
Based on the Figure 8.0, there are two input TNOR produces the output as highlighted on green line. The output generated is tabulated on the TNOR truth table in Table 3.0.

Table 3.0: Ternary Nor truth table

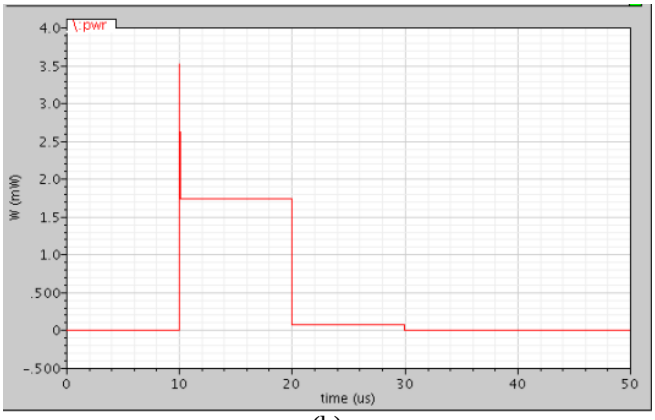
In 2 \ In 1	0	1	2
0	2	1	0
1	1	0	0
2	0	0	0

By referring to the Table 3.0, the first input, In1 is given 0 V and In2 is given 0 V the output produced is 2 V (high). Next, when In1 is given 1 V and In2 is 1 V, the output produced is 0 V. For the last interval, input In1 is 2 V and In2 is 2 V, the output produced is 0 V.

As stated on Figure 9.0, both graph is the representation of the power consumption between Binary Inverter and Ternary Inverter.



(a)



(b)

Figure 9.0: (a) Binary Inverter power consumption. (b) Ternary Inverter power consumption.

The comparison power consumption between both schematic represented which the power consumption of the NOR Binary and Ternary NOR is 860uW and 3.5mW respectively. It shows that the Ternary Inverter consume more power than the Binary Inverter. Hence, in term of performance, Ternary perform better than the Binary configuration in term of amount of complexity and number of interconnection.

IV. Conclusion

In the nutshell, all the listed project objective which to design the standard cell of CMOS Ternary inverter, Ternary Nand and Ternary Nor was successful and all the desired output produced is stated and tabulated. All the simulation process is design using the EDA tools which is Cadence 180nm Silterra process technology. Comparison on the power consumption analysis between Binary and Ternary design has been made, it shows that the Ternary standard cell consumes more power to produce the output than in Binary. Hence, Ternary can load more data in one time than the Binary which signed that there is trade-off between power and the complexity ofinterconnections.

V. Recommendations

Based on this project study, it is recommended that by using a Ternary schematic design cell which is Ternary inverter, NAND and NOR will reduce the interconnections and complexity of the circuit. However, as the elements in the MVL is increased, the process of fabricating the circuit also increase as the increase in the complexity. Next, it is recommended that Ternary standard cell should be used in developing technology such as Switch Box and other FPGA applications. As the technology keep in advancing, continuous and dedicated study on other application of Ternary can play major role and difference in the future technology.

References

[1] M. Mukaidono, "Regular ternary logic functions-Ternary logic functions suitable for treating ambiguity," Vols. vol. C-35, no. no. 2, pp. pp. 179-183, Feb. 1986.

[2] P. Saidutt, V. Srinivas, P. Phaneendra and N. Muthukrishnan, "Design of encoder for ternary logic circuits," 2012.

[3] P. P. Savitri Vanjol, "Design of Low Power CMOS Ternary Logic Gates," *IOSR Journal of Electronics and Communication Engneering,* pp. 55-59.

[4] X. a. P. F. Wu, "Binary-Ternary mixed-valued counter.," *Proceeding of the ISMVL,* pp. 53-60, 1987.

[5] A. a. A. B. Glass, "Design and Modeling of H-Ternary Line Encoder for Digital Tranmission," pp. 503-507, 2001.

[6] Ion Profeanu, ―A Ternary Arithmetic and Logic‖, ISBN: 978-988-17012-9-9, ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online); Proceedings of the World Congress on Engineering 2010 Vol. I , WCE 2010, June 30 - July 2, 2010, London, U.K.

[7] X.W.Wu, ―CMOS ternary logic circuits‖, IEEE PROCEEDINGS, Vol. 137, Pt. G, No. I, February 1990

[8] Xiaoqiang Shou, Nader Kalantari, Michael M. Green, ―Design of CMOS Ternary Latches‖,IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 53, NO. 12, December 2006.

[9] Kanchan S. Gorde, ―Design and simulation of ternary logic based arithmetic circuits‖ issue 2, vol-1, april-june 2010.