Modified GDI based time to digital converter

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Abstract— There are many ways to utilizes the solar power for different purpose. Here we need to use this solar power for smart nodes of internet of things (IOT) networks. This process will be designed with the MPPT techniques and it will be working by the hill climbing method. This MPPT will capture through FSM with TDC circuit. This proposed FSM will run in 14 clock cycle. The TDC functional blocks process the 5MHz internal clock frequency with 0.09µm MGDI Technology. Through this innovative technology the power and the process can reduce from the actual quantity.

Keywords— TDC,GDI, MGDI.

I. Introduction

A VLSI technology is being developed over the years thereby enhancing the performance of chips in terms of three basic constraints viz. delay, power, area. Efficient styles such as CMOS, PTL, GDI(Gate Diffusion Input) techniques are used to design VLSI circuits. The GDI cell contains three inputs:G(common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). This technique allows the use of a simple and efficient design algorithm, based on the Shannon expansion. Due to static power dissipation the output voltage reduced by two from the input voltage [6]. Various logic gates of GDI cell for different input configurations is given table I.

TABLE I. GDI Configuration of Logic Gates

N	P	G	Output	Gates
0	1	A	A´	Inverter
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A´B+AC	MUX
B´	B	A	A´B+B´A	XOR

This proves to be an additional advantage of MGDI over CMOS, PTL and GDI. Modified GDI circuits were implemented in regular GDI processes. The drawback of GDI has modified by connection of nMOS and pMOS substrate [1] is shown in figure1. The circuits using MGDI has less amount of power dissipation, transistor count and propagation delay as compared to pass transistor and transmission gate.

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Similarly, this technique can also be extended to complex circuits for their minimum power dissipation.The MOD-GDI technique is adopted from the basic GDI technique [7].This technique is a new technique which used to design the low power digital circuits. The MOD-GDI technique is mainly used to reduce the total power dissipation, propagation delay and also the transistor count. All these parameters are also achieved using GDI technique but due to some limitations of GDI technique like additional circuitry in order to give the inputs to the GDI circuits and difficulty in fabrication process.

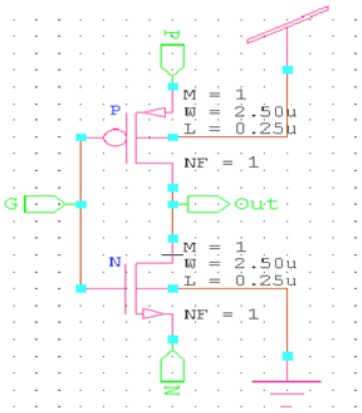

Fig. 1. Basic MGDI cell

The basic structure of MOD-GDI cell which is similar to the basic GDI cell, both the designs consists of three input terminals namely G, P and N. In GDI both the substrates of the PMOS and NMOS are connected to the source where as in the MOD-GDI the substrate of PMOS is connected to VDD and substrate of the NMOS is connected to the GND. Most of the complex circuits can be replaced with less transistor count, keeping the functionality and the output swing constant. It reaches the full swing output voltage. Method which helps to reduce the transistors count in table II, power and the time duration for input and output propagations [1]. In CMOS logic gates are implemented using universal gates, GDI techniques less transistor count for all logic gates.

TABLE II. Transistor Count of Logic Gates

Logic Gates	Transistor Count		
	CMOS	*GDI*	*MGDI*
Inverter	2	2	2
AND	6	2	2

Logic Gates	Transistor Count		
	CMOS	*GDI*	*MGDI*
OR	6	2	2
NAND	4	4	4
NOR	4	4	4
XOR	14	6	6

II. PRELIMINARIES

A. D Latch

The latch circuit is implemented by using logic gates with MGDI Technology. The number of transistor gets reduced with this technique. It seems only 14 transistors using instead of 32.

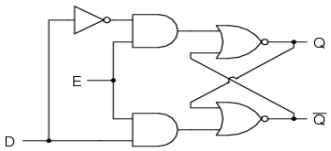

Fig. 2. D Latch Circuit

The figure 3 explains schematic diagram of modified GDI with 90 nm and the figure 4 explains AND gate module of latch.

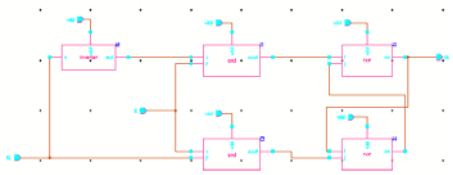

Fig. 3. Schematic Diagram of D Latch

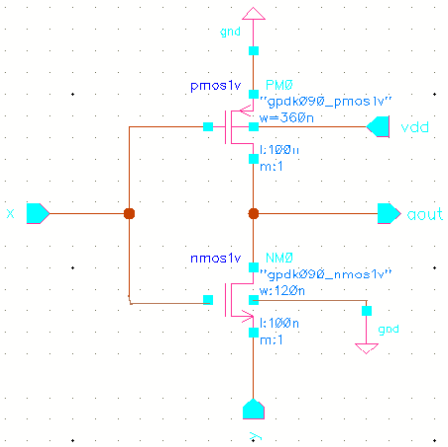

Fig. 4. Schematic Diagram Of AND Gate by Using MGDI

B. Delay Flip Flop

The D flip flop getting processed by 18 transistor in MGDI is given in the figure3.

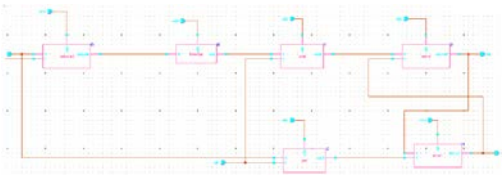

Fig. 5. Diagram of D Flip Flop

C. Two Bit magnitude Comparator:

This circuit helps to compare two magnitude bit and the comparator runs with 36 transistor of AND, OR gates. The draft figure shows 4 numbers of NOT gates,4 number of 3 input AND gate,2 number of 2 input AND gate,2 number of 4 input OR gate.

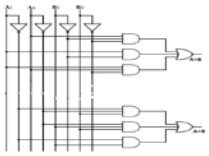

Fig. 6. Circuit Diagram of 2 bit magnitude comparator

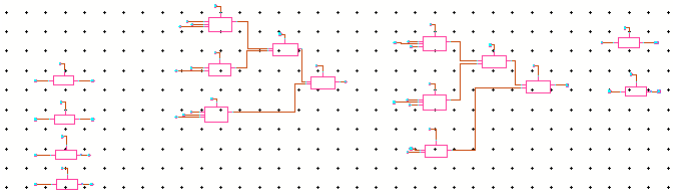

Fig. 7. Schematic diagram of 2 bit magnitude comparator

III. PROPOSED TDC FUNCTION BLOCKS

The Finite state machine with Time to Digital Conversion function used in Photovoltaic power harvesting system. Previously the CMOS 180 nm used for the TDC function and now the proposed MGDI technique in 90 nm is used for implementing the 6 bit ripple counter, 6 bit latch, 6 bit comparator and 4 bit decoder.

A. Six Bit Ripple Counter

The six bit ripple counter designed with six D flip flop in MGDI technique through 108 transistors. The counter value based on the 5MHz clock frequency.

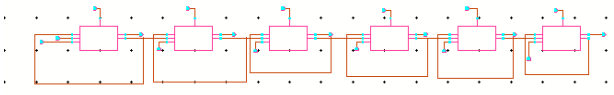

Fig. 8. Schematic diagram of six bit ripple counter

B. *Six Bit Latch:*

Symbol and schematic diagram of 6 bit latch designed by D latch explained in Figure A and B. It consumes 84 transistors for this module.

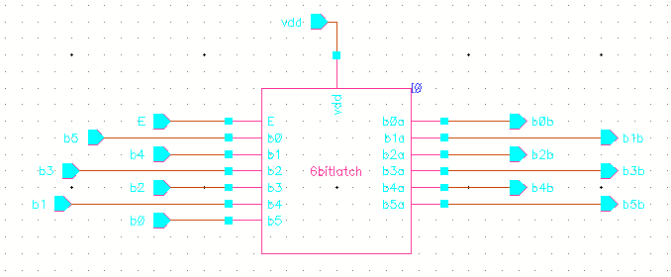

Fig. 9. Symbol of 6 bit latch

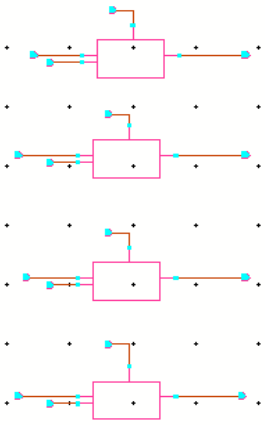

Fig. 10. Schematic diagram of 6 bit latch.

C. *Six bit Comparator*

It compares the six magnitude bit by using five numbers of 2 bit magnitude comparator. The transistor count scale down 180 followed by this techniques.

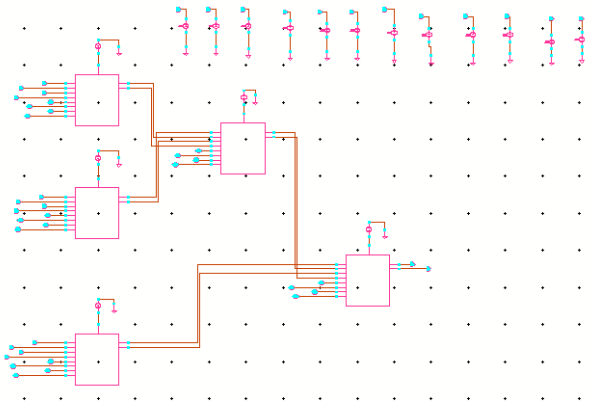

Fig. 11. Schematic diagram of six bit comparator.

D. *Decoder*

Decode the four bit counter value based on the NOT, AND gates. Using these technology 104 transistors is present.

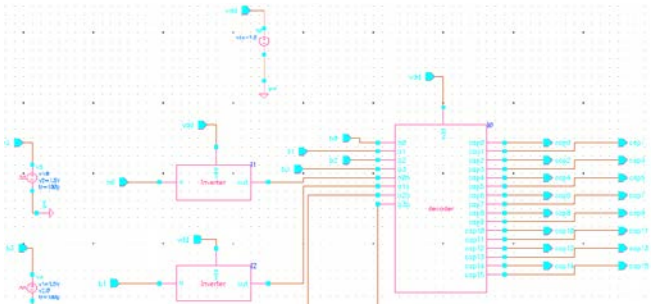

Fig. 12. Symbol of decoder circuit.

IV. RESULTS AND PROPAGATION DELAY

Major part of time to digital conversion and comparison function blocks are implemented in cadence tool using 90nm MGDI method.

A. *A Six Bit Ripple Counter*

The clock inputs given to 6-bit ripple counter. Clock frequency of this design is 5MHz. The outputs obtained at b[0:5] is given in figure 13, frequencies are divided into input frequency. The transient and DC response is analyzed using cadence 90nm tool. The propagation delay through clock to output port is 71.18ns.

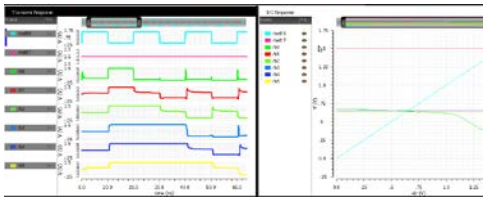

Fig. 13. Output waveform of 6-Bit Ripple Counter.

B. *A Six Bit Latch*

Based on 'E' enable control signal the inputs b[0:5] propagate to the output b[0b:5b]. In figure 14 analyze transient and DC response with 10.1ns delay.

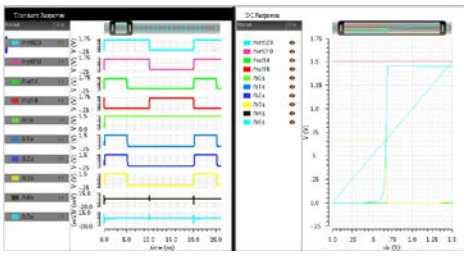

Fig. 14. Output Waveform of Six Bit Latch.

C. A Six Bit comparator

The inputs b[0x:5x] and b[0y:5y] compared under this techniques is given in figure 15. The transient and DC response of outputs 'G' greater than and 'L' less than is present in figure 16. The delay value is calculated from input to output is 315.3ns.

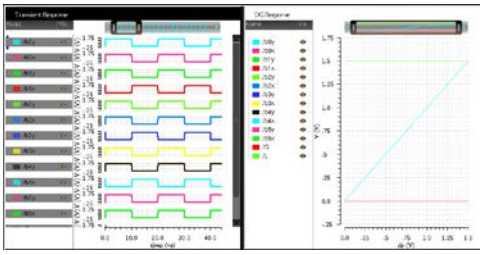

Fig. 15. Output waveform of 6 Bit Comparator inputs.

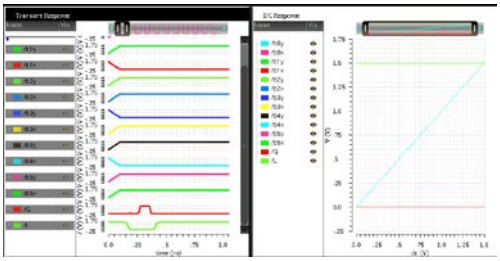

Fig. 16. Output waveform of 6 Bit Comparator outputs.

D. A Decoder

Figure 17 draft the inputs b[0:5], output cap[0:7] value and cap[8:15] is in figure 18. Time delay of 80.89ns is calculated the transient and DC response of decoder circuits.

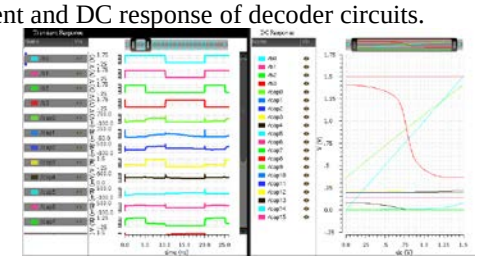

Fig. 17. Output waveform of Decoder input and lower byte output.

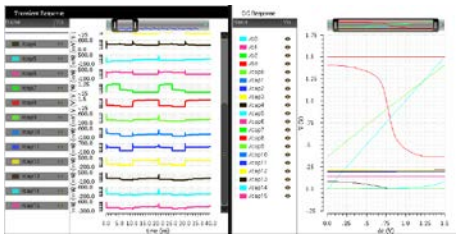

Fig. 18. Output waveform of Decoder higher byte output.

V. CONCLUSION

An extensive performance analysis of modified primitive cells of AND, OR gate, D latch D flip-flop and 2bit comparator has been presented. Using these cell module designed TDC blocks. The performance of these MGDI was analyzed in terms of transistor count, delay and power and it is compared with conventional GDI and CMOS logic. The simulation results reveal better delay performance of proposed blocks cells as compared to existing GDI cell and CMOS at 180nm technologies. Overall the simulation results and delay shows the MGDI TDC topologies have least delay, low power consumption and less transistor count.

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