A Simple BJT Based Circuit for Generating Chaotic Oscillations and Double-Scroll Attractors

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Abstract – **A simple BJT based circuit for generating chaotic waveforms is proposed in this paper. The simple circuit consisting of two BJTs, two diodes, nine resistors, two capacitors and an inductor, is based on Chua's circuit. The circuit is observed to exhibit the chaotic Double-Scroll attractor pattern as well as non-periodic oscillating current and voltage waveforms during SPICE simulations. The working of the circuit is analyzed and mathematical formalisms are developed to explain the chaotic phenomena so observed. It is seen that the chaotic waveforms are generated as a result of a nonlinear relationship between the current through the inductor and the voltages across the capacitors. These are mathematically modeled as a system of nonlinear differential equations and are presented in the paper along with the observations obtained.**

I. Introduction

Since L.O. Chua's defining work on chaotic circuits [1], a lot of research has gone into the study of chaotic circuits and nonlinear analog systems. A number of different circuits have been designed based on Chua's chaotic circuit and a multitude of variations of the same have also received considerable interest [2,3,4,5].

Chua's circuit exhibits chaotic waveforms, which can be understood as oscillating waveforms with no fixed time period. The circuit, along with two capacitors, an inductor and a resistor, also possesses a negative nonlinear resistance called Chua's diode. Therefore, devising new variations of the circuit comprising Chua's diode can lead to the development of new, simple and improved chaos generating circuits. For this very reason, Chua's circuit paves the way for a study of chaotic systems that essentially possess nonlinear circuit dynamics.

Moreover, recently, advances in the field of chaotic cryptography and encryption [6-12] have led to the investigation and application of various Double-Scroll chaotic oscillator circuits as random number generators (*RNGs*). Most of these continuous time chaotic systems are employed because they have the ability to generate truly random sequences of numbers and produce strong unbreakable keys. It has been found that even if the design of the chaotic crypto-system is known, it is virtually impossible to predict its output. Even more recently, memristor based chaotic circuit designs are being utilized to enhance the application of chaos in cryptography [13,14]. Therefore, it is imperative to design chaotic circuits that can suit the needs of a variety of applications.

In this paper, a new BJT based design is presented that is simple and robust in both design and use. The nonlinear negative resistance (or Chua's diode) is designed using two BJTs, two diodes and resistances. The subsequent sections detail the circuit diagrams of Chua's circuit as well as the proposed BJT based design.

II. Basic Design of Chua's Circuit

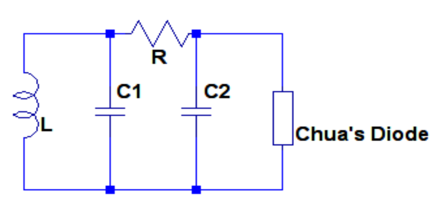

Fig. 1 Chua's chaotic circuit

As can be seen in Fig. 1, Chua's circuit must contain three or greater energy storing circuit elements. In this case, they are the capacitors and the inductor. It can also be seen through the circuit that there is a requirement of at least one nonlinear circuit element, known here as the Chua diode. One variation of Chua's circuit given in [5], when analyzed by writing down the appropriate current and voltage equations, consists of a system of nonlinear differential equations. In fact, the nonlinearity of the equations is the reason that the circuit is able to generate chaos. The equations are as follows –

$$\frac{dV_{C2}}{dt} = k(V_{C1} - V_{C2} - x(V_{C2})) \qquad (1)$$

$$\frac{dV_{C1}}{dt} = \frac{(V_{C2} - V_{C1} + Ri_L)}{RC_1} \qquad (2)$$

$$\frac{di_L}{dt} = m(-V_{C1}) \qquad (3)$$

Here, V_{C1} and V_{C2} are the voltages across the capacitors; i_L is the current flowing through the inductor and k, m and $x(V_{C2})$ are obtained by solving the circuit making up the nonlinear resistance. $x(V_{C2})$ is the piece-wise segmented function due to which the nonlinearity arises in the equations.

Thus, when designing a new circuit based on the one given in Fig. 1, it is essential that after applying Kirchhoff's laws and analyzing the circuit, we get nonlinear relationships between the inductor current and capacitor voltages as in equations (1), (2) and (3).

Moreover, the time response of all three parameters – the two voltages and the current, should give chaotically oscillating waveforms as outputs. The work at hand revolves around designing an appropriate circuit that can simulate Chua's diode. With these developments as a basis for analysis, we design the BJT based circuit shown in the next section.

III. Proposed BJT Based Chaotic Circuit

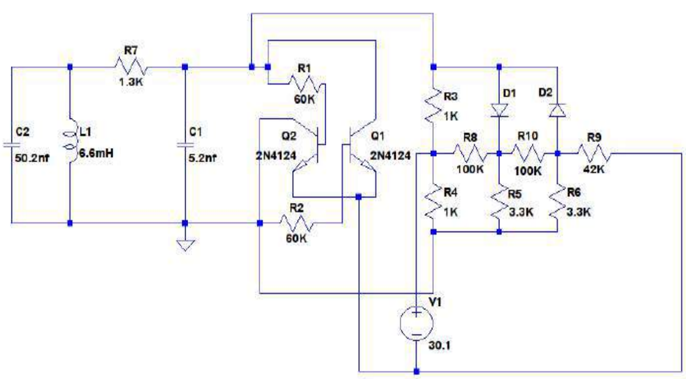

Fig. 2 Proposed chaotic circuit

The proposed circuit is shown in Fig. 2. The left hand side of the circuit, comprising of the capacitors, the resistor and the inductor is similar to that shown in Fig. 1. The circuit for the nonlinear resistive part has been replaced with a circuit comprising of two BJTs, two diodes, a number of resistors and a voltage source. The nonlinear part of the circuit is expanded and shown in Fig 3. The values chosen for the circuit elements are as such –

- Resistors: R1 = 60KΩ, R2 = 60KΩ, R3 = 1KΩ, R4 = 1KΩ, R5 = 3.3KΩ, R6 = 3.3KΩ, R7 = 1.3KΩ, R8 = 100KΩ, R9 = 42KΩ, R10 = 100KΩ.
- Capacitors: C1 = 5.2nF, C2 = 50.2nF
- Inductor: L1 = 6.6mH
- Diodes: D1 and D2 are model MURS120 manufactured by OnSemi.
- Transistors: Q1 and Q2 are model 2N4124 manufactured by Fairchild.
- Voltage source: V1 = 30.1V

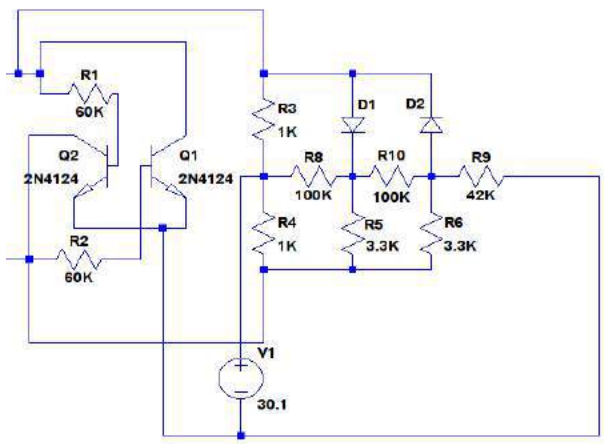

Fig. 3 The nonlinear resistive part of the proposed chaotic circuit

Fig. 3 is then analyzed mathematically using circuit analysis and it is observed that the given circuit can also be modeled by a set of nonlinear differential equations, just like Chua's circuit. The equations that are described below, confirm that the circuit in Fig. 2 does behave like a chaotic circuit. Moreover, by observing the nonlinear part of the equations we derive, we can hypothesize about the graphical nature of the relationship between the current and voltages. All these mathematically derived results are later confirmed by simulating the circuit in SPICE and observing the plots and waveforms obtained.

The equations derived from the circuit are as follows –

$$\frac{dV_1}{dt} = \frac{V_2 - V_1}{RC_1} - \frac{f(V_1)}{C_1} \qquad (4)$$

$$\frac{dV_2}{dt} = \frac{V_2 - V_1}{RC_2} + \frac{I_L}{C_2} \qquad (5)$$

$$\frac{dI_L}{dt} = \frac{-V_2}{L} \qquad (6)$$

where V_1 is the voltage across capacitor C1, V_2 is the voltage across capacitor C2, I_L is the current through inductor, C_1 is the capacitance of capacitor C1, C_2 is the capacitance of capacitor C2, R is the resistance of resistor R7 and L is the inductance of inductor L1 in the circuit of Fig. 2.

It can be seen clearly that the equations (4), (5), (6) are similar mathematically to equations (1), (2), (3). This implies that the circuit will generate chaos if the function of voltage V_1, $f(V_1)$ is nonlinear in nature in equation (4). It is found that $f(V_1)$ is actually a three-segment piece-wise nonlinear function. Mathematically it is of the type,

$$f(V_1) = \begin{cases} \alpha(V_1 - 1) + \beta, \ V_1 \geq 1 \\ \beta V_1, \ -1 \leq V_1 \leq 1 \\ \alpha(V_1 + 1) - \beta, \ V_1 \leq -1 \end{cases} \tag{7}$$

where α and β are constant values computed from solving the nonlinear resistive circuit.

The definition of $f(V_1)$, which lends nonlinearity to equations (4), (5) and (6) is also the reason that the Double-Scroll attractor pattern is observed in the output waveforms. Thus, we have been able to confirm mathematically that the circuit of Fig. 2 is in fact a Double-Scroll chaotic oscillator. The results confirming these mathematical developments are given in the next section.

IV. Simulations And Results

The circuit of Fig. 2 is simulated in SPICE and then output waveforms are generated. Firstly, plots of V_1 and V_2 with respect to time are plotted. In these, I_L is also plotted alongside V_1 and V_2 for a general idea of the nature of the waveforms obtained. These are shown in Fig. 4 and Fig. 5.

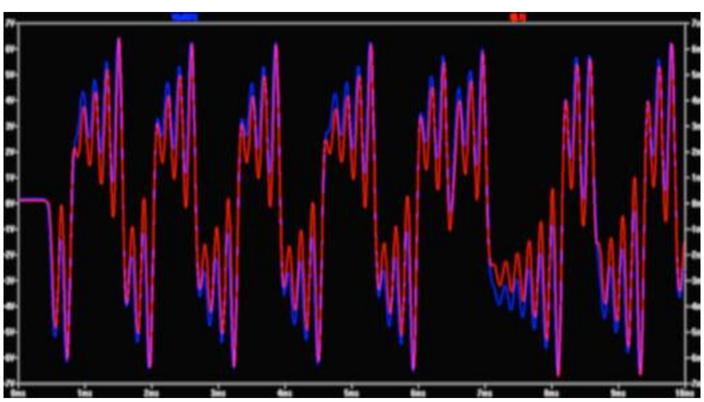

Fig. 4 Transient response of V_1 (in blue) and I_L (in red) obtained

The output waveforms obtained in Fig. 4 can be observed to be chaotic in nature. They are adjudged as chaotic oscillations because they are oscillating but without ever repeating. That is, they oscillate but without any fixed time period. Both V_1 and I_L are confirmed to be chaotically oscillating waveforms.

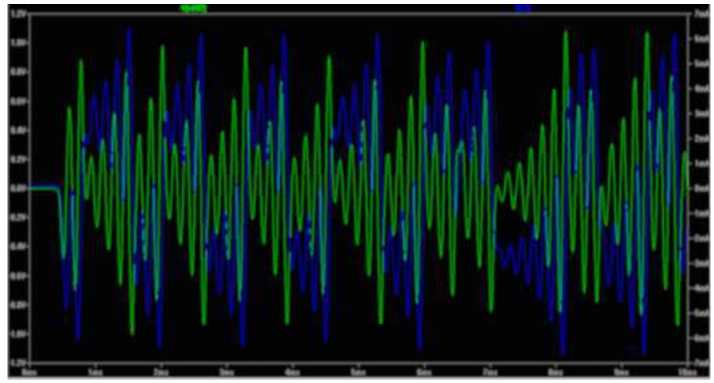

Fig. 5 Transient response of V_2 (in green) and I_L (in blue) obtained

Also it is seen in Fig. 5, that the waveform of V_2 is also chaotically oscillating. Thus, the mathematical formalism of the previous section has been experimentally verified.

Moreover, the chaotic Double-Scroll attractor can also be obtained by plotting either voltage V_1 or voltage V_2 on the y axis and the current flowing through the inductor, I_L on the x axis. The waveforms so obtained are plotted together and are shown in Fig. 6 below.

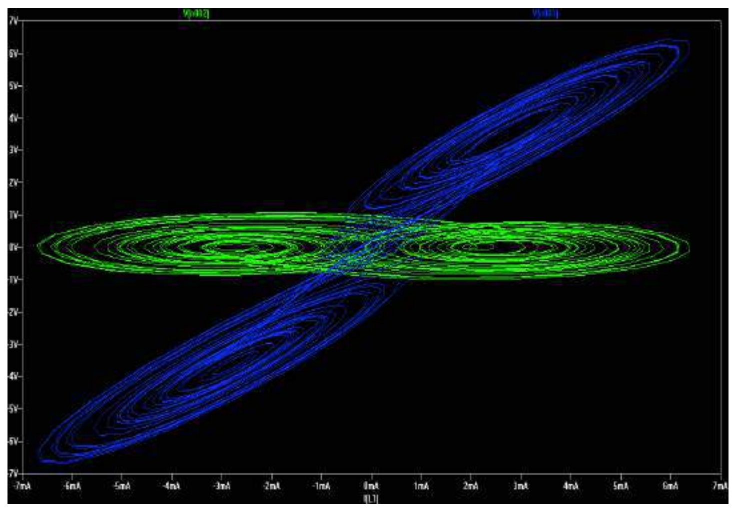

Fig. 6 The Double-Scroll attractor pattern obtained by plotting V_2 (in green) and V_1 (in blue) with respect to I_L

The circuit exhibits the Double-Scroll attractor shown in Fig. 6 because the nonlinear function of equation (7) is a three-segmented piece-wise function. As can be seen, both V_1 and V_2 when plotted with respect to I_L yield the attractor pattern.

V. Conclusion

In this paper we have presented the design of a simple BJT based chaotic circuit. We have developed the mathematical equations governing the functioning of the circuit taking

Chua's circuit as the basis. Along with mathematical analysis, the proposed circuit has also been simulated in SPICE and appropriate waveforms have been plotted. The circuit is observed to exhibit chaotically oscillating waveforms as well as chaotic Double-Scroll patterns. The working of the circuit has been both experimentally and theoretically proven and verified.

REFERENCES

[1] L. O.Chua, C.W. Wu, A.Huang, G. Q. Zhong, "A universal circuit for studying and generating chaos – Part I: routes to chaos", IEEE Trans. Circ. Syst.-I: Fund. Th. Appl, vol. 40, 1993, pp. 732–744.

[2] R. N. Madan, Chua's Circuit: A Paradigm for Chaos. World Scientific, Singapore, 1993.

[3] H. Nayfeh, B. Balachandran, Applied nonlinear dynamics: Analytical, Computational, and Experimental methods. Wiley, New York, 1995.

[4] M. Lakshmanan, K. Murali, Chaos in Nonlinear Oscillators: Controlling and Synchronization. World Scientific, Singapore, 1996.

[5] M.P. Kennedy, "Robust op amp realization of Chua's circuit", Frequenz, vol. 46, 1992, pp. 66–80.

[6] Gao Tie-gang, Chen Zeng-qiang, "A New Image Encryption Algorithm Based On Hyper-chaos," Science Direct Physics Letters A, vol372, pp. 394-400, 2008.

[7] Liu Hong-jun, Wang Xing-yuan, "Color Image Encryption Based On One-time Keys And Robust Chaotic Maps," Computers and Mathematics with Applications, vol59, pp. 3320-3327, 2010.

[8] Seyed Mohammad Seyedzadeh, Sattar Mirzakuchaki, "A Fast Color Image Encryption Algorithm Based On Coupled Two-dimensional Piecewise Chaotic Map," Signal Processing, vol92, pp. 1202–1215, 2012.

[9] Wang Jing, Jiang Guo-ping, "Cryptanalysis of a Hyper-chaotic Image Encryption Algorithm And Its Improved Version," Acta Phys, Sin, vol60, pp. 060503(1)-060503(11), 2011.

[10]Li Tai-yong, Jia Hua-ding, Wu Jiang, "Study On Digital Image Encryption Algorithm Based On 3D Chaotic Sequences," Computer Applications, vol26, pp. 1652-1654, 2006.

[11]Wei Peng-cheng, "Studies on the Design and Implementation of Chaotic Stream Ciphers," Master Dissertation of Chongqing University, 2004, pp. 30-48.

[12]Liu Cheng-bin, "Study And Implementation of the Chaotic Encryption Algorithm.," Master Dissertation of Beijing University of Posts and Telecommunications, 2008, pp. 28-37.

[13]C. Yang, Q. Hu, Y. Yu, R. Zhang, Y. Yao and J. Cai, "Memristor-Based Chaotic Circuit for Text/Image Encryption and Decryption," 2015 8th International Symposium on Computational Intelligence and Design (ISCID), Hangzhou, 2015, pp. 447-450.

[14]F. Corinto, O. V. Krulikovskyi and S. D. Haliuk, "Memristor-based chaotic circuit for pseudo-random sequence generators," 2016 18th Mediterranean Electrotechnical Conference (MELECON), Lemesos, 2016, pp. 1-3.