Design of Differential 130nm CMOS Low Noise Amplifier

M. Muhamad, N. A. A M. Ali

***Abstract*—This paper presents a Differential Low Noise Amplifier (LNA) circuit design using 0.13um RFCMOS technology. The LNA operating at 2.4 GHz frequency band. A good quality of LNA should has noise figure (NF) that low, high gain, wide band width and low power consumption. The differential Low Noise Amplifier proposed provide high gain, low noise and it provide large superior out of band IIP3. A cascade output stage was added in the differential LNA to the Single-ended source degenerated source. At the drain of the main transistor, an inductor is added to reduce the noise contribution of cascode transistor. In a Differential cascode LNA, at the gate of the cascode transistor another inductor is connected to reduce the noise and to increase the gain of the cascode transistor. Besides that, the power gain of the LNA can be increase and reduce power consumption.**

Keywords*— *Low Noise Amplifier (LNA), Noise Figure (NF), Radio Frequency Complementary Metal-Oxide (RFCMOS)

I. INTRODUCTION

Nowadays the wireless communication demand is increasing day by day due to the development of technology. A wireless system comprise of a back-end and front-end section. Analog signal is being process in the front-end section in the high radio frequency. While analog and digital signal is processed at the back-end section in baseband of low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications [1]. Typically the frequency lies from 100 KHz to 100 GHz. In general baseband frequency is frequency that below 1 GHz while those bigger than 1GHz describes as RF. The mainstay of radio frequency communication receiver is the Low Noise Amplifier (LNA). Low noise amplifier (LNA) which is in the RF front-end circuit has the great value in this field [2-4]..It main purpose is to provide gain while preserving the input signal-to-noise ratio of the output which is important characteristic because the receiver signals usually weak and can be the presence of a great amount of interface[5]. Besides that, the characteristic of good LNA is shown in Figure 1.

The authors are with the Faculty of Electrical Engineering, Universiti Teknologi Mara, Shah Alam, Selangor, Malaysia
aina_adibah05@yahoo.com

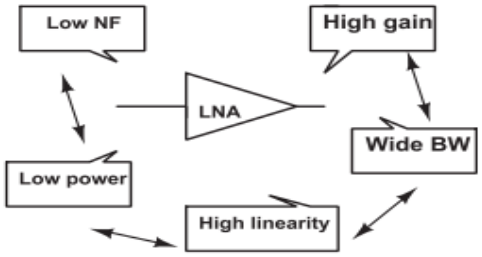

Figure 1: Characteristic of LNA.

This paper present a design of 2.4 GHz RFMOS Differential LNA which is used to improve performance of Differential LNA. The aim of this paper is to provide Differential LNA that have low power consumption but still have acceptable performance of noise, linearity that acceptable and high range of dynamic.

II. METHODOLOGY

A. *Differential LNA Topology*

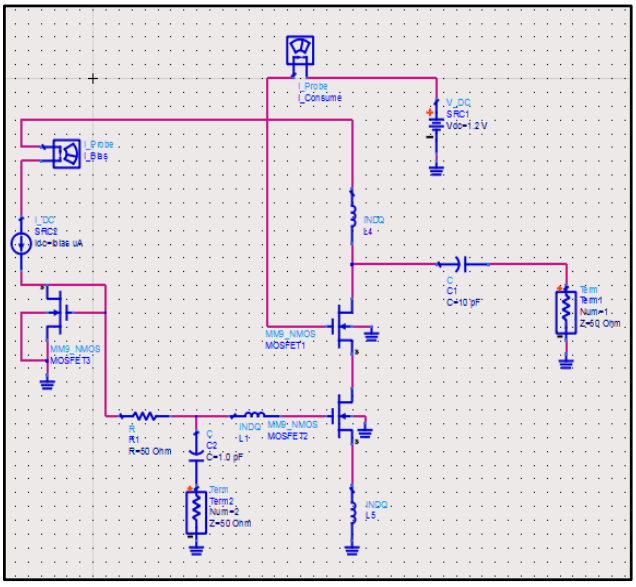

Figure 2: Schematic circuit of single ended Low Noise Amplifier

In Figure 2 above, it shows the schematic circuit of a single source–inductor–feedback amplifier for input impedance matching with the gate inductor. In order to gain simultaneous input and noise matching, the source inductor

is used. The value of desired input resistance is 50 Ohm. Structure of cascode is a combination of a common-gate load and it effect the increasing of output impedance. Device of additional cascode has a diode .The inductor between the cascode source and supply blocks any RF is leaking to the supply rail and maybe varied in value to optimize the gain response of the LNA. Figure 2 represents a half of final differential DLNA. By using the inductive Degeneration Ls the topology is matched to 50 Ω. The parameter is often expressed by S11. LNA input impedance expression is defined in (1)

$$Zin(s) = Lps \parallel (LGS + LsS + \frac{1}{Cts} + \frac{gm1Ls}{Ct}) \quad (1)$$

The Zin should be 50 Ω to achieve input matching, so

$$Zin = gm/CgsLs \quad (2)$$

In most LNA design the value of Ls was assumed and the values of gm and Cgs are calculated based on the formula to find the required for Zin [6]

Degeneration Inductor, Ls

$$\omega T \cong \frac{gm}{Cgs} = \frac{Rs}{Ls} \quad (3)$$

Where ωT is defined as a cut-off frequency. The value of the Rs is 50 Ω [7]

Optical Q of Inductor

$$QL = \sqrt{1 + (\frac{1}{\rho})} \quad (4)$$

Where $\rho = \frac{\sigma.\alpha^2}{5.\gamma}$

For parameter p usually depend on the RFCMOS technology, but typically γ is set between 2-3, σ is set to 2-3 times the value of Y and the α assumed to be 0.8-1[7]

Evaluation of Lg

$$Lg = \frac{QL.Rs}{\omega o} . Ls \quad (5)$$

Gate source capacitance

$$Cgs = \frac{1}{\omega o^2 (Lg+Ls)} \quad (6)$$

Width of transmitter

$$Cgs = \frac{2}{3} Cox.W.Lmin \quad (7)$$

$$W = \frac{3}{2} \frac{Cgs}{2Cox.Lmin} \quad (8)$$

$$\varepsilon ox = \varepsilon ox. \varepsilon o \quad (9)$$

Where

εo = dielectric constant for free space 8.854E^-14 F/cm

εox= dielectric constant for silicon 3.9 [7]

Estimate optimum noise figure

$$NFOpt = 1 + \frac{2\gamma}{\alpha} (\frac{\omega o}{\omega T}) \sqrt{p} \ (|c| + \sqrt{p} + \sqrt{1+p}) \quad (10)$$

B. Differential LNA Circuit Design

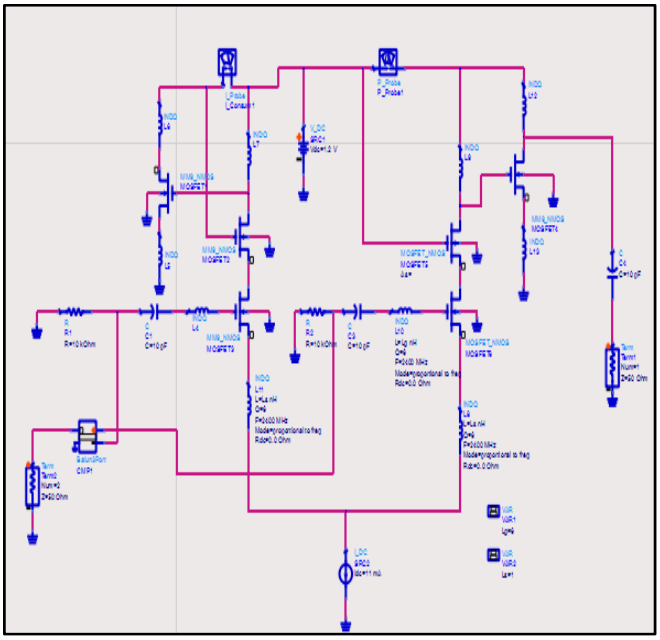

Figure 3: Schematic circuit of Differential LNA

The differential of LNA schematic circuit is shown in Figure 3. Many advantages can be gain by the differential LNA over single ended LNA. A stable reference point is offer by the DLNA compared to the single ended. Second, the noise in the circuit can be reduced by using the Differential LNA. The composite signal swing of the differential signal can be twice that of the single ended swing on the same power supply, increasing the signal-to-noise ratio. The amplifier alternatively can be increased on the same power supply, distortion will be low, or a low power supply voltage can be used in order to provide same signal swing and lowering the power dissipation. Besides that, an image rejection scheme and the use of Gilbert mixers are required to be fed from a differential source.

The signal of the differential amplification ensure an attenuation of the common mode signal which is in the most system the common mode signal will be noise. The virtual ground formed at the tail removes the sensitivity to parasitic ground inductances which makes the real part of the input impedance purely controlled by Ls [8]. The balun transformer (CMP1) supply the differential input voltage in the circuit. The balun (a contraction of balanced-unbalanced) is a two-port component placed between a source and load when a differential, balanced RF functional block must connect to a single-ended, ground-referenced one [9]. While at the tail of this stage the ideal current source is added. Source impedance of an ideal current source is an infinite.

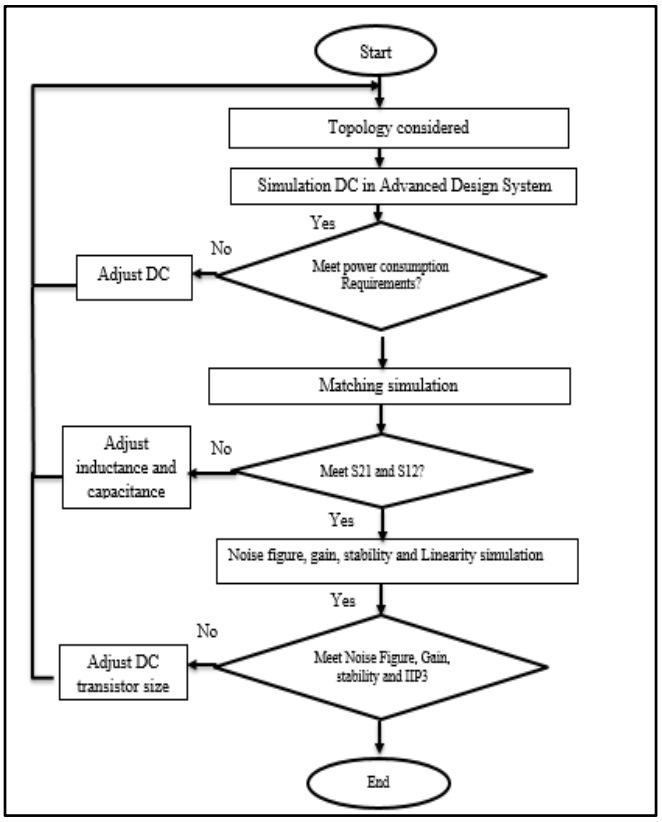

Figure 4: The flow chart of simulation using Advanced Design System

III. SIMULATION RESULT

The DLNA is simulated using ADS 2016 software using 0.13 um technology of CMOS process. The DLNA is operated with 1.2 V supply. The maximum gain that the differential amplifier provides is 23.465 dB at 2.4 GHz frequency band as shown in Figure 5.

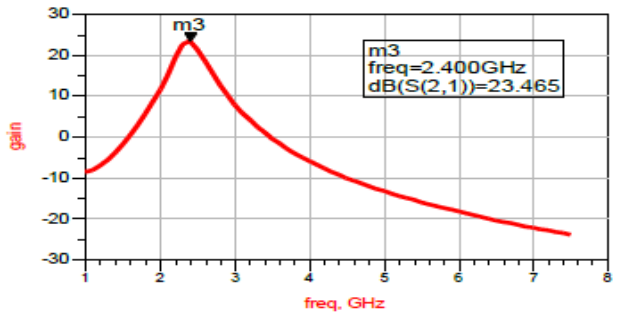

Figure 5: Simulation result of gain characteristic (S21)

From the Figure 6 below, the simulation of DLNA using ADS software show the input matching, S11 gained versus frequency is -11.186 dB.

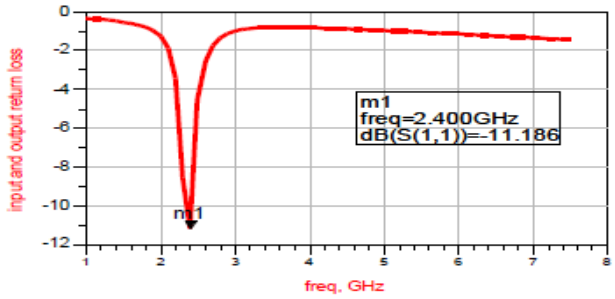

Figure 6: Simulation characteristic of input matching (S11)

From the Figure 7 below, the simulation of DLNA using ADS software show the output macthing S22 gained is -9.492 dB.

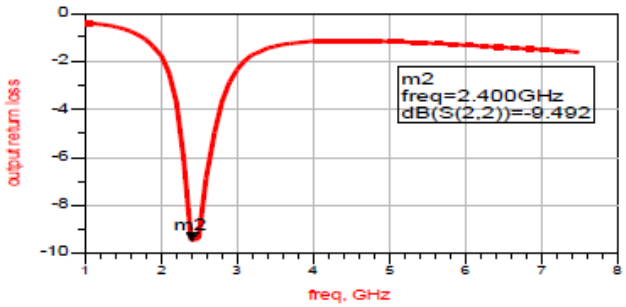

Figure 7: Simulation characteristic of output matching (S22)

From the Figure 8 below, the simulation of DLNA using ADS software show the reverse isolation S12 gained is -39.715 dB.

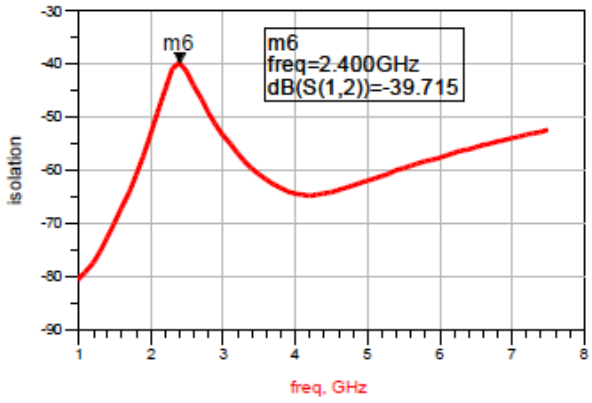

Figure 8: Simulation result of characteristics of reverse isolation (S12)

From Figure 9, the stability figure K that been achieved in the circuit is 2.667 at frequency 2.4 GHz. According to the meaning of the stability figure

$$K = \frac{1-|S11|^2-|S22|^2+|\Delta|}{2|S22S12|} \quad (11)$$

$$\Delta = S11S22 - S12S21 \quad (12)$$

Circuit is stable unconditionally when K>1 it means that Δ<1.

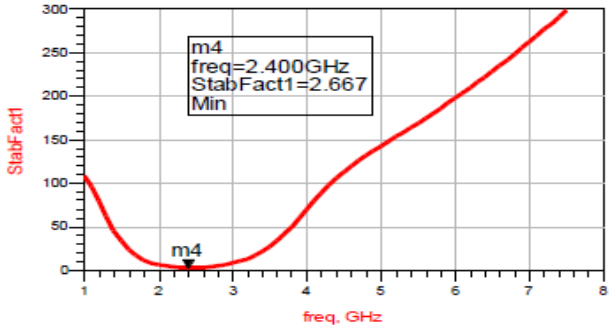

Figure 9: Simulation result of Stability figure K

From simulation result in Figure 10, the noise figure of DLNA in the proposed circuit is indicated by the red line while the minimum noise figure result is indicated by the blue line in the graph. At frequency 2.40 GHz the noise figure is low which 2.586 dB.

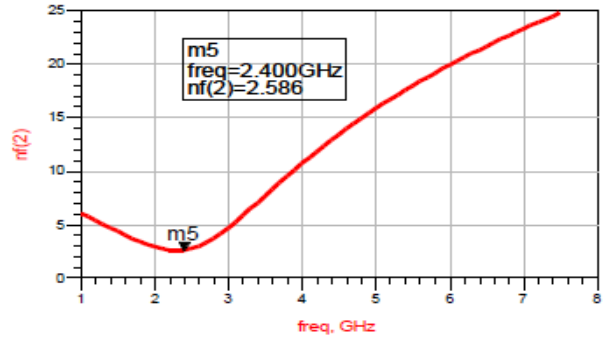

Figure 10: Simulation result of noise figure, NF.

Value of third order input intercept point IIP3 is calculated using following formula. It also using 1 dB compression slot. A measure of the linearity of the receiver is the 1 dB compression point and defined as input of RF power required to increase conversion loss by 1 dB from ideal. From Figure 11, input power versus gain plot has maximum gain is 23.46 dB which is 1 dB compress at - 20 dBm input power.

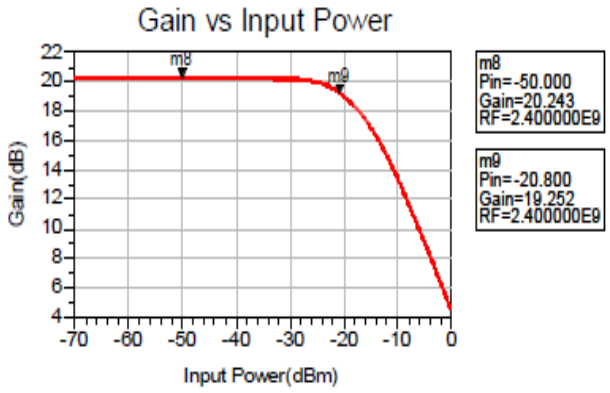

Figure 11: Simulation result of gain versus input power.

Based on Figure 12, it shows a graph of input power versus output power. It shows -1.051 dBm output power at -20 dBm input power. To estimate IIP3 use cubic power series approximation and analytic device which is typically 10 to 15 dB beyond 1 –dB compression point.

IIP3= P1dB + 10 to 15dBm

From the graph, value of P1=-1.051dBm, the minimum IIP3 calculated is 9.049dBm which show the device is linear and without third order distortion at 2.4 GHz.

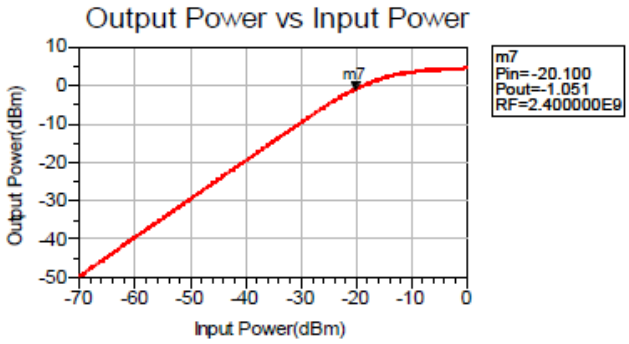

Figure 12: Simulation of output power versus input power.

From all the above result gained from the simulation, the circuit provide high gain, high stability, low noise figure and low IIP3. In Table 1, a comparison of the simulated LNA characteristic is included. From the comparison in Table 1, the proposed CMOS LNA in this paper is reported to have a best values among the other CMOS LNA while comparing the characteristic.

Table 1: Comparison table for LNA performance

Ref	Tech (µm)	Freq. GHz	Gain (dB)	NF (dB)	Power Consumption (mW)	S11 (dB)	IIP3 (dBm)
[10]	0.13	3.1-10.6	10.2	0.9-4.1	17.2	-	6.80
[11]	0.18	3.1-10.3	9.6	3.9	13.4	<-9	-3
[12]	0.13	3-5	9.5	3.5	16.5	<-10	-
[13]	0.13	0.1-2	7.6	4.15	3	<-10	0.5
[14]	0.18	0-1.4	16	3	12.8	<-10	<13
[15]	0.065	0.2-5.2	13-15.6	<3.5	21	<-14	0
This work	**0.13**	**2.4**	**23.465**	**2.59**	**3.24**	**<-11**	**9.05**

Table 2: LNA performance summary

No.	Parameters	Measured Value
1.	(S21) Gain	23.46 dB
2.	(S11) Input Matching	-11.18 dB
3.	(S22) Output matching	-9.49dB
4.	(S12) Reverse Isolation	-39.715dB
5.	Stability	2.66
6.	Noise Figure	2.60 dB
7.	IIP3	9.049
8.	Total Power Consumption	3.24mW
9.	Total DC Current	2.59mA

V. CONCLUSION

This paper present a simulation of 2.4 GHz CMOS DLNA using 0.13um technology. The simulation is being done using Advanced Design System (ADS) version 2016. The result show that the Differential LNA circuit achieves a gain power (S21) of 23.465 dB and it maximum noise figure (NF) of 2.586 dB from a supply of voltage 1.2V. While the consumption power of the Differential LNA proposed is 3.24 mW. All the result obtained meet the specifications of RFCMOS Differential LNA which is low NF, high gain performance, high stability and low consumption power.

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