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# A Novel Approach for Analysis CNTFET Based Domino circuit in Nano-Scale Design

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*Abstract:- As semiconductor industries is developing day by day to meet the requirement of today's world. As scaling of ICs day by day to introduce functionality of the device while fabrication more and more component which results in shorter the life of the battery operated device which has to be improved. Here in this article we have measured performance parameters like power consumption, UNG, Evaluation Delay, standby power and speed of various domino circuits provided for various inputs like 8 & 16 input OR gate. When we compared power, delay, and PDP of different topologies of domino circuit design with the simulation results which is performed by using SPICE tool at 32nm CNTFET process technology with supply voltage 0.9V and $27^0$ C of temperature at 100 MHz. All the simulation results is done in CMOS & CNTFET technology, it is observed that saving of average power upto 90.46% with same delay, with improvement of 5.8 × Noise-immunity with scaling of technology.*

*Key Words:- High Speed. MOS, CNTFET, Domino Logic,*

## 1. INTRODUCTION

Due to the increasing demand of functions in the portable devices such as smart phones laptops tablets etcetera, successive scaling is required according to moor's law, that is number of transistor will be double in every two year, that result in more number of transistor count that causes increased packing and cooling cost and hence overall cost is increased that is undesired now if we want to be efficient in terms of cost as well as performance of device then we will have to do a trade-off between different parameters to find an optimum result. Enhancement in performance of portable devices need low power consumption and increase the yield of the circuit. Root cause of using new IC is low power circuit design which is merged in digital ICs [1-5]. As with inserting more no of transistor count the chip die area increases as a results unwanted bad current flow inside the device which reduces overall performance of the circuit. The main aim of the research is to reduce the leakage power inside the transistor to improve the functionality of the device. Not only the increased no. of transistor count but the operating frequency of clock is also a major attribute for development of high performance Digital based application circuit. As there is a huge demand in early nineties to save the area and power, which results in development of MOS technology for mitigation of power consumption. The MOS technology not only reduced the power but overall performance is improved while increasing the speed of the circuit. It exist somewhere between static and dynamic circuit. So dynamic circuit, combines the benefit of static and pseudo NMOS, introduced to enhance the performance and reduce the size simultaneously. Intention of dynamic logic is to use charge stored in parasitic capacitances in a fruitful manner. Dynamic circuit is similar to sequential circuit with memory function [6-9]. Dynamic circuit used widely, for improvement of performance parameters like reduction delay, mitigation of power and less transistor count in comparison of static circuit design.. Domino logic CMOS circuit allows significant reduction in number of transistor count. It also plays a vital role where fan-in of the domino circuit is high are high such as multiplexer or comparator circuit. There are several applications on which domino circuit can be made like turnery adder for high speed application [10-15].

In Domino circuit design there is novel circuit design for mitigation of power and improvement in UNG in ultra-deep submicron technologies with the use of CNTFET technology. While proposed design is implemented for enhancement of speed in the microprocessor with less power consumption. Here we have compared two technologies MOS and FinFET and show that there is improvement in the performance parameters. All the simulation is performed at 32nm process technologies, theses technologies has better impact in the device scaling with improvement of all process parameters. The CNTFET is the future of digital world and all angle for views of the CNTFET transistor in Fig.1[16-17].

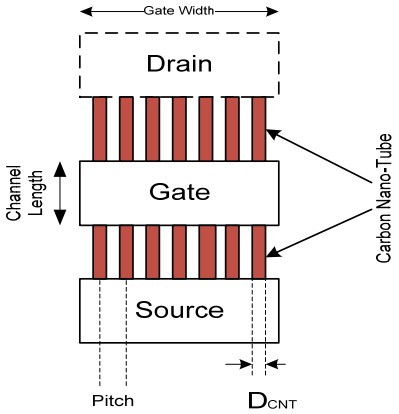


Fig.1 Top view of CNTFET

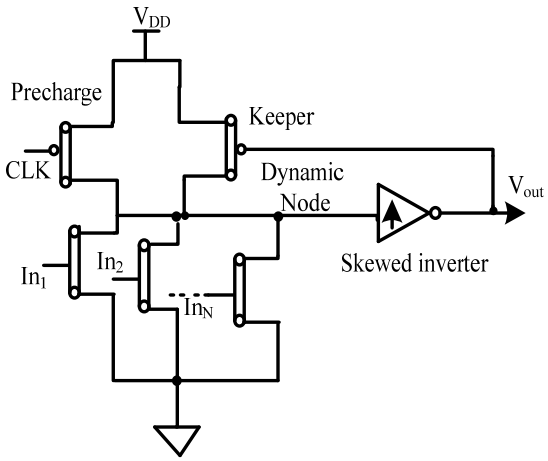


Fig.2 SFLD

## II. RELATED WORK

Domino circuit includes noise margin problem because of parasitic capacitance, charge sharing at internal nodes and due to that false output may be produced. As compared to static CMOS circuit domino have faster switching speed and lesser area. Domino is not a rationed logic. Domino logic work on two phase mostly ,or clock, that provides us pre-charge and evaluate phase, when the signal of clock is zero circuit enters into the pre-charge state and dynamic node is charged to Vdd and when clock is high the circuit is in evaluate phase and NMOS network perform it's implemented logic according to input[18-19].

The keeper ratio *K* is defined as

$$K = \frac{\mu_P\left(\frac{W}{L}\right)_{Keeper-transistor}}{\mu_n\left(\frac{W}{L}\right)_{evaluation-network}} \quad (3)$$

Here the *W* and *L* ratio plays a major role in sizing of the transistor, and $\mu_n$ and $\mu_p$ is the mobility of electron and hole, of the circuit. In complex dynamic circuits, where several stages are present, clock should be maintained means the circuit should be pre-charged and in evaluate cycle executed completely but practically due to several interconnects, parasitic capacitances, and resistances delay occurs for different stages this is called as clock skew problem some time also called as hazard or race condition. In domino logic circuit, if we see the circuit enters in the evaluation phase the clock pulse is low level when help in turning NMOS block which act as a OR gate operation where leakage is maximum. It does not affect the leakage current in the circuit [4]. Here a existing approach is simulated in the same platform and measure the results in order to improve the performance of the novel technique with comparing with existing approach [20], high-speed domino (HSD) [12], [14], as shown in

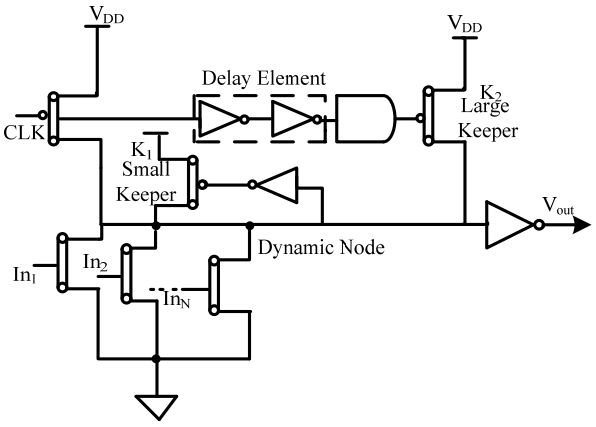


Fig.3 (a) CKD

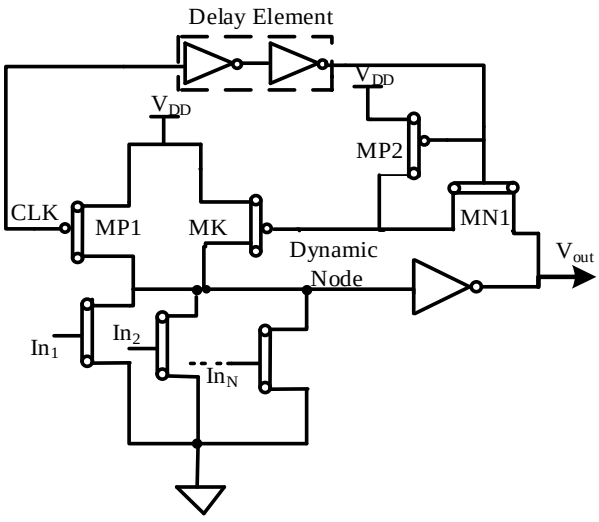


Fig.3 (b) HSD

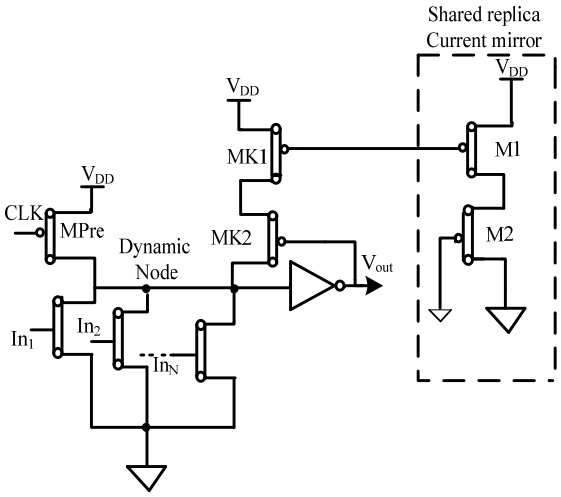


Fig.3 (c) LCR Keeper

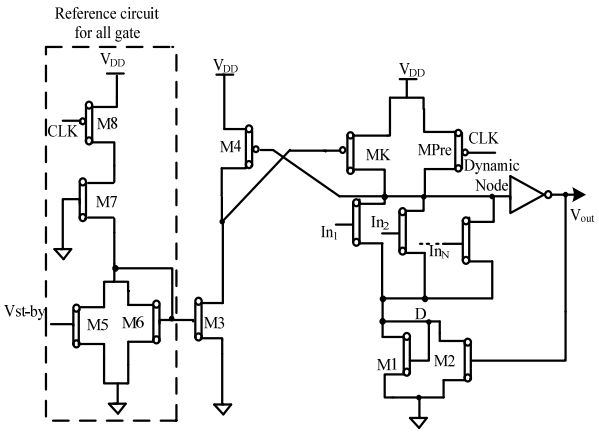


Fig.3 (d) CKCCD

Here there is several modification is done to improve the performance as diode by using a NMOS mirror transistor which in DFD which improves all primates [10], the clock signal reduces the delay it is known as HSD circuit in both the phase [11], another approach which help in CEDL with combination of both the logic [13] to generate a novel technique.

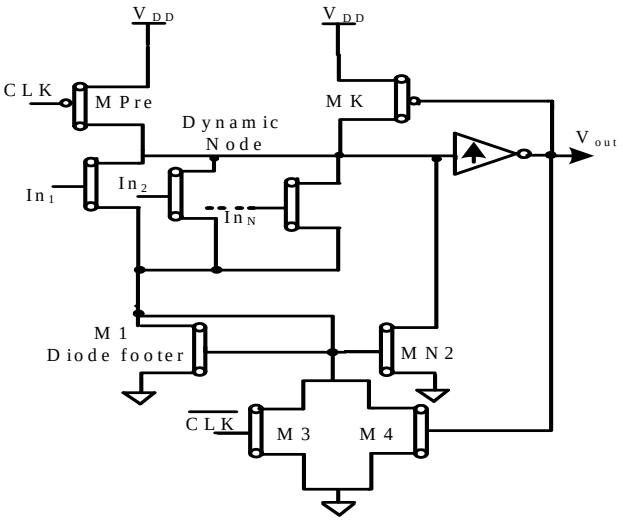


Fig.4 (a) DFD

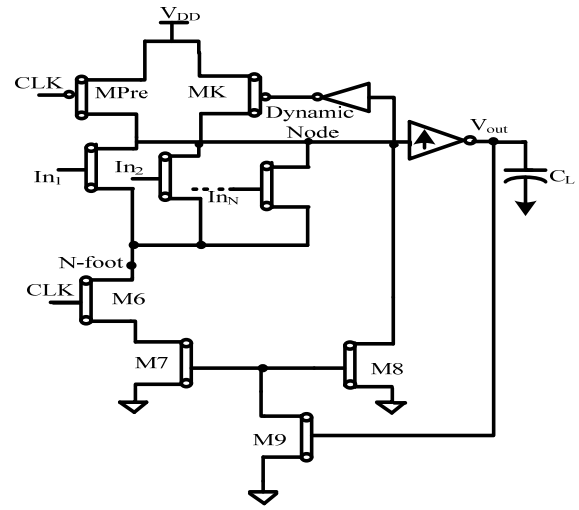


Fig.4 (b) CMFD

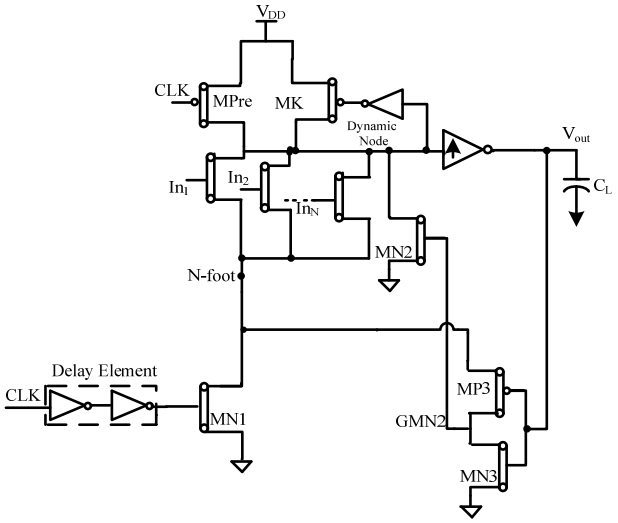


Fig.4(c) HSCD

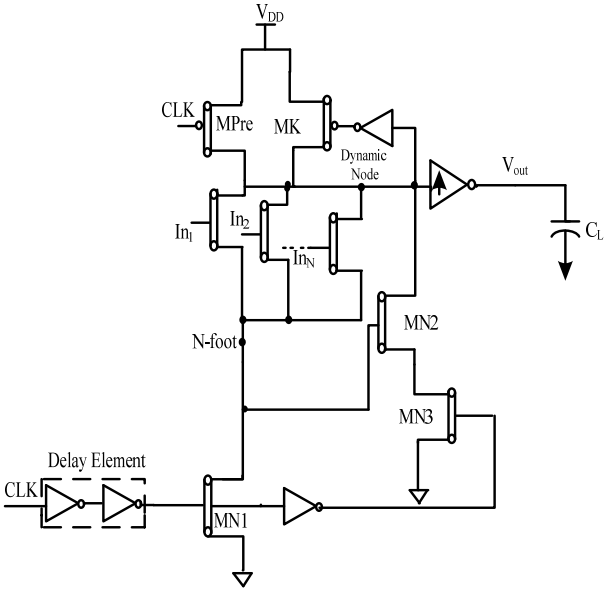


Fig.4 (c) CEDL

Due to the increasing demand of functions in the portable devices such as smart phones laptops tablets etcetera, successive scaling is required according to moor's law, that is number of transistor will be double in every two year, that result in more number of transistor count that causes increased packing and cooling cost and hence overall cost is increased that is undesired now if we want to be efficient in terms of cost as well as performance of device then we will have to do a trade-off between different parameters to find an optimum result . Enhancement in performance of portable devices need low power consumption and increase the yield of the circuit. Root cause of using new IC is low power circuit design which is merged in digital ICs.

Not only the increased no. of transistor count but the operating frequency of clock is also a major attribute for development of high performance Digital based application circuit [21-22].

It exist somewhere between static and dynamic circuit. So dynamic circuit, combines the benefit of static and pseudo NMOS, introduced to enhance the performance and reduce the size simultaneously. Intention of dynamic logic is to use charge stored in parasitic capacitances in a fruitful manner. As there is a huge demand in early nineties to save the area and power, which results in development of MOS technology for mitigation of power consumption. The MOS technology not only reduced the power but overall performance is improved while increasing the speed of the circuit.

Dynamic circuit is similar to sequential circuit with memory function. Dynamic circuit used widely, since it provides higher speed, less power consumption and less area in comparison of static circuit design. Domino logic circuit is a type of dynamic logic which is used where high performance is the prime requirement. Domino logic CMOS circuit allows significant reduction in number of transistor count. It also plays a vital role where fan-in of the domino circuit is high are high such as multiplexer or comparator circuit [23].

During this phase, applied clock pulse is high and implemented functions start operating as per input at that moment, the inputs are allowed to switch to high level. Some voltage drops across the diode footer M1 due to the leakage current of the evaluation transistor. Therefore at the evaluation transistors, that is in OFF mode, a negative voltage exists between gate and source. Due to this negative voltage subthreshold current reduces exponentially. Furthermore, the body effect of the evaluation transistors is increased by the voltage-drop across the diode, resulted in subthreshold leakage reduction. Switching threshold voltage of the gate is increased by threshold of NMOS devices as shown in Fig.4. (a) to (d).

In CMFD approach a mirror transistor is adder and compare the voltage of the input and evaluation face voltage so to improve the UNG of the circuit without any degradation of performance of the circuit [19] as shown in Fig.4. (a) to (d)..

## III. SIMULATIONS RESULTS AND COMPARISONS

The existing and proposed domino circuit techniques are implemented in the CNTFET and CMOS technologies. For gating the fair comparison of the results we simulated the existing and proposed circuit at same environment at 32nm of process technology with the help of BPTM library 0.9V of supply voltage, output capacitance of the circuit is taken as $C_L$=1pF and. The noise parameters is the main cause to improve performance as noise UNG reduces if OR transistor increases. Average power, Delay, power-delay product (PDP), evaluation delay and standby power for the different schemes of the OR gate with the fan-in gates 8 and 16 inputs.

Upsizing of the keeper transistor which helps in improving the circuit robustness, but increases the power consumption, evaluation delay and degrades the performance. For improvement of UNG of the circuit the sizing of feedback keeper transistor must be taken into the consideration which help in maintaining the robustness with proper sizing. Variations in the keeper size are from 0.25 to 1.5 due to the high contention current produced by the large keeper, with clock frequency of 10 MHz.

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15.42% DFD which is shown for the 8 and 16 input OR gates, respectively is observed to exponentially reduce, and the PDP of the circuit reduces overall drastically for both the 8 & 16 inputs of the FinFET domino circuit.

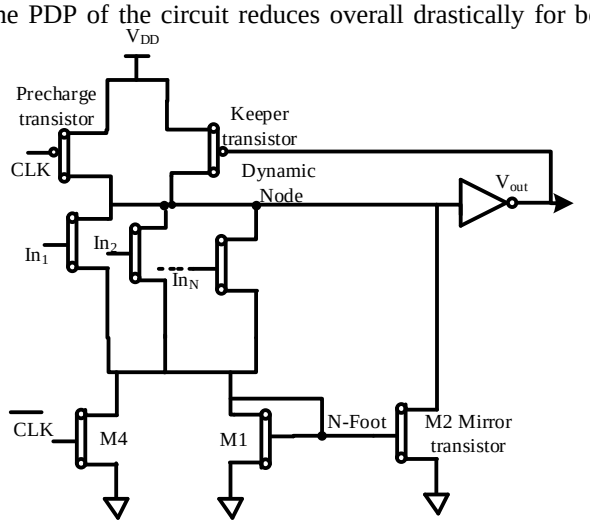


Fig.5. Proposed Logic Design

The evaluation network to make the diode footed, whose drain and gate terminal are shorted, and which also produces the stacking effect. The stacking height increases the charge store in the evaluation network which increases the delay; therefore, the current mirror transistor $MN_2$ is added in parallel to transistor $MN_1$ which facilitates fast discharge the charge which store in dynamic node, quickly reducing the evaluation delay. The transistor MN4 whose gate is connected with the output node helps to fully discharge the dynamic node to ensure the achievement of the proper logic level, if the dynamic node is discharging during the evaluation phase. Also, if there is a voltage drop across transistor $MN_1$ due to the presence of noise voltage, there is a flow inside the transistor is known as leakage current in transistor $MN_2$ and the circuit with more power dissipation to become less noise robust. To avoid this situation, transistor $MP_3$ is connected below the mirror transistor $MN_2$ to provide a stacking effect whose gates are biased with the clock.

Transistor $MN_1$ is added to the diode configuration below

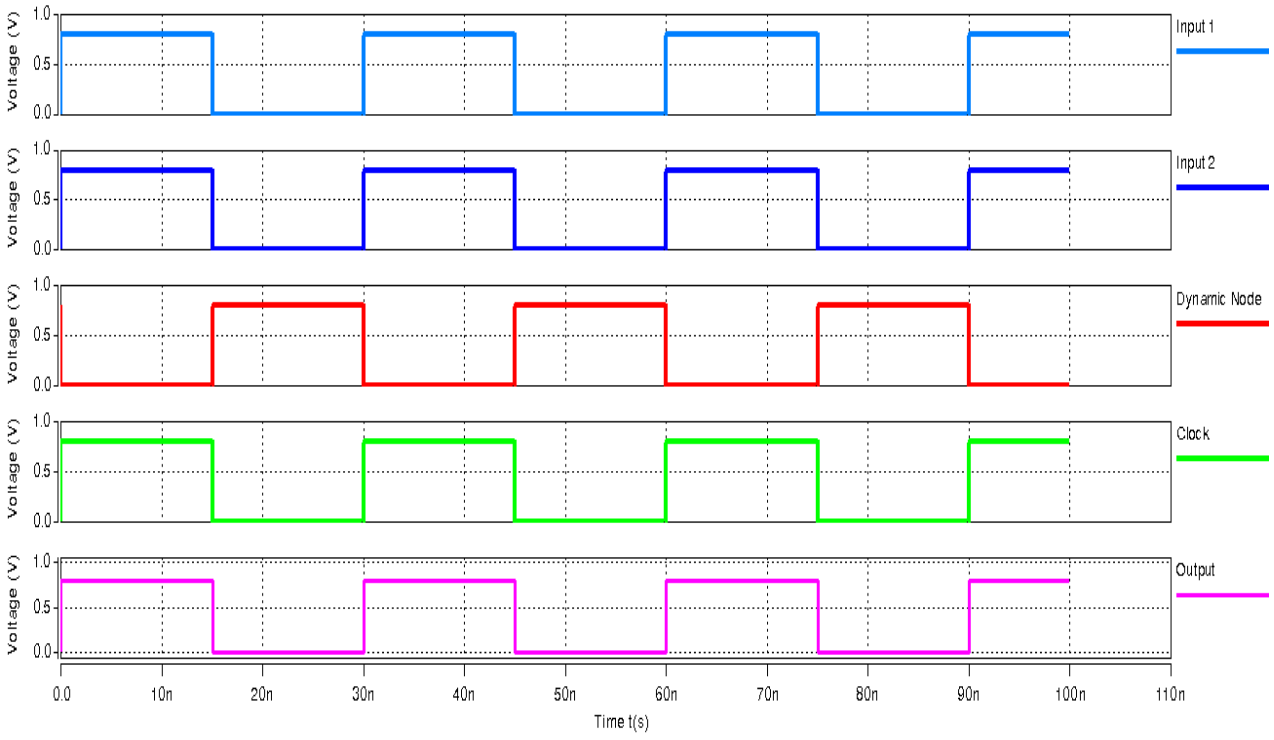


Fig.6: 4-input OR gate DFD logic

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**Table I.** Proposed Domino Circuit by varying Back gate Voltage of PUN and $V_{DDH}$=0.9V

| | Average Power | | Delay | | PDP | |
|---|---|---|---|---|---|---|
| | CMOS | CNTFET | CMOS | CNTFET | CMOS | CNTFET |
| FLD | 0.1200 | 0.0316 | 9.635 | 8.243 | 1.156 | 0.3458 |
| FDL | 0.0776 | 0.0242 | 15.58 | 13.45 | 0.492 | 0.0563 |
| HSD | 0.1306 | 0.0342 | 9.185 | 7.982 | 1.199 | 0.4837 |
| CKD | 0.1537 | 0.0428 | 10.32 | 9.541 | 1.586 | 0.3635 |
| Proposed Circuit | 0.1132 | 0.0340 | 6.214 | 6.136 | 0.664 | 0.0342 |

**Table.II..** Comparison of Proposed and Existing approch

| Input | | Proposed | (CKD ) | (HSD) | LCR Keeper | CKCCD | (DFD) | (HSCD) | (CEDL) |
|---|---|---|---|---|---|---|---|---|---|
| | Power (nw) | 18.98 | 6931 | 37.786 | 24.70 | 138.94 | 22.90 | 37.78 | 49.11 |
| | Delay (ps) | 6.144 | 7.614 | 6.258 | 7.582 | 1352 | 9.410 | 6.257 | 11.53 |
| 2 | PDP (aJ) | 0.116 | 52.77 | 0.236 | 0.187 | 187.8 | 0.215 | 0.236 | 0.566 |
| | Power (nw) | 22.99 | 6990 | 41.758 | 28.78 | 48.58 | 28.33 | 41.75 | 58.04 |
| | Delay (ps) | 6.138 | 7.243 | 6.333 | 7.618 | 590.7 | 9.989 | 6.333 | 12.14 |
| 4 | PDP (aJ) | 0.141 | 50.62 | 0.264 | 0.219 | 28.69 | 0.282 | 0.264 | 0.704 |
| | Power (nw) | 30.27 | 7024 | 49.200 | 35.51 | 41.18 | 41.49 | 49.20 | 192.64 |
| | Delay (ps) | 6.479 | 7.419 | 6.704 | 7.799 | 293.2 | 11.484 | 6.704 | 13.472 |
| 8 | PDP (aJ) | 0.196 | 52.11 | 0.329 | 0.276 | 12.07 | 0.476 | 0.329 | 2.595 |
| | Power (nw) | 45.06 | 7052 | 63.892 | 50.12 | 58.73 | 80.82 | 63.89 | 899.77 |
| | Delay (ps) | 7.500 | 8.200 | 7.747 | 8.842 | 190.2 | 13.956 | 7.747 | 16.156 |
| 16 | PDP (aJ) | 0.337 | 57.82 | 0.494 | 0.443 | 11.17 | 1.127 | 0.494 | 14.53 |
| | Power (nw) | 73.85 | 7088 | 92.89 | 574.2 | 91.88 | 158.95 | 92.89 | 1366 |
| | Delay (ps) | 9.744 | 8.200 | 10.051 | 9.588 | 174.71 | 18.924 | 10.05 | 22.48 |
| 32 | PDP (aJ) | 0.719 | 58.12 | 0.933 | 5.505 | 16.05 | 3.007 | 0.933 | 30.70 |
| | Power (nw) | 131.9 | 7.148 | 150.42 | 665.2 | 114.09 | 238.08 | 150.42 | 1167 |
| | Delay (ps) | 12.46 | 14.47 | 14.57 | 10.181 | 124.78 | 40.572 | 14.574 | 104.5 |
| 64 | PDP (aJ) | 1.643 | 0.103 | 2.191 | 6.772 | 14.23 | 9.659 | 2.192 | 121.9 |

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## IV. CONCLUSION

The main contribution of the domino circuit implementation is to increase the speed of operation of the transistor and made GHz range of frequency to compete this nanoscale world, the domino circuit is the extended version of MOS technology. Domino circuit design saving the average power consumption of 19.16%, 31.21% SFLD technique, 39.72%, 38.84% HSD techniques, 51.23%, 49.62% CKD techniques, 29.73%, 40.23% DFD and when compared with MOS based proposed techniques it saving the average power of 14.84%, 24.64% SFLD, 34.63%, 32.73% HSD, 86.32%, 84.43% CKD, 18.36%, 24.83% LCR, 15.23%, 16.73% DFD . SFLD has a speed improvement of 19% as compared to DFDL and noise immunity also increases. SFLD is highly improved method for faster operation of circuit design.

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