A Robust and Efficient Fault-Resilient RadHard ADPLL

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Abstract—**The high pace emergence in semiconductor technologies and associated application demands have revitalized industries to explore power efficient, stable and fault tolerant digital communication solutions, particularly for time critical applications operating at higher frequency ranges. Thus strengthening low cost CMOS digital design with Radiation Hardened by Design (RHBD) approach can be of paramount significance compared against the high cost Radiation Hard by Process (RHBP) approach. With this motivation, in this paper a novel and robust All-Digital-Phase Locked Loop (ADPLL) design has been developed for frequency synthesis. Our ADPLL design model encompasses multiple novelties and contributions including Feedback-Divider-Less-Counter (FDLC) based ADPLL, predictive phase-frequency detection (PFD), enhanced Time to Digital Converter (TDC) to detect next-edge occurrence of the reference clock that reduces locking period and complexity. The predictive PFD applies a phase-prediction scheme that delays the clock-edges of the reference frequency with a calibrated amount that it always aligned towards the expected frequency clock edge. It makes TDC to be narrow enough to cover the reference and oscillator jitter. Our proposed ADPLL design applied a narrow range converter (TDC) that assist phase-error prediction, correction and phase detection. The reference clock delay facilitates accurate timing relationship estimation with the variable frequency and hence performs retuning of the variable clock to reduce locking period and reduce noise. The ADPLL design has exhibited satisfactory performance for the frequency synthesis with reference frequency of 20MHz and the synthesis frequency of 2.4 GHz meeting radiation hardened features. The simulation results has revealed that the proposed Rad Hard ADPLL design can be a potential solution for space communication systems by maintaining low jitter of 340ps and power consumption of 371.7mW, as the narrow range TDC designed can detect sample radiation induced impulse noise of 20ns, 1mV and correct it.**

Key words—RHBD,ADPLL; frequency synthesis; phase frequency prediction, FDLC-ADPLL, Radhard ADPLL, DTC, TDC

I. INTRODUCTION

The high pace emergence in semiconductor and associated hardware technologies have revitalized almost major industries to facilitate power efficient, stable and fault tolerant digital solutions for space applications, industrial purposes as well as defence strategic utilities. However, with rise in application demands and associated complexities the proportionate needs for system optimization has also been realized. The technique called

Phase-Locked Loop (PLL) signifies a closed-loop frequency-control mechanism that exploits the key information such as the difference of phase between the input clock signal and the feedback clock signal of certain controlled oscillator unit. Since the day of inception, PLLs have been found as a potential candidate to perform time recovery and frequency synthesis. In addition, it has been realised for generating an variable frequency source with a pre-defined input frequency. Furthermore, its robustness enables it to be applied for tracking or locking input signals in both phases as well as frequency domain. Whenever the frequency and the phase of the input signals become synchronized, the PLL is stated to be in the locked state. In locked period, the phase difference between the reference signal and the output signal remains constant. As stated, PLLs are used in major application such as motor speed control, frequency control, clock signal recovery, etc. The versatility of PLLs enables it to be embedded in advanced microprocessor chipset and modern communication systems to perform modulation, demodulation and the carrier frequency regeneration from an input signal in which it is suppressed during transmission [1]. Furthermore, PLLs are applied to perform local clock synchronization with other signals. Considering the architectural discussion, the key components of PLL are the Phase Frequency Detector (PFD), loop filter units, charge pump, Voltage Controlled Oscillator (VCO), counters like feedback counter, pre/post counters. Typically, classical PLLs apply analog methods for designing; however integrating PLL with noise-prone application environment is highly tedious and somewhere confined. As per current knowledge majority of PLLs apply Analog Loop Filters (ALFs) and voltage controlled oscillators which are practically highly complicated to integrate with noisy environment. Even the traditional PLLs can't be ported to the advanced processors. In last few years, the emergence of deep-submicron CMOS technologies have enabled digitization of major traditional analog circuits, comprising the analog PLLs that as a result could be vital to overcome above mentioned issues and to achieve more efficient solution than classical analog implementation.

The implementation of Digital PLL architecture by incorporating digital loop filters and oscillator circuits is suggested [2], [3]. Thus, the digital implementation of the different PLL components gives rise to the new type of PLL called All-Digital Phase-Locked Loop (ADPLL). ADPLL

designs have turned out to be more significant due to augmented programmability, configurability, portability and stability over varied processes. In addition, it has been found robust against noisy environments. In fact, ADPLL has been widely studied for clock generation in digital systems to substitute classical analog PLL designs [4], [5]. In comparison to the classical PLL designs, ADPLL possess numerous advantages including higher (switching) noise immunity, configurability and portability to the advanced digital processors that possess vital significance in communication systems and consumer applications [6][7]. In addition, ADPLL has significant contribution towards Electronic Design Automatic (EDA) tools where it is found efficient in reducing design time. Digital filter of the ADPLL too reduces the design area significantly that enables overall hardware design to be more scalable to meet rising miniaturized design-demands. Furthermore, ADPLL can perform frequency tunning of the Digitally Controlled Oscillator (DCO) by means of digital codes that makes it more efficient to accomplish swift frequency acquisitions [8]. In last few years, the robustness of ADPLL has enabled it to be used for frequency synthesis [9] [10] [11]-[16] and data recovery [17-21] related applications. The efficacy of ADPLL, particularly in terms of flexibility, re-configurability, transfer function precision, settling speed, frequency modulation capability, and amenability to integration with digital baseband and application processors makes it a dominating choice for frequency synthesis [22],[23]. With nano-scale CMOS implementation it ensures low area, low power consumption and higher performance [24-26].

The above discussion reveals that ADPLL outperforms classical PLLs and have more significance towards communication systems as well as consumer applications. However, exploring in depth it can be found that there are numerous real-time application environments such as space radiation conditions where ADPLL undergoes adversaries due to emergence of relatively small square impulse in the main signal. Removal of such insignificant noise impulse is inevitable to avoid logical faults and resulting hazardous consequences. Eliminating the presence of jitter and other noise components while maintaining minimum lock period, can make ADPLL more suitable in real time applications for frequency synthesis, clock recovery, clock de-skewing, . With this motivation, in this paper a robust and highly radiation-heat fault tolerant ADPLL design is proposed for frequency synthesis. Our proposed system incorporates a novel dual-mode operation, Frequency-Acquisition Mode (FAM) and Phase-Acquisition-Mode (PAM). In FAM process, we have applied a feed-forward compensation model that takes two distinct reference cycles for calculating ADPLL parameters (predict variable and desired variable). Once estimating the predict variable, it is fed as input to a newly developed Numerically Controlled Oscillator (NCO) assisted DCO (N-DCO). It is then followed by the execution of PAM that activates PLL to minimize residual frequency error.

The other sections of the presented research paper are divided as follows. Section II discusses related works pertaining to ADPLL designs. In Section III proposed research method and

components discussion is presented, which is then followed by the discussion of the implementation and results in Section IV. Section V presents the overall conclusion and future works. References used in this study are mentioned at the end of the manuscript.

Some of the key variables and the list of abbreviations are given as follows:

TABLE I. ABBREVIATIONS

Variable	Definition
PLL	Phase-Locked Loop
PFD	Phase Frequency Detector
VCO	Voltage Controlled Oscillator
ALF	Analog Loop Filters
CMOS	Complementary Metal-Oxide Semiconductor
ADPLL	All-Digital Phase-Locked Loop
EDA	Electronic Design Automatic
DCO	Digitally Controlled Oscillator
LF	Loop Filter
ED	Edge Detector
FAM	Frequency-Acquisition Mode
PAM	Phase-Acquisition Mode
N-DCO	Numerically Controlled Oscillator Assisted DCO
DDS	Direct Digital Synthesizer
DDFS	Fractional-N Direct Digital Frequency Synthesizer
FDC	Frequency-to-Digital Converter
FA	Flying-Adder
SET	Single Event Transient
RF	Radio Frequency
DTC	Digital-to-Time Converter
DLL	Delay Locked Loop
PTM	Predictive Technology Model
PP-ADPLL	Phase-Prediction ADPLL
ref_{freq}	Reference Frequency
FCW	Frequency Command Word
Var_{clk}	Variable clock
FD	Feedback-Divider
FDLC	Feedback-Divider-Less Counter
PFD	Phase-Frequency Detector
TDC	Time-to-Digital Converter
CG	Conversion Gain
TDC	Timestamp/Time-to-Digital Converter
TWI	Tuning Word Inputs
PVT	Process, Voltage, Temperature
ref_{clk}	Re-Timed Reference Clock
PI	Proportional-Integral
UI	Unit Interval

TABLE II. NOMENCLATURE

Variable	Definition
f_{Ref}	average Reference frequency
T_{Ref}	Time to cover average reference frequency
$PE[t]$	phase error
$Ref\phi[t]$	reference phase
$Var\phi[t]$	variable phase
$f_{Ref}/\widehat{G}_{nor(DCO)}^{X=\{pb,ab,tb\}}$	Gain Normalization Multiplier

f_{BW}	3-dB cut-off frequency of the closed PLL loop
$G_{nor(DCO)}^{pb}$	DCO gain parameter during process
$G_{nor(DCO)}^{ab}$	DCO gain parameter during acquisition
ξ	Damping factor
$Ref\phi_F[k]$	Fractional reference phase
ref_{freq_D}	delayed form of the reference clock
Var_{clk_G}	gated Var_{clk} clock
$PE_F[t]$	dynamic phase error
$PE_I[t]$	integer phase error
PE	phase error
ϵ	statistical expectation factor
t_{s2}	timestamps of the Var_{clk} edges
t_{s1}	timestamps of the ref_{freq} edges
C_p	clock period of Var_{clk}
$G_{nor(DTC)}$	DTC Gain
$\Delta d_{(DTC)}$	step size of the LSB delay in the DTC
EXP_{freq}	Fixed point DTC control
$PE_F[t]$	fractional component of the phase error
$Var\phi_I[k]$	integer component of the variable phase
TDC_{res}	TDC Resolution
t	inverter delay
$G_{nor(TDC)}$	TDC Gain parameter
φ	Filter coefficient
FCW_F	fractional component of FCW
η	Step size

II. RELATED WORK

This section primarily discusses some of the key literatures pertaining to frequency synthesis using ADPLL. The prime objective of this discussion is to assess various approaches available and their respective strengths as well as limitation so as to derive a novel and robust fault tolerant and radiation hard ADPLL based frequency synthesizer.

A. ADPLL based frequency synthesizer

Unlike analogue or traditional PLL designs, ADPLL designs have played vital role in recent days CMOS design. In [27], a number of RF ADPLL designs are discussed. Authors have stated that though ADPLLs enables better phase-noise correction and enhancement of analog PLLs; however in-band spur level necessity often remains challenging. As enhancement, authors suggested digital-to-time converter (DTC) based ADPLL design where the time resolution can be scaled effortlessly. An enhanced ADPLL design was proposed in [28] where Delay Locked Loop (DLL) was used as the major core to replace classical PLL design. Authors in [29] derived a gain tracking model for ADPLL by exploiting correlation analysis. In addition, they applied correlation approach to identify unidentified impulse response from DCO input to TDC output where the use of training signal enabled better accuracy. In [29], authors developed fractional-N frequency synthesizer using ADPLL that employed phase-frequency detector, up/down counter as LF, P-Divider counter as DCO. In their design, the dual-modulus N/N+1 divider were managed through the output of the sigma-delta modulation to attain the aim of spur lessening. In [30], fractional-N PLL based frequency synthesizer was developed where an additional TDC was applied to estimate the

fractional value. Their proposed frequency synthesizer model was developed using 32nm CMOS Predictive Technology Model (PTM) at 0.9V supply voltage. A similar effort was made in [31], where authors derived a fractional frequency synthesizer using ADPLL. In [32-34.] an ADPLL-based frequency synthesizer was developed for WiMAX application. The proposed ADPLL focuses on enabling fault tolerant frequency synthesis in the rage of 2.3-2.7GHz for low range applications using frequency divider architecture. Authors [35] applied flying adder (FA) design based ADPPL frequency synthesizer. Due to sophisticate design FA it has enabled swift and efficient frequency synthesis to give a steady clock signal. In [36], a wide-band digital fault resilient frequency synthesizer was developed for cognitive radio sensor using ADPLL. In their architecture authors applied a digitally managed ring oscillator with an LC tank arranged to expand tuning range and minimize power dissipation. In [37] signal processing based approach was developed to perform ADPLL control to enable loop based fast frequency acquisition or tracking with excellent phase noise and spurious performance. Authors in [38] developed an ultra-wideband, low-power frequency synthesizer for Ku-band FMCW radars. Authors considered adaptive loop bandwidth to reduce alterations of the loop tracking feature in ramping under diverse chirp rate, through which, a low frequency RMS error of ~179kHz was attained for the chirp rate below 2GHz/ms. Observing above literatures it can be visualized that a number of significant efforts have been made to design enhanced ADPLL design so as to perform fault resilient and efficient frequency synthesis. However, the demand of minimum lock in period, minimum power consumption, minimum jitter etc has always remained an open research area. With this motivation, in this paper a robust and efficient fault resilient RadHard ADPLL based frequency synthesizer is designed.

III. OUR CONTRIBUTION

This section primarily discusses the proposed ADPLL design and implementation for frequency synthesis. Before discussing proposed design and implementation, a snippet of types of ADPLL is given:

A. Types of ADPLL

Typically, ADPLL is designed in two approaches; Feedback-Divider (FD) based ADPLL design (Fig. 1) [39-42] and Feedback-Divider-Less Counter (FDLC) enabled ADPLL design (Fig. 2) [24-26], [43-44]. Though, FDLC based ADPLL was developed before FD-ADPLL, FDLC-ADPLL has significant demand across industry because of competitive characteristics and even better feature than the Fractional-N charge-pump PLL by means of dithering of the modulus divider [45-46]. In ADPLL VCO is replaced with a DCO for generating expected frequency signal of the output variable clock (Var_{clk}). Similarly, a Phase/Frequency Detector (PFD) and charge pump are replaced by a Time-to-Digital Converter (TDC) to detect phase removals of the varying clock vs. the frequency reference (ref_{freq}) clock. In ADPLL design the analog loop RC filter is replaced by a digital loop filter so as to add DCO into the
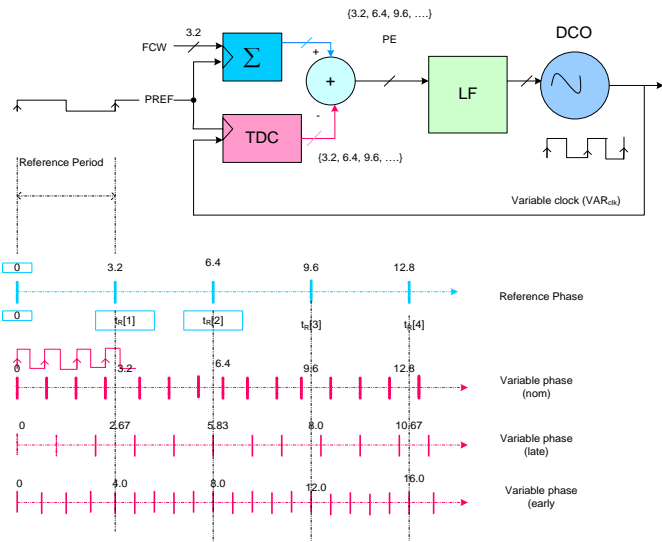
frequency and phase lock. Here, the Conversion Gain (CG) of DCO and TDC are predicted and compensated using efficient digital logic. Exploring in depth it can be visualized that the prime differentiating factor that distinguishes the two types of ADPLL is the way that the variable clock Var_{clk} is fed into TDC for phase/frequency detection. As depicted in Fig. 1, the Var_{clk} is edge-divided in such that maintains its average frequency equivalent to the reference frequency ref_{freq} clock.

Fig 1. FD Divider Based ADPLL

This model applies the noise-shaped dithering (Fig. 1) to obtain random Var_{clk} frequency and hence forcing the range of TDC to be augmented significantly. Furthermore, it is found that the phase error at TDC might impose or increase significantly high amount of phase-frequency noise which is required to be minimized or eliminated by means of certain loop filter. This as a result imposes additional burden of loop filtering to reduce noise components. Additionally, it might requires certain sophisticated design to distinguish ref_{freq} and down-divided Var_{clk}. This model requires an additional frequency detection unit too, particularly during frequency-settling. Applying TDC as envelop to cover complete $T_{Ref} = 1/f_{Ref}$ can also be a potential solution. The above mentioned complexities could be alleviated by means of more efficient hardware design.

Since, in this research we intend to develop a robust radiation-hard fault resilient ADPLL design, we have preferred FDLC-ADPLL that not only reduces computational complexity but also achieves swift locking time to perform frequency synthesis.

Fig. 2 presents the FDLC-ADPLL concept of phase-domain function. Interestingly, our proposed FDLC-ADPLL model avoids aforesaid problems in the classical FD-ADPLL design. In our proposed model, the classical TDC model is redefined and stated as Timestamp-to-Digital Converter (TDC) that comprises both the fraction components as well as integer component of the variable phase. In fact, it enables managing the fractional frequency ratio by avoiding any dithering requirement. In this model, both Var_{clk} as well as TDC are connected directly and since no dithering is applied the TDC covers relatively narrow range of Var_{clk} phase which is significantly lower than the ref_{freq} phase, which can be increased significantly at the system level by means of a Var_{clk}-edge counter [47]. Noticeably, the output is a definite number comprising the integer count of the Var_{clk} cycles and the normalized fractional difference between ref_{freq} and Var_{clk} edges. At the basic level, FDLC-ADPLL functions in the true-phase model [48], where it compares the variable phase of the multiple-Gigahertz (GHz) DCO with lower reference frequency, for example 8-40MHz. Since, in this research the emphasis is made on the frequency synthesis of 2.4 GHz by applying reference frequency of 20 MHz, FDLC-ADPLL becomes a potential solution to meet the requirement. In this model, the comparison output signifies the digital phase error which is then processed with digital loop filter so as to adjust DCO frequency in the negative feedback approach. Literatures [49,50] reveal that the FDLC-ADPLL model outperforms classical FD-ADPLL model in terms of computational time, power consumption and cost. It makes it suitable to be used in major higher-end applications such as mobile phone and consumer electronics and is being used in almost 33% of the mobile manufacturing globally. A schematic of the FDLC-ADPLL based phase domain operation is illustrated in Fig. 3.

Fig 2. FDLC based ADPLL

Fig 3. Illustration of a phase-domain FDLC-ADPLL function

As depicted in Fig. 3, the reference frequency signal information is completely encompassed in the transition period, also called as the timestamps of the ref_{freq} clock. Amongst the two feasible transition possibilities, in our proposed model only the edges of the rising clock are taken into consideration. Similarly, the time-information of the Var_{clk} is also included in its rising edge timestamps. As depicted in Fig. 3, FCW, which signifies the expected or the targeted frequency multiplicative ratio, is assigned as 3.2. As, the oscillation period refers the inverse of the oscillating frequency, there can be 3.2 Var_{clk} clock cycles per single cycle of the reference frequency ref_{freq}. Here, it is assumed that the initial phase is zero and therefore the rising edges of ref_{freq} and Var_{clk} are aligned at the initial time (i.e., zero time), though it is not inevitable. In fact, the phase domain function as depicted in Fig. 3 takes place on the basis of numerical estimation of the phase error PE[t], which is obtained as the difference in between the reference phase Refϕ[t] and the variable phase Varϕ[t]. Noticeably, here the phase estimation is denoted in terms of the Unit Interval (UI), which signifies clock period of the Var_{clk}. In this manner, the reference phase states the required Var_{clk} cycles originating from the time zero. In practice it is estimated as the cumulative addition of FCW, i.e., Refϕ[t] = ∑ FCW[t]. In summary, estimating the difference between the actual and ideal count of Var_{clk} cycles at each reference edge gives the value of phase error. Mathematically,

$$PE[t] = Ref\phi[t] - Var\phi[t] \qquad (1)$$

Once retrieving the value of the phase error the DCO frequency is adjusted. In case, the phase error requires to be augmented the DCO requires speeding up. Similarly, if the variable phase gets lower it signifies that the DCO has become slower, and in case the reference phase becomes higher it would state that there is a higher count of Var_{clk} cycles per ref_{freq} cycle. Considering ref_{freq} clock as stable and constant FCW,

both conditions signify that the DCO is getting slower. On contrary, if FCW increases, the DCO is supposed to be speed up. Thus, applying the above discussion FDLC-ADPLL design, in this research work a novel and robust frequency synthesizer is developed.

The following section discusses the implementation of the proposed fault-tolerant FDLC-ADPLL design.

B. ADPLL Implementation

Taking into consideration of the robustness and efficiency, we have applied FDLC-ADPLL architecture for radiation-hard fault tolerant ADPLL based frequency synthesis. A depth insight of the proposed ADPLL model is given in Fig. 4.

Unlike traditional phase prediction approaches, in our proposed ADPLL design, an enhanced phase prediction technique is applied [51]. As depicted in Fig. 4, the DCO component exhibits not merely a single but three distinct inputs (say, Tuning Word Inputs (TWI)) so as to control the Process, Voltage, Temperature centring (PVT); acquisition and tracking, distinctly. In this model, the PVT bank (In Fig. 4, "p") re-centres the natural frequency of DCO to the mid of the chosen frequency band. Similarly, the acquisition bank signified as "a" exhibits channel selection by means of swift settling towards the expected frequency. The third bank (i.e., "t") refers the tracking bank which is the one actually used during communication. One of the key strengths of the proposed ADPLL design is that it transverses the p/a/t banks swiftly with increasingly finer frequency steps while exhibiting reduction of the loop bandwidth iteratively.
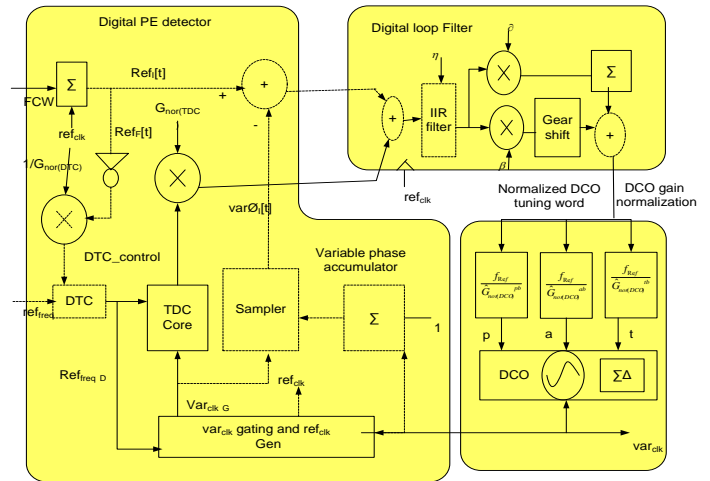

Fig 4. Depth design for FDLC-ADPLL

Implementing this approach, the overall settling period can be made very fast irrespective of the initial frequency difference. Now, to enable efficient ADPLL control, particularly its filtering ability, 4th order IIR filter is applied which is then followed by the use of a PI controller that embodies gain parameters, β and δ, respectively.

$$f_{CPLL} = \frac{f_{Ref}}{2\pi} \times \beta \qquad (2)$$

Where, f_{CPLL} presents the 3-dB cut-off frequency of the closed PLL loop. In practice, the eventual value of β is selected as to provide low jitter in the DCO output. To alleviate the issue of flickering noise and radiation caused impulse noises, in our proposed model the integral loop factor $\beta = 2^{-18}$ has been activated brusquely once the loop gets settled. In addition to it, in proposed digital phase error detector, at first we accumulate FCW so as to form a digital reference phase Refφ[t]. After estimating Refφ[t] it is compared with the DCO variable phase Varφ[t] that as a result provides the value of digital phase error. In our proposed model, we have implemented the integer phase error detection model and fractional phase error detection model distinctly by means of a phase prediction model that ultimately enhances the overall performance and power efficiency.

The detailed discussion of the proposed ADPLL system is given in the following sub-sections.

1) Digital Phase Error Detection

This circuit primarily functions to generate digital phase error by exploiting phase information of ref_{freq}, DCO clock (Var_{clk}) and FCW. This circuit encompasses two distinct functions, the integer part (on the basis of Var_{clk} cycle counter) and the fractional part (on the basis of TDC) functions. One of the key novelties of the proposed design is the inclusion of the generation of the re-timed reference clock for digital operation for phase error detection. It makes overall phase error detection simple and more efficient with radiation hard frequency synthesis applications.

A brief of the overall digital phase error detection mechanism and associated components is given as follows:

a) Principle of Phase Prediction

Considering the need of a radiation hard, fault tolerant frequency synthesis requirement, to achieve the targeted closed-loop phase noise performance, typically the time resolution of the TDC is maintained in the range of 10– 20 ps [53]. To cover a single unit Var_{clk} time-period with a consistent time resolution, we have designed an inverter-based TDC that functions by introducing significant delay in the Var_{clk} edges by means of a cascaded chain of inverters and performing sampling of their outputs at each rising edge of the reference frequency ref_{freq}. In this mechanism, the sampled digital state encompasses primarily the knowledge about the Var_{clk}-ref_{freq} timing separation of the inverter delay. In practice, such TDC might require sufficient number of flip-flops and delay cells to obtain expected timing resolution. However, introducing delay in Var_{clk} edges by means of chain of inverters might be power consuming as all delay cells perform toggling at relatively higher Var_{clk} frequency. To deal with such issue, we have incorporated a novel phase prediction scheme. An illustrative presentation of the derived phase prediction model to be used in

ADPLL is given in Fig. 5. In Fig. 5, the above lines signify the timestamps of the Var_{clk} and the reference frequency ref_{freq} rising edges, correspondingly. Noticeably, in this illustration FCW is taken as $2\frac{1}{4}$.
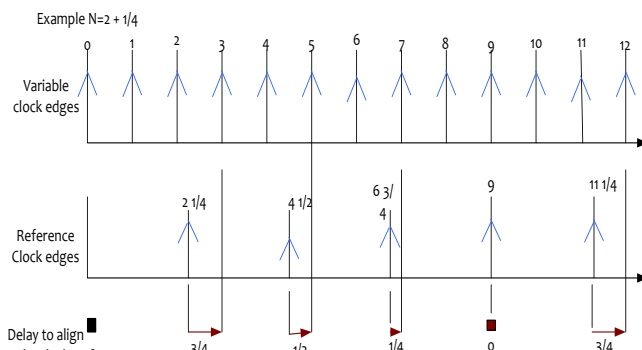
Fig 5. FCW based phase prediction model by estimating phase separation between Var_{clk} edges and the ref_{freq} rising edges

Since, in this method, the fractional FCW is non-zero, the phase difference of the timing difference (or separation) between Var_{clk} edges and the ref_{freq} edge exhibits a periodical pattern of $0, \frac{3}{4}, \frac{1}{2}, \frac{1}{4}, 0$, etc, where the repetition interval is assigned as 4. In the proposed phase prediction model, the edges of reference frequency get delayed in such manner that it is often aligned with the consecutive edge of the Var_{clk} edge. Thus, it enables TDC to cover relatively very small range merely to deal with the phase noise or jitter and errors in the delay control. In our proposed model, ref_{freq} is fed through a DTC unit for generating a delayed form of the reference clock(ref_{freq_D}). In this model, the TDC performs comparison of the ref_{freq_D} edges with the edge of a gated clock, Var_{clk_G}(details are provided in the section b). The illustration of the timing diagram of the phase prediction model is given in Fig. 6.
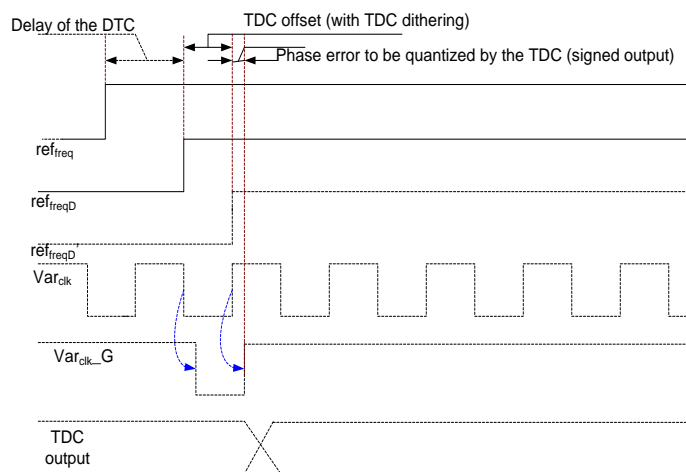

Fig 6. Timing diagram of the phase prediction model

As illustrated in Fig. 6, the difference between the two virtual signals ref_{freq_D} and ref_{freq_D}' is stated to be the TDC offset. In practice, this parameter, (TDC offset as constant) doesn't have significant impact on the phase noise performance. Once, PLL comes in the phase-locked state, ref_{freq_D}' tends to incline towards the next "safe" edge of Var_{clk} or Var_{clk_G}. In this approach certain finer resolution of TDC can also be used to reduce quantization error of the dynamic phase error ($PE_F[t]$). To achieve the total phase error, the estimated value of $PE_F[t]$ is added with integer phase error $PE_I[t]$ which signifies the integer component of the phase error PE. In this case, the total time resolution becomes equal to the resolution of the narrow TDC. Since this approach reduces the need of TDC operating range and therefore multiple high-resolution TDC circuits can be applied without exhausting additional power. It should be noted that with the fractional component enabled situation, part enabled, $PE_I[t]$ equals zero at least for those period when the loop remains in the locked period (say, locked condition) and in this case its allied circuit elements (i.e., the circuit elements of the integer part) could be turned OFF to preserve power consumption. The other advantage of the proposed phase prediction technique is that ref_{freq_D} is employed to perform gating of the Var_{clk} clock before feeding it to the narrow TDC. It enables TDC to operate only on the edges needed for time quantization that significantly reduces power consumption (Fig. 6).

b). Phase Prediction Block

Once reaching the phased-locked state, the normalized time difference between the reference frequency ref_{freq} and variable clock Var_{clk} edges becomes equivalent to $Ref\phi_F$. Mathematically,

$$\epsilon \left\{ \frac{t_{S1} - t_{S2}}{C_p} - Ref\phi_F \right\} = 0 \qquad (3)$$

In (Eqn 1), the parameter ε signifies a statistical expectation factor, and the other variables t_{S2} and t_{S1} state for the timestamps of the Var_{clk} and ref_{freq} edges, respectively. Here, the variable C_p signifies the clock period of Var_{clk}. Now to obtain the expected delay in DTC, Eqn1 can be defined as shown in Eqn 4.

$$[t_{S1} + C_p \times (1 - Ref\phi_F)] - t_{S2} = C_p \qquad (4)$$

The non-zero value of C_p signifies that the edges of the reference signal ref_{freq} are delayed by $C_p \times (1 - Ref\phi_F)$ in such manner that it gets aligned with the consecutive edge of the Var_{clk}, but now with the current edge. This is inevitable to ensure time causality. Now, we have derive a gain parameter called normalized DTC gain is obtained as:

$$G_{nor(DTC)} = \frac{\Delta d_{(DTC)}}{C_p} \qquad (5)$$

In above expression, $\Delta d_{(DTC)}$ signifies the step size of the LSB delay in the DTC, and thus the expected DTC can be obtained as (6)

$$EXP_{DTC} = \frac{(1 - Ref\phi_F)}{G_{nor(DTC)}} \qquad (6)$$

In our proposed model, the integer component of the estimated is fixed-point EXP_{DTC} is applied for DTC control, where $(1 - Ref\phi_F)$ is obtained by means of bit inversion. To further enhance the performance the value of EXP_{DTC} can be obtained by:

1. Dithering into the integer component by means of a digital $\Sigma\Delta$ modulator by ensuring TDC resolution $\Delta d_{(TDC)}$ equivalent to the DTC resolution $\Delta d_{(DTC)}$;

2. Converting EXP_{DTC} into residue and adding it to the TDC output in case the resolution of TDC is much narrower than the resolution of DTC.

In first approach, performing dithering of the fractional component of the targeted DTC delay of EXP_{DTC} to the integer control can significantly minimize the impact of the DTC quantization noise by means of quantization noise shaping to the high frequency. Consequently, it can be vital for fault tolerant ADPLL design as the proposed digital loop filter enables better attenuation of the rad-hard noise components. It contributes a significant novelty and fault resiliency in those scenarios when DTC quantization noise is not treated properly.

c). Var_{clk} *Gating and* ref_{clk} *Generation*

In our proposed ADPLL design (Fig. 4), the key components such as the reference phase accumulator, edge prediction unit, digital loop filter etc, are clocked by means of ref_{clk} and continues running on reference frequency f_{Ref}. ref_{clk} is edge-synchronized with the Var_{clk} edge. In order to generate ref_{clk} clock, a simple approach can be to perform sampling of the reference clock with the Var_{clk} clock. However, this mechanism can have a few intricacies. These are:

1. Since the edges of Var_{clk} clock are not synchronized with RREF, performing direct sampling might cause the generation of the meta-stable outputs, even though performing sampling at the exact edges of the reference clock.

2. Though, the results of ref_{clk} toggle once after detecting edge of each reference signal, and hence the sampler is required to be clocked at relatively higher Var_{clk} frequency. This as a result can cause excessive power exhaustion.

Observing above problems, the first issue can be resolved by sampling reference clock using two distinct and parallel flip-flops which could be triggered as per falling and rising edges of the Var_{clk}. Additionally, selecting the output the output bit

(spatially) away from meta-stability by means of applying certain arbitration signal from TDC [26] can help in alleviating the aforesaid problem. Undeniably, it can help in achieving meta-stability-free functions; however at the cost of increased hardware complexity and power exhaustion. Now, considering second issue, the unwanted energy exhaustion can be minimized by turning off the ref_{clk} circuit in between the edges of the timer circuits and the reference clock. Unlike the above mentioned approaches, our proposed method performs ref_{clk} generation gating automatically by means of a delayed reference clock running at the reference clock rate. Our proposed model doesn't encompass any supplementary circuits that eventually reduces hardware complexity, power consumption as well as alleviates the problem of meta-stability. An illustration of the proposed ref_{clk} generation model with connected TDC gating is presented in Fig. 7.
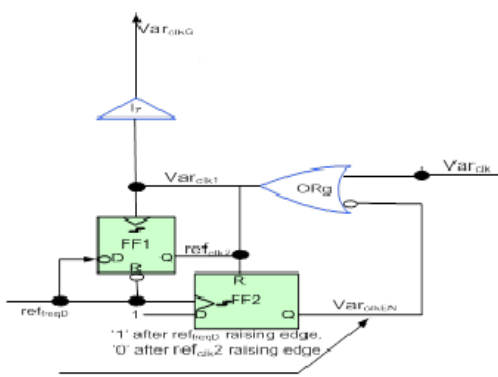
Fig 7. ref_{clk} generation model with connected TDC gating
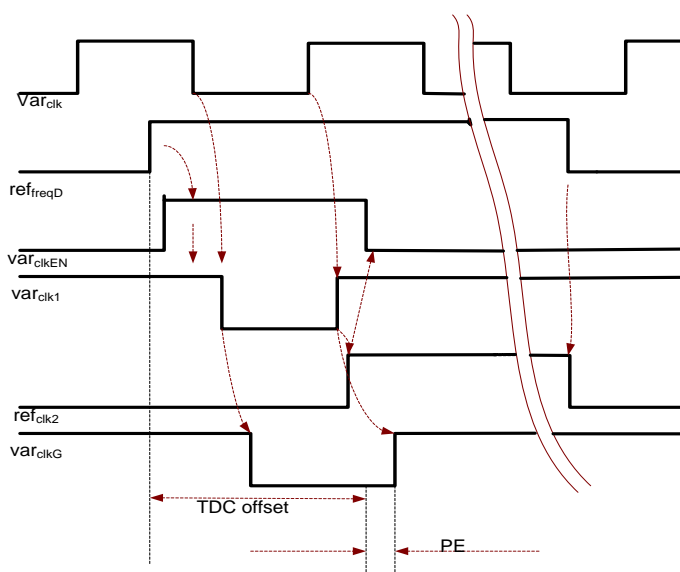
Fig 8. ref_{clk} generation and clock gating circuit

As depicted in Fig. 7, the components FF1 and FF2 represents the flip-flops which can be reset asynchronously, I7 represent controlled buffer. Now, considering the timing diagram Fig. 8 until the occurrence of the rising edge of ref_{freq_D}, $Var_{clk_{EN}}$ remains low and the OR gate (ORg) is initially disabled so as to maintain Var_{clk_1} high. Especially, at the rising edge of ref_{freq_D}, $Var_{clk_{EN}}$ turns out to be high thus permits Var_{clk} edge to cross ORg and therefore the first rising edge of the Var_{clk} after the ref_{freq_D} causes a rising edge at Var_{clk_1} and then triggers FF1 thus creating a rising edge on ref_{clk_2}.

In subsequent process the rising edge of ref_{clk_2} resets FF2 that makes $Var_{clk_{EN}}$ to low state.

Similarly, the falling edge of ref_{freq_D}, resets FF1 to give rise to a falling edge at ref_{clk_2}.

In our proposed design ref_{clk_2} is re-timed two times by dividing Var_{clk}. Stating mathematically, the time gap or the delay in between ref_{clk_2} and Var_{clkG} is $\geq 8 \times C_p$, which is sufficient for TDC to decide the fractional component of the phase error (PE$_F$[t]), and thus phase error (PE[t]). Here even the small phase noise introduced by impulse signal due to radiation effect can be corrected. Thus making it suitable for space bound applications.

Similarly, in next instance once detecting the rising edge of ref_{freq_D}, the rising edge of the Var_{clk} emerges at Var_{clk_1} and is buffered for generating the Var_{clk_G} and this process continues.

This as a result enables comparing of Var_{clk_G} and ref_{freq_D} at the reference rate. The total difference between these two quantities comprises of two parameters namely: TDC offset and Phase error (PE).

This enables our proposed model to be well suited for major real-time application environment, especially space radiation environment.

Undeniably, to achieve fault tolerant radiation-hard ADPLL design enhancing TDC is of paramount significance. A brief of our proposed TDC unit is given as follows:

b) Time-to-Digital Converter (TDC)

An illustration of the applied TDC unit is given in Fig. 9. As stated, the fractional component of PE$_F$[t] is obtained through quantization of the time difference in between ref_{freq_D} and Var_{clk_G} edges. As shown in Fig. 9, ref_{freq_D} gets delayed by the string of inverters or buffers, whose outputs are sampled with the rising edge of the gated Var_{clk} clock (Var_{clk_G}).
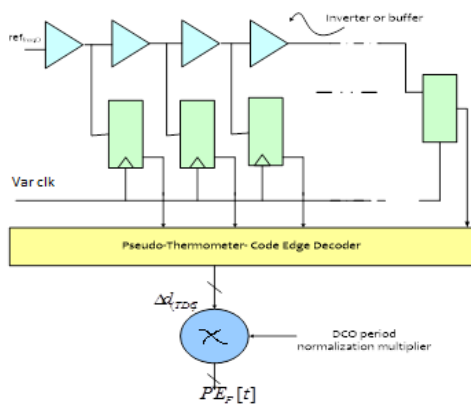
Fig 9. TDC Structure

In this manner the output of the TDC core constitutes an positive edge detection model, which is further converted to binary. The output of TDC $= ref_{freqD} - var_{clkG}$ and the phase error component PE[t] = TDC – TDC offset and is normalised with the DCO period via the loop gain multipliers, to minimize hardware complexity.

2) Digital Loop Filter (DLF)

In our model the TDC unit function doesn't cause any reference spurs that eventually enables digital loop filter to be calibrated at the best performance point in between the noise components (i.e., reference phase noise and oscillator phase noise). It strengthens our proposed model to exhibit better filtering even at 1st or 2nd order. On contrary, PLLs require minimum 3rd order filtering to give equivalent result. On contrary, in radiation-hard environment it might require even more sharp filtering approach which might seem impractical with traditional PLLs. In our proposed ADPLL design, a digital loop filter encompassing phase error combiner unit, cascaded 4th order IIR filters with distinct filtering coefficient $(\varphi_1 - \varphi_4)$ is applied (Fig. 11). In addition, it contains path loops gain coefficients, β (proportional path) and δ (integral path).
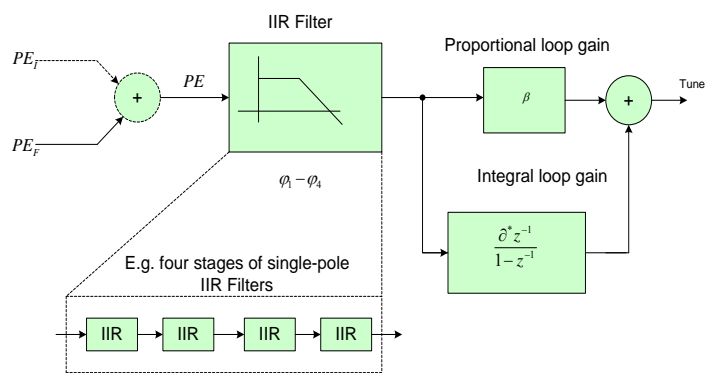
Fig 10. Digital loop filter

As depicted in Fig. 11, our proposed phase error combiner model combines both PE_F as well as PE_I components to estimate a complete error PE. Though, it can be accomplished by

means of applying a binary adder, we find that the it can be applied as a multiplexer so as to select PE_I during loop acquisition and PE_F once loop is in locked condition. The IIR filter under consideration follows the following expression (7).

$$q_i[t] = (1 - \varphi_i) \cdot q_i[\varphi - 1] + \varphi_i \cdot p_i[t] \qquad (7)$$

where the variables $p_i[t]$ and $q_i[t]$ represents the inputs and outputs, correspondingly. Here, i represents each stage while φ_i presents respective coefficient value. In fact, in this manner the proportional and integral components are arranged in parallel manner that eventually forms a PI controller. Here, IIR filter processes the PI controller that intends to improve the transition band rejection of the filtering characteristics of our proposed ADPLL design.

3) Digitally Controlled Oscillator (DCO)

Undeniably, DCO is considered as the heart of the ADPLL, which functions on the basis of an LC-tank having (-) resistance so as to enable oscillations, in the similar way as performed by VCO (Fig. 12). Unlike traditional variable capacitor based VCO, DCO uses a number of binary-controlled varactors (Fig. 13) which could be set in either low or high capacitive state. As the input of DCO are usually controlled digitally, and as the varactors (i.e., DCO input) are digitally controlled and the output clock at multi-GHz frequencies is extensively applied shape of the digital waveform in DCO, which corrects its phase and frequency, can be called as fully digital [54].
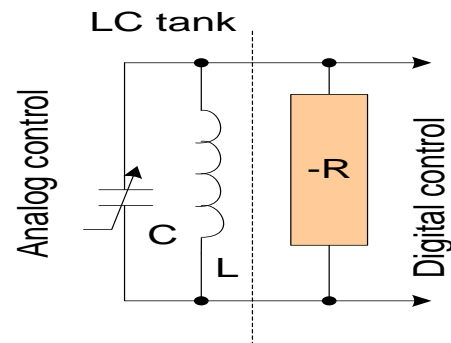

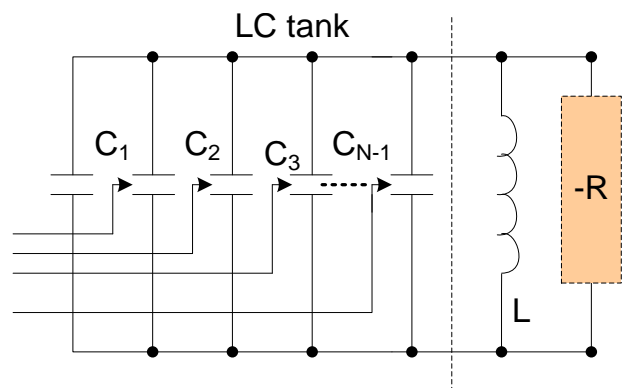Fig 11. Traditional Voltage Controlled Oscillator

Fig 12. Digital Controlled Oscillator

It should be noted that the negative resistance in Fig. 13 signifies perpetuations of the resonance of the lossy LC tank. The smallest size of the varactor step is in the order of 40 pF. It corresponds to the frequency step size of 12 kHz at 2.4 GHz DCO output. However, in practice such type of fine control is not suitable for any application, particularly in those applications where there can be the possibility of space radiation. Therefore, to alleviate such limitations dithering is performed which enhances the time-averaged capacitive resolution. Since, in this paper, our intent is to develop a robust and efficient ADPLL based frequency synthesizer with reference frequency 20 MHz and targets frequency of 2.4 GHz, and therefore, our proposed ADPLL model (Fig. 14) obtains the low and high band cellular frequency through dynamic edge dividers. In our proposed model, the tuning control is divided in multiple banks with different or varying frequency step size. In proposed DCO architecture, the oscillator phase noise has been controlled by means of the current dissipated, which has been arranged with the help of a 7-bit "bias" control. Further, to alleviate the possibility of biasing current sources, we proposed to implement T_0 transistor array that can function in linear region rather than in saturation. Here, the current can be defined by means of automatic calibration at certain least possible value at which the oscillator generates RF phase noise in acceptable range. An illustration of the preventative oscillator core and varactor state is given in Fig. 14.
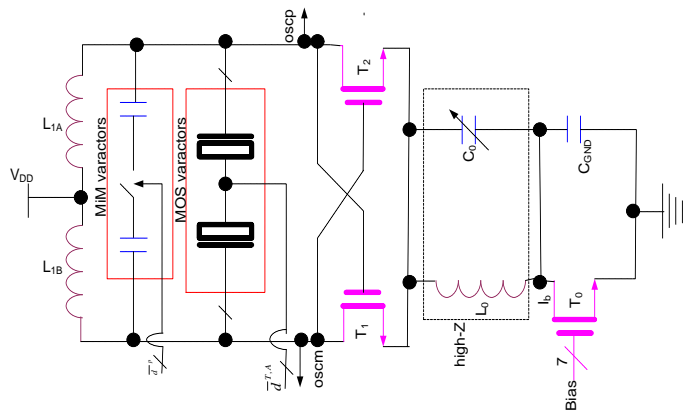
Fig 13. Oscillator core and the array of varactor state

C. RESULTS AND DISCUSSIONS

In this paper a robust radiation hardened ADPLL design was developed for high frequency space communication applications. The overall proposed FDLC ADPLL model was developed for frequency synthesis purpose where the reference frequency was fixed at 20 MHz, while the synthesis frequency was maintained at 2.4GHz. In the proposed system, the delay resolution in DTC (i.e., $\Delta d_{(DTC)}$) of 15 ps is selected.

A snippet of the test simulation and results obtained is given as follows in Table III.

Table III. Results of FDLC-ADPLL

Sl No.	Parameter	Simulated Results	Specification
1	Input Frequency	20MHz input	20MHz+/-5MHz
2	Output Synthesized Frequency	2.4GHz	2.2GHz-2.5GHz
3	TDC resolution	15ps	20ps
4	Loop Filter Type and Order	4th Order ,IIR Filter	3rd Order
5	Settling Time	60us	<100us
6	Power	371.7mW	
7	Cycle to cycle jitter	312ps	250-350ps
8	Period Jitter	256ps	250-350ps
9	Impulse Noise	20ns, 1mV input	
10	Settling time with noise	105us	<100us
11	Cycle to cycle jitter in presence of impulse noise	340ps	250-350ps

The reference frequency, DCO outputs and the phase error outputs are illustrated in Fig. 14, Fig. 15 and Fig 16. respectively. Results reveal that the total phase error reduces and reaches to zero that makes instantaneous DCO frequency to reach targeted 2.4 GHz. The phase error obtained in our proposed predictive PFD is presented in Fig. 15. Now, observing the results (Fig. 14, Fig. 15 and Fig. 16), it can be easily observed that the proposed ADPLL design reduces the error soon before 50 us (Fig. 16).
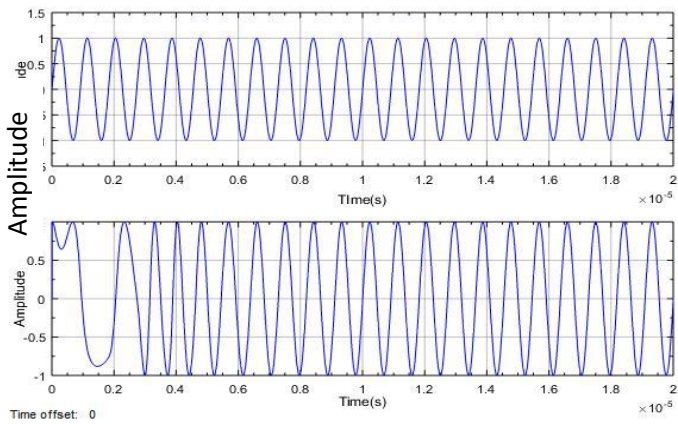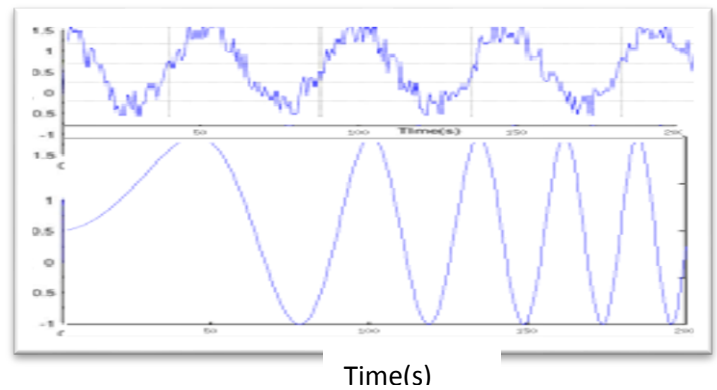
Fig 14. Reference frequency and DCO output

Fig 15. Phase-error between reference ref_{freq} and ref_{clk}

Fig 16. Settling time of output

When the ADPLL is simulated in presence of impulse noise of 20ns and 1mv added at the reference as shown in Fig 17, the settling time obtained is shown in Fig 18.

Fig 17. Reference frequency and DCO output in presence of noise
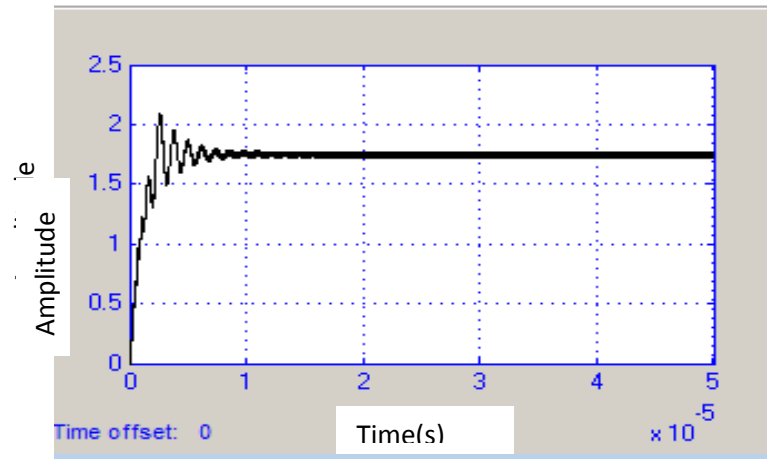
Fig 18. Settling time of output with radiation induced impulse noise
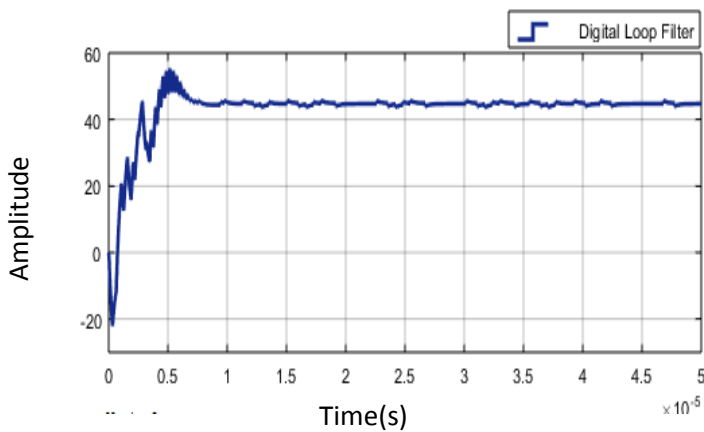
Here, it can be found that after 60 us, the integer phase error becomes zero and the ADPLL is controlled by fractional phase component or path.

In addition, we have assessed our developed ADPLL architecture in terms of complementary cumulative distribution function (CCDF) that signifies the probability of the instantaneous power level of a single above the signal's average power. Fig. 19. reveals that the obtained DCO signals there is the probability of 0.0001% of the signals to have the instantaneous power more than the average.
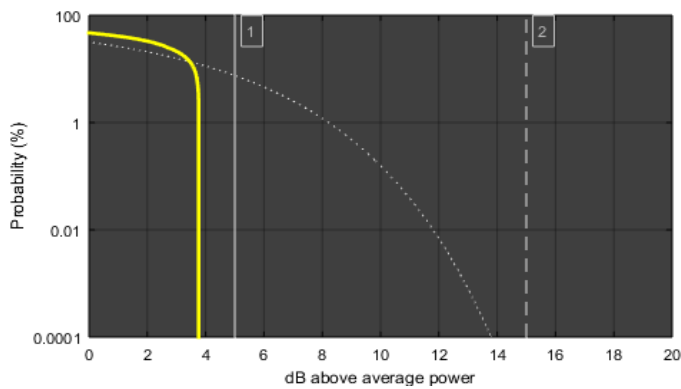
Fig19. CCDF performance by proposed ADPLL DCO signal

Thus, the overall results have demonstrated that the proposed FDLC-ADPLL architecture can be a potential fault tolerant solution to be used in high frequency, radiation hard by design "digital frequency-synthesis" applications where it has resulted in minimum power consumption of 371.7mw, low jitter of 340ps and less locking period of 105us in the presence of 20ns, 1mV radiation simulated impulse noise.

D. CONCLUSION

In this work, unlike traditional feedback divider based ADPLL an enhanced Feedback-Divider Less Counter based ADPLL design was developed. The design has been tested for frequency synthesis with the reference frequency of 20MHz and the synthesis frequency of 2.4 GHz. The simulation results has revealed that the proposed Rad Hard ADPLL design can be a potential solution for space communication systems by maintaining low jitter of 340ps and power consumption of 371.7mW, as the narrow range TDC designed can detect sample radiation induced impulse noise of 20ns, 1mV and correct it . Further fine tuning will be done in the design to meet the listed specifications.

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