Low power CMOS based Self Controlled Pre-charge Free Content Addressable Memory with Minimum area for Image Processing Devices

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***Abstract*—**Image processing devices plays a vital role in several applications like medical, security, biometric etc. The devices ranges from portable size to larger machines with and without Human Computer Interface possibilities. As the image processing and human computer interface system application requires higher memory requirements, the power and area should be small. Searching of data is a high priority work in image classification. To perform high speed search through hardware Content Addressable Memory is used. But the circuit suffers from higher power consumption, precharging issues and low performance. For longer word length the elimination of precharge is needed. So for high speed applications self-controlled precharge-free CAM (SCPF-CAM) is suitable. A 4T hybrid self controlled pre charge free Content Addressable Memory is proposed in this paper using CMOS 32nm technology. The observation shows that the circuit works at high speed, minimizes the search time and has high performance operation. When compared to the conventional SCPF-CAM, 8T CAM the proposed design reduces the number of transistors. The reduction in area is about approximately 20% and can be used in low power and low energy applications. In Synopsis HSPICE Predictive technology models were used for the implementation in 32nm CMOS technology. The work will be extended in future using FinFET technology where the leakage current can be minimized.

***Keywords*—**CMOS, Search line, Static Random Access Memory (SRAM), Low power, Self Controlled Pre-Charge Free –Content Addressable Memory (SCPF-CAM), high speed.

I. Introduction

Image processing applications used in real time works faster when compared to other systems. The storing, analysis and transmission of data is the major processing done. Memories are the key elements to perform the functions. Content addressable memory is mainly used in internet for packet forwarding with high performance which will give the accurate results in a single clock cycle [1]. It implements look up table function. CAM is also a memory to store and retrieve the data; this can be done with the help of a storage and compare unit as shown Fig.1. The use of a compare unit is that in SRAM the address of the stored data is given directly to retrieve the data but in CAM the same data can be stored in several memory cell that all addresses can be retrieved easily by comparing the search data with that of the stored data.CAM is mainly used in applications like longest prefix matching, network router, radix tree, 5G Communication network, etc.,

In CAM data storage can be of row wise manner and the search operation is of parallel .Mainly the data storage is through bit line and the search operation through search lines. For each row Match Line will be connected to identify the match of data. The challenging task in designing the CAM is that the high performance with low power consumption [2]. The search operation of CAM can be done with the help of pre-charge of match lines, so that the power dissipation is high. Here the search operation will give the result as hit or miss, if the data is not matched then the ML should be dropped to ground [3]. This will increase the dynamic power dissipation of CAM since the dynamic power plays a vital role in total power dissipation, overall power dissipation is high.

Another drawback of the conventional Cam is that the frequent switching of ML causes the switching power to increase. This switching can avoided by the segmentation of words into several small words or the Master –Slave architecture can be implemented so that the first segment or master is matched then only the remaining part is involved in the search operation [4]. The next invention to reduce the drawback of the above method is that the Pre-Computation in which each stored word is having parity Bit and search starts with the matching of parity bit of both stored and search word if it matches then the original word can searched otherwise the process can be stopped there itself [5]. The method neither is having a drawback of short circuit current of NOR type cell. This can be eliminated by using the Pre-charge free CAM, here the short circuit current problem of NOR and charge sharing problem of NAND is avoided but the memory cell dependency will create the performance degradation. In Self Controlled Pre – Charge free CAM, Control Bits are omitted and efficiency also increased but the power consumption is getting increased.

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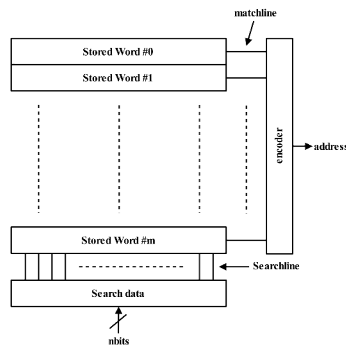


Fig. 1 Basic CAM Architecture [1]

In CAM, Random Access memory (RAM) is mainly used for storing the data. In this the data can be read or write roughly with same amount of time regardless of the order of the data. In direct access data storage media, the time required read and write operation can be varied based on the location where the data has to be stored due to some mechanical limitations.RAM is volatile memory there is some challenges while it is designed as non-volatile such as write operation cannot be performed randomly. In recent days high speed and low energy memories are in demand and flash memory has been replaced by new memory devices so that the programming time and energy is improved a lot [6]. In some memory Storing techniques can vary such as the magneto resistive random access memory (MRAM) depends on the orientation of magnetic moment in a magnetic tunnel junction (MTJ).It consists of magnetic layer with tunneling barrier in between, if the orientation on both layer are same then the junction in low resistive state (LRS), Otherwise it is in High Resistive State (HRS).The programming of memory can be done in the following manner. Spin-transfer torque (STT), spin-orbit torque and voltage-controlled magnetic anisotropy (VCMA) effect [6]. If the programming done on MRAM with VCMA effect called magneto-electric RAM (MeRAM). In Resistive RAM (ReRAM), storage of data is done by growing a conductive filament; here the resistance value can be either low or high depends on the conductive path present or absent.

The phase change RAM (PCRAM) can store the data according to the structure as crystalline or amorphous, if it's a case resistance state changes can also depends on structure of the material. Scaling can affect the resistive memory for example resistance value is inversely proportional to the area. So the reduction in area increases the resistance value of the memory. Thus increase in resistance results in longer read time and smaller read current. There may be a chance of increase in tail bits (i.e.) devices at the edge of distribution. Till now we saw about the way of designing 4T SRAM by using different techniques. But with the help of SRAM only CAM can be designed. In CAM there are two types of architectures.

- NAND type architecture
- NOR type architecture

In NAND type of architecture the speed of operation is low but the power consumption is also low. But in NOR type of CAM architecture performance is good with high power consumption. Section II deals with the related work on 4T SRAM and Sections III deals the conventional CAM. The proposed method of CMOS based CAMs are described in Section IV. The simulation results of the conventional and proposed CAM architectures are described in Section V. Section VI ends with the corresponding conclusion.

II. Conventional 4T SRAM

A. Loaded 4T-SRAM Cell

The loaded 4T SRAM consists of four NMOS as drive and transfer gate and also contains two load elements to hold the data as shown in Fig. 2. Initially the bit lines are pre charged to VDD but the node level during READ/WRITE operation will be slightly reduced from high, by a threshold voltage of the transfer transistor. Since the cell is selected the transfer gate acts as a source follower circuits. The current used in this design is in the order of pA since the node level raises to VDD once the transfer gate get closed. Due to the above mention reason the cell is not stable for noise [7]. The cell size used for this design is more because the cell ratio selected should be more than 6.5 at 2.5v.

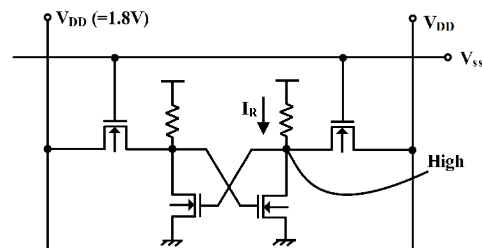


Fig. 2 Loaded 4T-SRAM [7]

B. Loadless 4T-SRAM Cell

The supply voltage used in this design is 1.8v, drive transistor is made with the help of two NMOS. The transfer transistor is made using two PMOS as shown in Fig. 3. Advantage of using PMOS in Loadless 4T SRAM is that the node level can be raised to VDD right after READ/WRITE operation. The PMOS itself will act as a load element which is in OFF condition, during this standby cycle the bit lines also raised to VDD. The condition for retaining the data without any refresh cycle, is that the offset current of NMOS (Ioff-N) should be lower than that of PMOS (Ioff-P) even though the bias at the source drain of NMOS is set as 1.8V & for PMOS less than 0.1V.

The threshold voltage assigned to NMOS is 0.25V higher than normal but the PMOS is designed with normal threshold voltage.[7] The sub-threshold characteristic shows that the offset current for NMOS operated in saturation region at VDS=1.8V is lower than that of PMOS working in linear region at VDS=0.05V by two orders of magnitude. If the gate bias voltage is 0V then the band-to-band tunneling current and the leakage current at the junction are negligible.

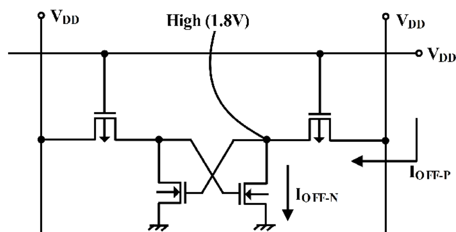
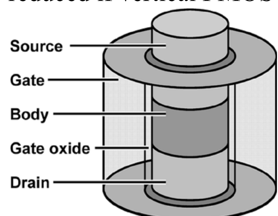


Fig. 3 Loadless 4T-SRAM [7]

C. *Stacked Vertical PMOS 4T SRAM Cell*

From Fig .4 drain and source is formed as cylindrical in shape and the channel region between those two terminal formed by a body and it is made of poly-silicon [8]. Here the body is surrounded by a gate of the transistor, so that the width of the channel is getting large. The voltages at the gate-source and drain-source are equal to -1.8V and the drive current is 20μA at 25˚C.

From the above current and voltage it is assumed that the vertical PMOS can be used as load element in 6T SRAM and transfer MOSnin 4T SRAM cell [8].The vertical PMOS (Fig. 4) is stacked over bulk MOS so that the cell size of 6T and 4T is reduced if vertical PMOS is used.



Channel width	1.0 μm
Channel length	0.3 μm
Gate-oxide thickness	5.7 nm

Fig. 4 Vertical poly silicon PMOS structure [8]

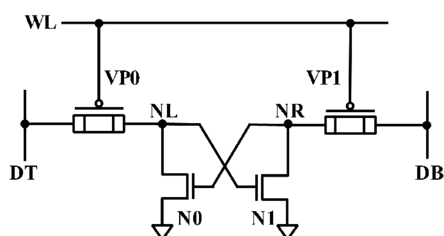


Fig. 5 4T SRAM using stacked vertical PMOS [8]

The stacked vertical 4T SRAM is having bulk NMOS as (N0 & N1) and vertical PMOS (VP0 and VP1) as described in Fig. 5.The data lines can be driven by the driver MOS transistors and the connection between the data lines and storage nodes can be laid by the transfer MOS. The transfer MOS VP0 and VP1 can be used as load element so that the design doesn't have a load element.

D. *Electric Field Relaxation Scheme*

Here the leakage current requirements of vertical PMOS and BULK NMOS can be discussed as shown in Fig. 6, in which the vertical PMOS can be connected to both high voltage(VPH) and low voltage(VPL). The leakage current can be represented by IVPH when connected to high storage node and IVPL at low storage node. The data stored in the SV4T cell can be retained with the help of IVPH without the use of refresh operation. The condition to be satisfied for keeping the high storage node near the stable data-line voltage is that at Vds=0.1V, the off current of the vertical PMOS (Ioff, Vp) should be greater than two orders of magnitude than the sum of the off current (Ioff, N) at Vds=1.7V [8] and gate-Leakage current (Ig, N) at Vgs=1.7V and Vds=0V of NMOS.

The cell leakage current can be calculated by the addition of both IVPH and IVPL. This condition will increase the IVPL so that the cell leakage current can be increased. The leakage current is minimized by suppressing the Ioff, N, Ig, N. The offset current depends on the subthreshold leakage current and the gate induced drain leakage current which in turn the sub threshold current can be reduced by using high threshold voltage for bulk NMOS. But the tunnel-leakage can be reduced by optimizing the device parameters. In order to overcome this problem the SV4T cell with Electric field relaxation technique can be used.

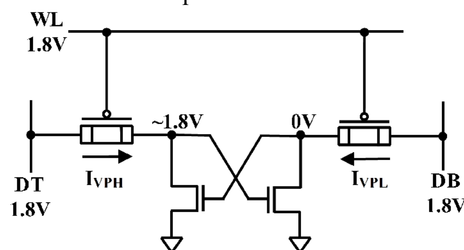


Fig. 6 Leakage currents [8]

E. *Methods of Reducing Leakage Current*

From Fig. 7 it is observed that the GIDL and the gate tunnel leakage are reduced to reduce the leakage current. But the GIDL depends on drain gate voltage [8] and the gate source voltage which in turn has an impact on gate tunnel leakage current.

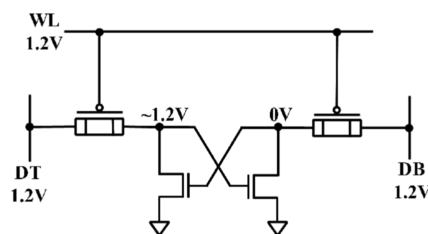


Fig. 7 EFR scheme [8]

The voltage at the high storage node should be maintained near 1.2V by keeping data line voltage at 1.2V.The voltage of the VPH and VPL can have the same level when the line voltage is at 1.2V. Once the high storage node reaches 1.2V the Vdg of NMOS at VPH node and Vgs of NMOS at VPL node are getting decreased. So that the adopted method reduces the cell leakage to 88.7fA which is 90% lower as compared with conventional method.

F. *Dual Word Voltage Scheme*

The dual word voltage scheme is developed to solve the

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problem of retention of data in the SV4T cell. The data retention can be lost due to the voltage drop in the vertical PMOS. In the scheme, while read operation before the activation of word line, the data line should precharged to 1.8V. The body voltage which acts as a transfer MOS is now floating at the same time the body voltage is lowered to 1.2V by making VWL as 0V from 1.8V.

The reduction in body voltage results in a reduction of equivalent resistance. The equivalent resistance ratio is decreased which can be given by the ratio of equivalent resistance of VPL to the equivalent resistance of bulk NMOS which is connected with low storage node.It is clear that the read operation is very difficult in SV4T cell as compared to write operation . This can be overcome by DWV techniques.

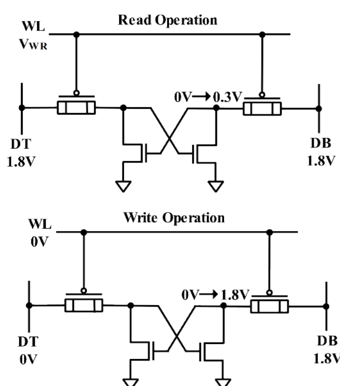

Fig. 8 DWV Scheme [8]

Here the word line voltage which is selected should be set to the value higher than 0 during read operation and during write operation the voltage should be 0V as shown in Fig. 8. In read operation the increase in word line voltage reduces the source gate voltage of the VPL so that the equivalent resistance and ratio are getting increased. At the same time Vsg of write operation is larger than that in read operation and equivalent resistance is smaller in write operation so that the write time is small.

G. 4T SRAM with Low Dynamic Power

In this design Fig. 9 a pair of bit line and two word line are used , during read/write operation ,the dynamic power can be reduced with the help of reduction in swing voltage and the read and write operation performed on opposite sides of the design [9].

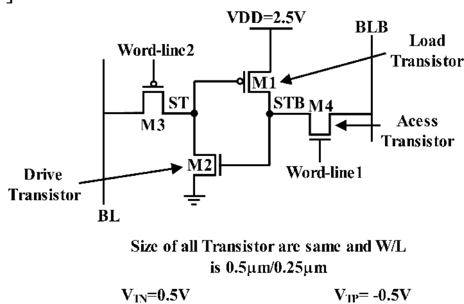

Fig. 9 4T SRAM [9]

In the Fig. 9 the stored bit is ‘0’ then both the driver and load transistors are in ‘ON’ condition. Now the feedback occurs between ST and STB node so that the ST node automatically pulled down to GND by driver transistor and STB node raised to VDD by load transistor.

$$I_{off\ NMOS\ access} \geq 3x(I_{DS\ Load} - I_{G\ Driver}) \qquad (1)$$
$$I_{off\ PMOS\ access} \geq 3x(I_{DS\ Driver} - I_{G\ Load})$$

The above said condition to be satisfied when bit ‘1’ stored in memory cell, the threshold current of access transistor to be taken into account. During Idle mode BL to be grounded the word-line to be maintained at respective idle voltage. The condition to be noted for retaining the data is leakage current [9], here the leakage current of access transistor is sub-threshold since the transistors are maintained at sub-threshold condition.

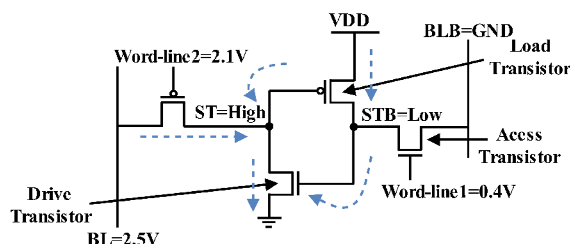

Fig. 10 4T SRAM in IDLE mode [9]

The idle voltage at wordline1 and 2 should take the value of 0.5V & 1.8V when bit ‘1’ is stored as shown in Fig. 10. The write operation involves the following steps as,

- Bit-Line driving
- Cell-Flipping
- Idle mode

The read operation involves the following steps as,

- Bit-Line pre charging
- Word line activation
- Sensing
- Idle node

H. Robust Multi VT SRAM

The un-doped ultra-thin fully depleted silicon-on-insulator architecture with high k-dielectric and metal gate is mainly used reduce leakage current and intrinsic variability. The device matching can be improved with the help of narrow MOSFET and silicon film scaling. The buried oxide layer can induce the isolation of the substrate so that the sub-threshold slope and the short channel effects are improved. The multi Vt device can be designed effectively by reducing the thickness of the Box and the ground plane (GP) integration.

The back gate technique is used to improve the electrical characteristics of SRAM cell. The drawback behind the optimization of stability by integration the feedback at cell level is due to the back gate contact implementation and GP isolation. Dual Box approach depends on the integration of the thin and thick Box by the complex substrate fabrication process flow with oxygen implant or wafer bonding. The Vt modulation can be improved by the back gate biasing &

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thinning of Box method in FDSOI devices. The Box oxide thickness can be increased by the extension of depleted zone under Box. It reduces the SCE and DIBL. The DIBL [10] and SS can be improved by integrating the GP so that the depletion can be reduced. Three device characteristics can be identified as i)an increase of VT ii) a quasi-constant VT iii) a reduction of VT.

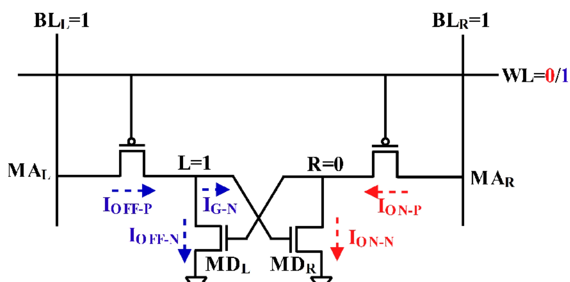

Fig. 11 Load-less 4T SRAM [10]

Consider the high logic level; the supply voltage is directly connected to the BL & WL during retention period as depicted in Fig. 11. The L node is maintained at VDD by the leakage current in ML. The process fluctuations can be handled easily by keeping IOFF-P to be one hundred to one thousand times higher than IOFF-P and IG-N at retention state. BL is pre charged to VDD & left float during read operation, to access the data the WL is grounded. The IOFF current of MA transistor should be higher than MD to obtain good stability during retention & read mode.

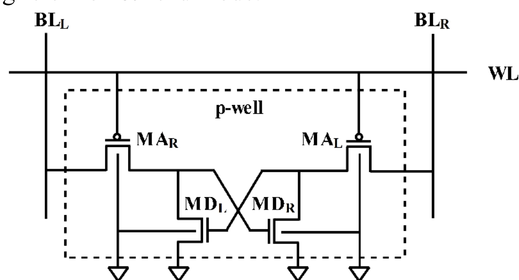

Fig. 12 Multi Vt 4T SRAM [10]

Here in Fig.12 the GP doping is used in the design and the back gate is connected to the ground here MA is having low-VT and MD with high VT.

III. Conventional CAM

Content Addressable Memory consists of Memory cell made of 6T SRAM for storage and also the compare unit to compare the stored word and the search word. Based on the comparison unit CAM classified as NOR CAM architecture and NAND CAM architecture.

A. Robust Multi VT SRAM

Here the NOR type CAM cells are connected in parallel manner. In NOR type architecture two pairs of NMOS are connected in series to form the comparison unit[11], in which one pair of transistor is connected to the bitline (bitlinebar) and another pair is connected to the stored data D(Dbar) as shown Fig. 13.

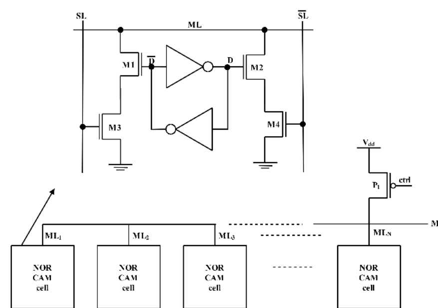

Fig. 13 NOR type ML CAM

The operation is separated into precharge and evaluation phase, in precharge phase the PMOS connected to the MAT is given a LOW signal so that the MAT will be charged to HIGH and the second phase Evaluation in which the search operation is initiated if the data stored and data in search line is matched the MAT retains the same state HIGH otherwise the mismatch occurs the MAT automatically drops to zero by either pair of transistors.

In this series connection if any one of the bit is mismatch then the whole ML drops to zero once again ML should be precharged for the next search operation so that the power consumption is high since the ML capacitance plays a vital role in the power consumption. The power consumption of NOR match line architecture is given in (2). The delay of NOR type CAM cell is expressed in (3).

$$P_{NOR} \alpha (N-1).C_{MLNOR} V^2{}_{DDNOR} \quad (2)$$

$$\text{Delay} = T_{DNOR} + t_{RC} \quad (3)$$

Where, T_{DNOR} =Delay of one transistor to identify the match and tRC is the RC time constant. In NOR type ML the power consumption is high and also the short circuit current problem occurs.In match condition the current for pre charging and evaluation is minimal but during mismatch the power consumption of pre charge is higher than the evaluation phase that too depends on number of bits mismatch [11].

B. Robust Multi VT SRAM

Unlike the NOR CAM cell in this technique NAND CAM cells (Fig. 14) are connected in serial manner and inside the cell, a pair of NMOS connected serially whose gates are connected to the data storage node D and DB at the same time the source of each gate is given an input of search bit and the drain is connected to gate of another NMOS link with the ML[11].In this method also ML initially pre charged to HIGH and when all the bits of the word matches then ML retain the charge if any one of the CAM cell mismatches then the nmos pass transistor does not allows the previous bit output to the next bit since it will be in OFF mode.

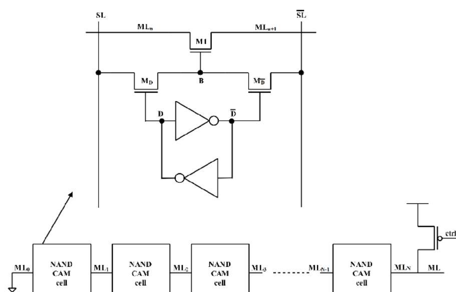

Fig. 14 NAND Type ML CAM [11]

The power consumption of NAND type ML architecture is low as compared to the NOR type ML. It is given in (4). In terms of power consumption NAND type consumes low power but with high Delay (5) since it discharges through K transistors and t_{RC}. NAND type CAM cell is having large Delay so that it is not selected for larger word length and also it is having charge sharing problem so it is chosen for smaller word length alone.

$$\text{Power} = C_{ML} + V^2 V_{DD} \quad (4)$$

$$\text{Delay} = K(T_D + t_{RC}) \quad (5)$$

C. Pre Charge Free CAM Architecture

In conventional CAM pre charging the ML plays a major role in increasing the power consumption and limiting the speed of search operation. In order to avoid this situation, Pre charge free CAM is designed as shown in Fig.15.

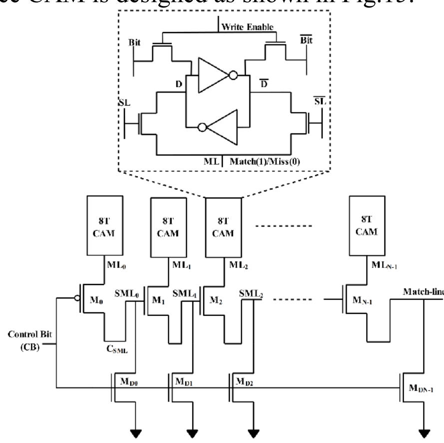

Fig. 15 PFCAM architecture [11]

Here the short circuit current problem of NOR type CAM can be avoided by resetting the ML at every search operation. In the above circuit control bit and the pull down transistors are introduced for this purpose only. Initially the control bit is set to zero before initiating the search and once the first bit of the word matches then ML0 becomes HIGH to make the M0 to saturation and SML0 also goes to HIGH and the second bit is compared if it matches ML1 becomes HIGH otherwise SML2 leads to ZERO so the operation stops there itself any how the remaining bits matches or mismatches. By using this method will create a false matching in some cases, there we can use the pull down transistors to reset the ML between two successive search operation by making control bit to HIGH. The total capacitance needed for charging after the search bit applied to CAM is given in (6).

$$C_S = MC_{SML} \sum_{i=1 \text{to } N} (1/2)^i \quad (6)$$

Where, C_{SML}=capacitance of segment which charges if it matches, M=number of words in the CAM, From the above equation the total capacitance depends on the number of words rather than the number of bits C_S=MC_{SML}.

D. Self Controlled Pre Charge Free CAM Architecture

The pre charging of ML will create a problem of increasing the power consumption, in order to reduce the power consumption, pre charge can be avoided in Pre Charge Free Content Addressable Memory so the number of SC path is getting reduced and the overall power is also reduced. But the CAM cells are cascaded in PFCAM so the dependency decreases the speed of operation [12].To increase the speed of operation SCPF CAM is designed, this design is mainly for longer word length at higher frequency of operation with high performance. The control Bit in PFCAM is eliminated so that each CAM cell in this design directly give the output i.e match or miss which don't want to depends on the previous output. The produced output of the cell is connected to ML through the buffer. The SCPF is made of 8TCAM cell as shown in Fig. 16 which is designed as such NAND CAM cell except the pass transistor which is eliminated. The output of 8TCAM cell is either S=1(match) or s=0(miss) and connected to buffer, buffer contains one NMOS and one PMOS. If s=1 NMOS is in ON condition so the output s=1 is directly connected to ML then s=0 PMOS is in OFF condition ML drops to zero. NMOS in this buffer is designed with low threshold voltage and this SCPF is mainly used in high speed application since it executes more searches within the given time. The minimum time required to do the operation is given in (7). Compared to conventional technology SCPF eliminates the pre charge time.

$$T_{TOTALSCPF} = T_{WRITESCPF} + T_{SEARCHSCPF} \quad (7)$$

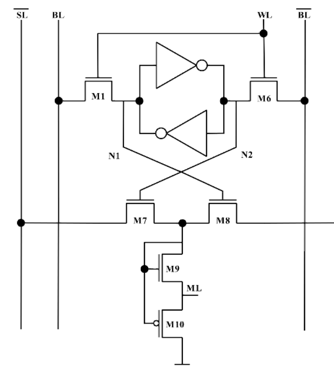

Fig. 16 SCPF CAM architecture [12]

E. Self Controlled Pre Charge Free CAM Architecture

In SCPF each cell is connected to buffer and then connected to ML so the number of transistor is increased. In order to reduce the count of the transistor two CAM cells connected to

AND logic so the transistor count getting reduced [13].

- AND gate using pass transistor logic

The pass transistor logic is widely used in integrated circuits for its reduction of number of transistors [14], but the output levels are not up to the level. Here the input is applied at source or drain rather than a gate as like in CMOS which acts as a switch. Both nmos and pmos can be used in pass transistor logic, but nmos passes strong '0' and weak '1'and pmos passes strong '1' and weak '0'.AND gate designed in CMOS needs six transistors but in pass transistor logic only two transistors alone (Fig. 17).

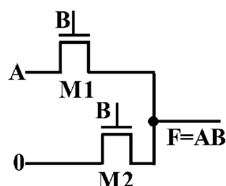

Fig. 17 Diagram of AND using pass transistor

When A=B=1 F=1since M1 is in ON condition, A=B=0 F=0 since M2 is in ON condition so '0' is directly connected to F. Either A=0 or B=0 F=0. This can be clearly illustrated in the Table. 1. In this hybrid SCPF design two CAM cells are connected to AND logic using pass transistor, if both the CAM cells gives the result as match then ML becomes HIGH else any one of the CAM cell gives mismatch condition the ML drops to LOW value as shown in Fig.18.

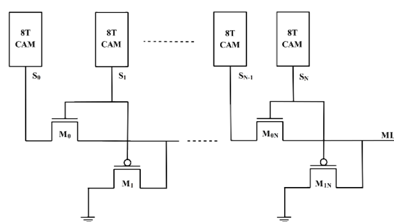

Fig. 18 Hybrid SCPF architecture

Table. 1 Truth Table of the AND using Pass Transistor Logic

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

IV. Proposed Method

In the existing method six transistor SRAM is used for storing the data it will increase the power consumption and area usage [15] [16]. The problem mentioned above can be reduced using our new technique of designing four transistor SRAM in the pre charge free CAM , Self controlled pre charge free CAM and in Hybrid CAM as shown in Fig. 19 (a), (b) and (c) respectively.

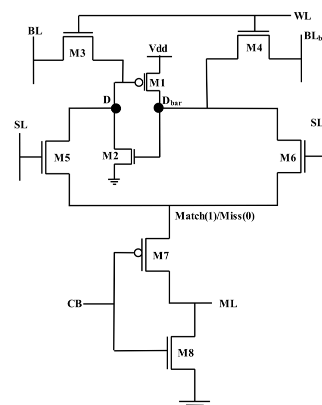

Fig. 19 (a) Pre charge free CAM

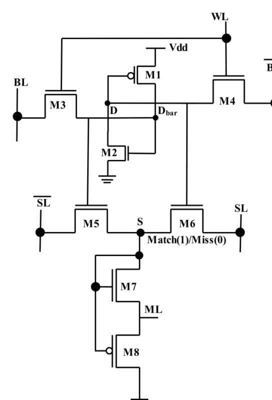

Fig. 19 (b) Self Controlled Pre charge free CAM

Here two cross coupled inverters can be replaced by one NMOS and one PMOS, where remaining part that is write enable, bit line and bit line bar occupies same place. In the proposed technique WL enable the two NMOS while writing so that data in BL and BLbar will reach D and DB.

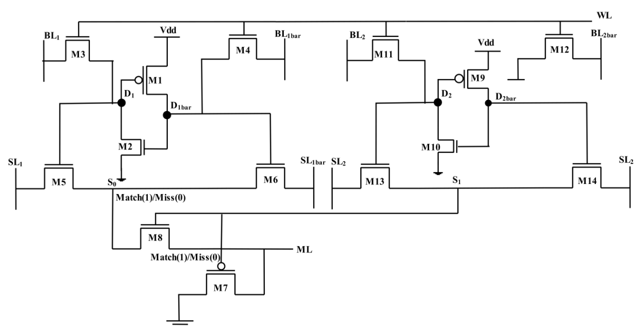

Fig. 19 (c) Hybrid Self Controlled Pre charge free CAM

V. Results And Discussion

The circuits are implemented in SYNOPSIS HSPICE the different parameters are observed. The performance of the different CAM circuits is shown in Table. 2 to Table. 7. Parameters like Average current, average power and average energy are analyzed. From the analysis it's been found that the 32nm technology performance is better when compared to other CMOS technology.

Table. 2 Parameters of 6T PFCAM

CMOS Technology	Avg.Current	Avg.Power	Avg.Energy	No. of Transistor
180nm	8.844u	8.844u	90.278f	40
90nm	4.6919u	4.6919u	48.19f	
65nm	5.4933u	5.4933u	56.244f	
45nm	1.8305u	1.8305u	18.841f	
32nm	1.9324u	1.9324u	19.798f	

Table. 3 Parameters of 4T PFCAM

CMOS Technology	Avg.Current	Avg.Power	Avg.Energy	No.of Transistor
180nm	8.7008u	8.7008u	91.011f	32
90nm	7.9429u	7.9429u	83.737f	
65nm	4.3965u	4.3965u	46.351f	
45nm	5.6232u	5.6232u	59.38f	
32nm	5.0242u	5.0242u	53.256f	

Table. 4 Parameters of 6T SCPFCAM

CMOS Technology	Avg.Current	Avg.Power	Avg.Energy	No.of Transistor
180nm	8.9015u	8.9015u	90.884f	40
90nm	4.0956u	4.0956u	41.976f	
65nm	5.0323u	5.0323u	51.402f	
45nm	1.519u	1.519u	15.603f	
32nm	1.6711u	1.6711u	17.101f	

Table. 5 Parameters of 4T SCPFCAM

CMOS Technology	Avg.Current	Avg.Power	Avg.Energy	No.of Transistor
180nm	8.4337u	8.4337u	88.101f	32
90nm	7.563u	7.563u	76.697f	
65nm	4.1586u	4.1586u	43.784f	
45nm	5.3808u	5.3808u	56.837f	
32nm	4.6572u	4.6572u	49.369f	

Table. 6 Parameters of 6T Hybrid SCPFCAM

CMOS Technology	Avg.Current	Avg.Power	Avg.Energy	No.of Transistor
180nm	0.33608u	0.33608u	5.436f	36
90nm	0.17979u	0.17979u	2.800f	
65nm	0.23748u	0.23748u	3.4903f	
45nm	0.10714u	0.10714u	1.4419f	
32nm	0.32558u	0.32558u	3.521f	

Table. 7 Parameters of 4T Hybrid SCPFCAM

CMOS Technology	Avg.Current	Avg.Power	Avg.Energy	No.of Transistor
180nm	8.5258u	8.5258u	89.029f	28
90nm	7.6172u	7.6172u	80.272f	
65nm	4.2274u	4.2274u	44.485f	
45nm	5.3886u	5.3886u	56.928f	
32nm	4.6569u	4.6569u	49.37f	

VI. CONCLUSION

In this paper a hybrid self controlled pre charge free Content Addressable Memory is proposed using CMOS 32nm technology for image processing devices. The design performs well with high speed and high performance search engine. The main advantage is the minimization of search time for larger word length. When compared to the conventional SCPF-CAM, 8T CAM the proposed HSCPF CAM reduces the number of transistors. The reduction in area is about approximately 20%. The results show that the proposed area reduced 4T SRAM can be used in content addressable memory to reduce power. It can be applied in low power and low energy applications effectively. In future the work is to be carried out using FinFET technology where the leakage current is expected to be reduced compared to the CMOS circuits.

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