Embedded system for audio source localization based on beamforming

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***Abstract*—** Paper presents design of embedded audio source localization system with respect to compact dimensions, low power consumption and easy implementation to applications such as teleconferencing, security and robotics systems. It consists of the three main functional parts: fixed geometry microphone array with fifteen omnidirectional units with geometrical configuration adapted for beamforming at center frequency of 1750 Hz, sixteen channel preamplifier unit with built-in antialias filter and evaluation unit based on five 32bit microcontrollers Freescale MCF51AC128 where each concurrently processes a part of the localization algorithm. Evaluation unit is equipped with alphanumerical LCD display for visualization of the device state and localization results in autonomous mode. For communication with supervision system is provided USB interface allowing complete configuration possibilities and results transferring including diagnostic data.

***Keywords*—**acoustic source localization, beamforming, FFT, intelligent sensor, microphone array, ColdFire V1.

I. Introduction

Beginning of audio localization is dated to the year 1880 when the first device for this purpose was designed. Its inventor Professor Mayer used it for navigation improvement in fog. This instrument was called by its author Mayer's topophone. On the basis of his invention was constructed number of similar devices but with questionable practical usage. The biggest interest in audio location systems occurs in the period between World War 1 and World War 2. They were primarily used for detection a localization of the aircraft engine sound. Measured data about aircraft position was directly transferred to air-defense artillery which can aim at target before visual contact. Constructions and dimensions of these systems were very various but the basic concept is based on Mayer's topophone improved with next two horns oriented in vertical plane. Due to state of electronics then minimally two people were required for sound analysis originated from horn system. Since it was impossible to continuously enlarge horn dimensions for better gain achieving, static dishes and walls based on spherical reflection surface was developed. These systems were able to detect aircrafts at longer distances. After radio locator invention in 1934 audio location devices were not further developed in this area because they were completely replaced by RADAR systems with better detection and ranging properties [6].

Nowadays very dynamical development in electronics and computer science enables applying of the sound localization systems in areas where it was impossible due to technical and economical aspects several years ago. These areas include applications in security, teleconferencing, robotic systems and other else where information is coded in audio signal source position.

This paper deals with design of the compact audio source localization system consisting of microphone array with fifteen electret units, multichannel preamplifier with antialias filter and evaluation unit based on five 32bit microcontrollers. It also includes software implementation of data acquisition, digital filters and sound source localization algorithm. Theoretical part describes main principle of delay and sum type beamformer operation and its application in sound source localization system. Next part proposes design of the sensory system consisting of microphone array with fixed geometry and preamplifiers with antialiasing filters for signal conditioning to correct voltage levels before analog-to-digital conversion process in microcontrollers. Then follows chapter describing hardware architecture of the evaluation system based on five 32bit Freescale ColdFire V1 MCF51AC128 microcontrollers where each performs concurrently portion of the localization algorithm. Last part of the paper deals with software implementation of the evaluation unit.

II. Beamforming principle

Principle of delay and sum beamformer operation is obvious from Fig. 1. Input signals from microphone array x[k] are delayed by time which depends on sensory system geometrical configuration and sound source angle [1], [5]. We can consider that signals from microphone units in the array are same except time-shift. Maximum level of useful signal after summing we obtain by setting of appropriate delay d_a[m] to each audio channel.

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Beamformer output $y_a[k]$ steered to angle a can be computed by equation (1) where $x_m[k]$ is input signal from microphone m, d_a is delay in samples introduced to signal path of microphone m for beam direction a and M is number of microphone units.

$$y_a[k] = \sum_{m=1}^{M} x_m[k - d_a[m]] \tag{1}$$

For linear uniform microphone array depicted in Fig. 2 and on assumption that sound source is in much larger distance than is each sensor spacing d_S, time delay in each microphone unit signal for direction of sound wave arrival α can be computed by equation (2), where k is microphone unit index and v is sound wave propagation speed in air. Reference unit is microphone with index 1 which has zero time shifts for all source angles.

$$t_k = \frac{\sin\alpha \cdot d_s}{v} \cdot (k-1) \tag{2}$$

Sound source localization using delay and sum beamformer is based on computation of its output signal level for each sound source azimuth angle. Root-mean-square value of the n samples length output signal and azimuth angle a can be determined by equation (3).

$$V_{RMS}[a] = \sqrt{\frac{1}{n}\sum_{k=1}^{n} y_a{}^2[k]} \tag{3}$$

Maximum RMS value of beamformer output and corresponding angle indicates sound source azimuth:

$$\alpha = \arg\max_a (V_{RMS}[a]). \tag{4}$$

A. Signal filtering

Because of beamformer best works in narrow frequency range which is fully determined by microphone array geometry it is very important to limit bandwidth of the signal entering beamformer inputs. This can be done by inserting analog band-pass filters realized by operational amplifiers to the signal path before analog-to-digital converter or by digital band-pass filter which operates with digital signal after A/D converter. Advantage of the first approach is that there is no computational cost on evaluation system. On the other hand it is difficult to practical realize precision higher orders filters which are required for this purpose. Second method assumes that signal bandwidth is restricted by microphone units itself and therefore there is no need to apply antialias filter before A/D converter if sampling frequency is high enough. All filtration tasks are then processed digitally enabling to use filter which best fulfills our requirements. In real audio processing system it is still better to use at least lower order antialias filter which can smooth transients originating on long signal path from microphone units to preamplifier. Filter cutoff frequency should be selected as highest possible for proper beamformer operation on the other hand it must band limit signal to fulfill the Shannon-Kotelnikov sampling theorem at used sampling frequency.

With respect to usage of fixed point arithmetic in evaluation system it is better to use finite impulse response (FIR) filter instead of infinite impulse response (IIR) filter by reason of higher order IIR filter implementation is sensitive to round-off errors during computations. FIR filters does not have this limitation so there is no problem with filter instability or bad results. But requirements on the computational power are much higher due to processing time intensive convolution of filter kernel with filtered signal.

For our application is suitable digital version of Butterworth 8th order low-pass and high-pass filters combined to band pass filter. Butterworth low-pass filter poles s_k can be computed using equation (5), where ω_c is cutoff angular frequency, n filter order and k pole index in the range of 1, 2, 3, …, n [8].

$$s_k = e^{\frac{j\pi}{2n}(2kn-1)} \tag{5}$$

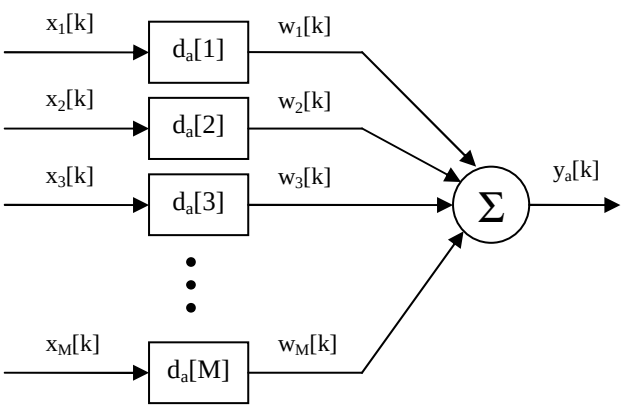

Fig. 1 Delay and sum beamformer operation.

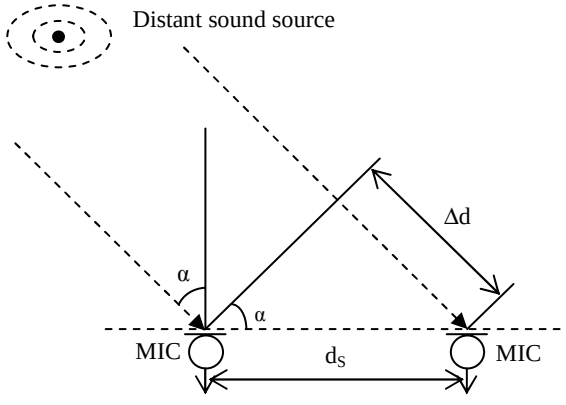

Fig. 2 Sound wave impacting pair of sensors.

Transfer function of the n-th order low-pass filter then is:

$$H_{LP}(s)=\frac{\prod_{k=1}^{n} s_k}{\prod_{k=1}^{n}\left(\frac{1}{\omega_c}s-s_k\right)}, \quad (6)$$

where ω_c is cutoff angular frequency. Transfer function of high-pass filter is:

$$H_{HP}(s)=\frac{s^n\prod_{k=1}^{n} s_k}{\prod_{k=1}^{n}\left(\frac{1}{\omega_c}s-s_k\right)}. \quad (7)$$

Discrete impulse responses (filter kernels) of the both filters we obtain after conversion of continuous-time models (6) and (7) to discrete-time models in the form (8) followed by computation of filters response to unit impulse δ[k].

$$H(z)=\frac{b_n z^n+b_{n-1}z^{n-1}+\ldots+b_0}{a_n z^n+a_{n-1}z^{n-1}+\ldots+a_0} \quad (8)$$

Band-pass filter kernel $h_{BP}[k]$ is equal to the convolution of the low-pass $h_{LP}[k]$ and high-pass $h_{HP}[k]$ filter kernels:

$$h_{BP}[k]=h_{LP}[k]*h_{HP}[k]. \quad (9)$$

Filter output y[k] is equal to the convolution of filter kernel $h_{BP}[k]$ with input signal x[k] [7]:

$$y[k]=h_{BP}[k]*x[k]. \quad (10)$$

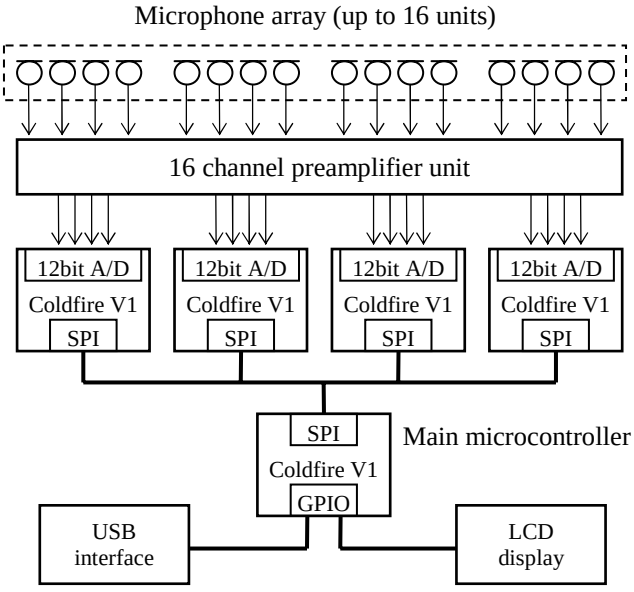

Fig. 3 Localization system architecture.

Due to the fact that convolution computation for large *N* takes a lot of computer processing time, it is suitable to compute it in the frequency domain in which processing time consuming convolution is replaced by multiplication of Fourier transformed input signal x[k] and filter kernel $h_{BP}[k]$ [7]:

$$y[k]=F^{-1}\{F\{h_{BP}[k]\}\cdot F\{x[k]\}\}. \quad (11)$$

III. Localization System Hardware Architecture

Hardware of the acoustic source localization system is obvious from Fig. 3. It consists of microphone array with fixed geometry configuration, sixteen channels preamplifier with built-in antialias filter and evaluation unit.

A. Microphone array

For microphone array geometry design was created program equipment working in Matlab 6.5 environment which can compute for given geometry both directional and steered directional characteristic using beamforming for demanded main lobe angle. Using this program was designed array geometry optimized for audio source frequencies in the range of 1000 Hz to 3000 Hz where is on the basis of simulation results ensured required shape of directional characteristic and satisfactory steered directional characteristic over all demanded main lobe angles without distinct side lobes. Operation with wider frequency range is possible but with negative effect on the directional characteristic. Simulated characteristics for different microphone array configurations are depicted in the Fig. 4. In the first column is microphone array configuration, in the second column array directional characteristic and in the last steered directional characteristic to angle 45 degrees using beamforming. Practically realized is the last array at the bottom of the figure.

Table I. Coordinates of microphones in the array.

Microphone index [-]	X coordinate [mm]	Y coordinate [mm]
1	45.0	0.0
2	28.1	35.2
3	-10.0	43.9
4	-40.5	19.5
5	-40.5	-19.5
6	-10.0	-43.9
7	28.1	-35.2
8	81.1	39.1
9	20.0	87.7
10	-56.1	70.4
11	-90.0	0.0
12	-56.1	-70.4
13	20.0	-87.7
14	81.1	-39.1
15	0.0	0.0

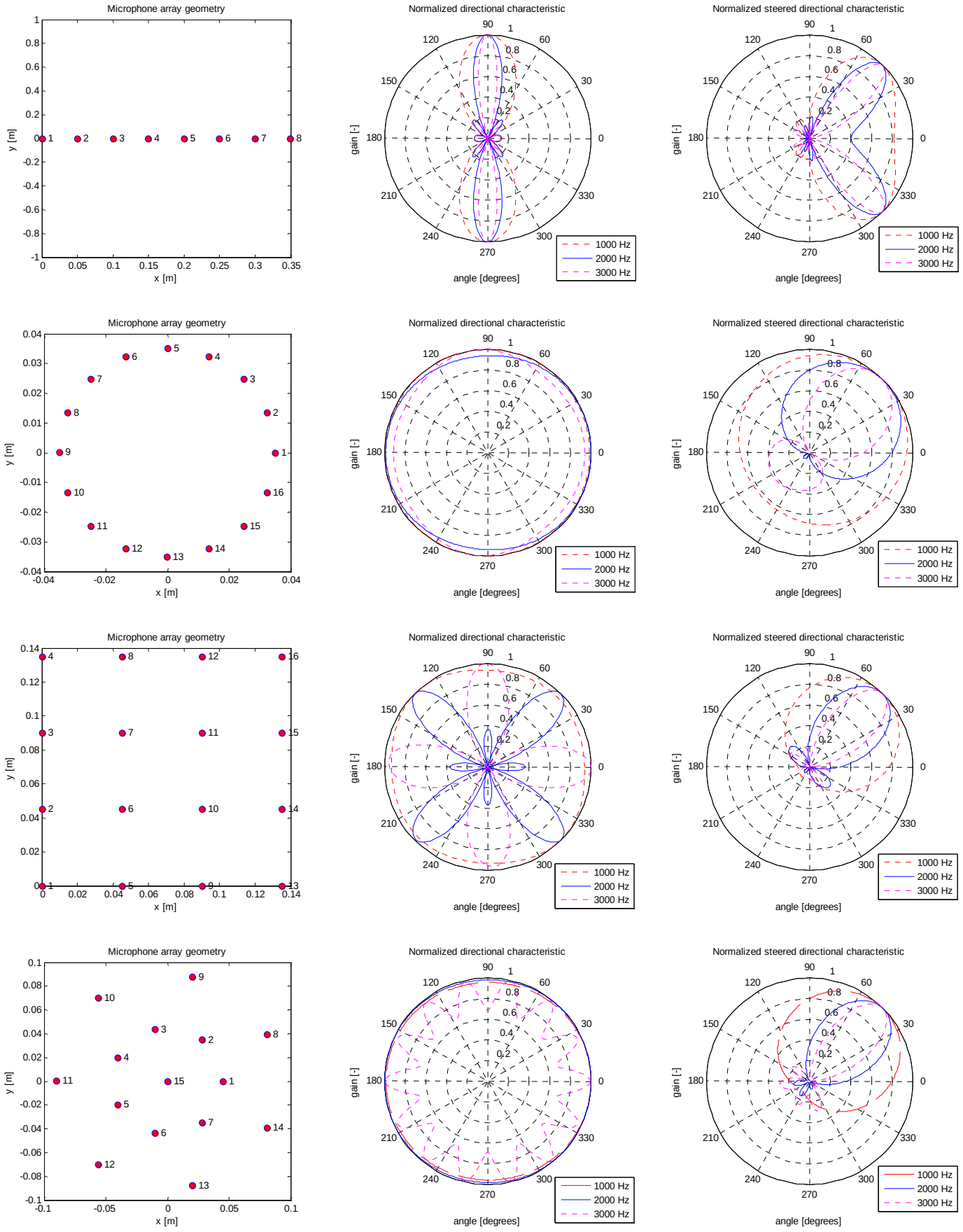

Fig. 4 Simulated directional characteristics of different microphone array geometrical configuration.

Realized microphone array contains 15 omnidirectional electret microphone units MCE100 soldered on the printed circuit board (PCB) with dimensions of 200 x 200 mm. On the board is integrated stabilized power supply with output voltage of 5 V which is needed for operation of microphone units. Output signal from each microphone is connected to double-row connector where 4 pins are reserved for array supply voltage in the range of 7.5 to 15 V, 20 pins for ground and 16 pins for audio signal output. Because of preamplifier is not integrated in the microphone array board it is suitable to connect amplifier with shortest possible ribbon cable to avoid interference leakage and useful signal losses. Schematic of the microphone array is in the Fig. 5, photograph of completed array in the Fig. 6.

B. Microphone preamplifier

Each microphone cartridge of microphone array is connected with preamplifier units followed by 2nd order active low-pass antialias filters based on rail-to-rail quad operational amplifiers TS914 (for one audio channel is used half of the operators). Filter parts was designed using Bessel approximation with cut-off frequency of 16000 Hz and gain of 0 dB in the passband. This type of the filter was chosen due to linear curve of the phase characteristic in the wide frequency range and advantageous step response with small overshot. On the other hand its drawback is smaller slope of the stop-band part of the frequency characteristic in comparison with Chebyshev or Butterworth approximations.

Parts values were designed using procedure published in [8]. Computation of filter parts is based on transfer function of Sallen-Key 2nd order low-pass filter (12) where coefficients a_1 and b_1 are equal to (13) and (14).

$$A(s)=\frac{A_0}{1+a_1 s+b_1 s^2} \tag{12}$$

$$a_1=\omega_c\left[C_1(R_1+R_2)+(1-A_0)R_1C_2\right] \tag{13}$$

$$b_1=\omega_c{}^2 R_1R_2C_1C_2 \tag{14}$$

Transfer function of the 2nd order low-pass filter is:

$$A(s)=\frac{A_0}{1+\omega_c\left[C_1(R_1+R_2)+(1-A_0)R_1C_2\right]s+\omega_c{}^2R_1R_2C_1C_2s^2}, \tag{15}$$

where ω_c is a cutoff angular frequency, A_0 is gain of the filter in the passband and a_1 and b_1 are filter coefficients determining its properties. After the formulation of R_1 from equation (14) and constituting to (13) we obtain quadratic equation:

$$R_2{}^2C_1{}^2C_2\omega_c{}^2-a_1R_2C_1C_2\omega_c+b_1\left(C_1+C_2-A_0C_2\right)=0 \tag{16}$$

Its solution is equation for computation of R_2 part value (18), R_1 part value can be computed by (17).

$$R_1=\frac{b_1}{R_2C_1C_2\omega_c{}^2} \tag{17}$$

$$R_2=\frac{a_1C_1C_2\omega_c+\sqrt{\left(-a_1C_1C_2\omega_c\right)^2-4C_1{}^2C_2\omega_c{}^2b_1\left(C_1+C_2-A_0C_2\right)}}{2C_1{}^2C_2\omega_c{}^2} \tag{18}$$

In order to obtain non negative value under square root in (18), capacitors values must fulfill (19).

$$C_2\geq C_1\frac{4b_1A_0+a_1{}^2A_0-a_1{}^2}{a_1{}^2A_0} \tag{19}$$

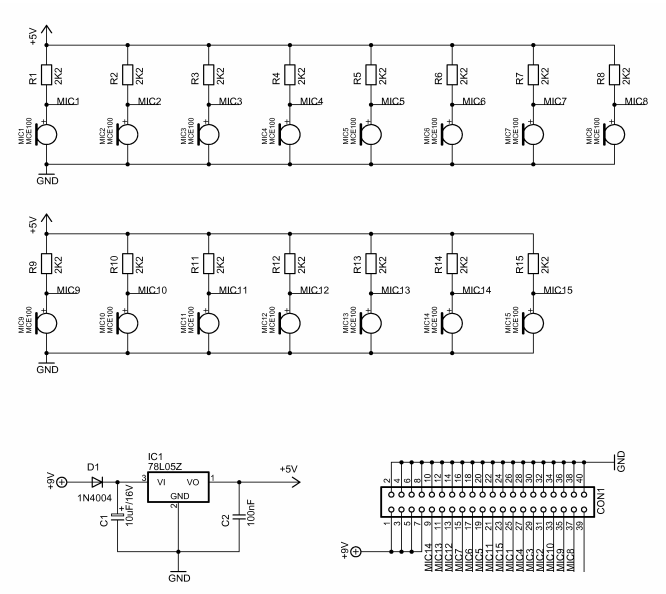

Fig. 5 Microphone array board schematic.

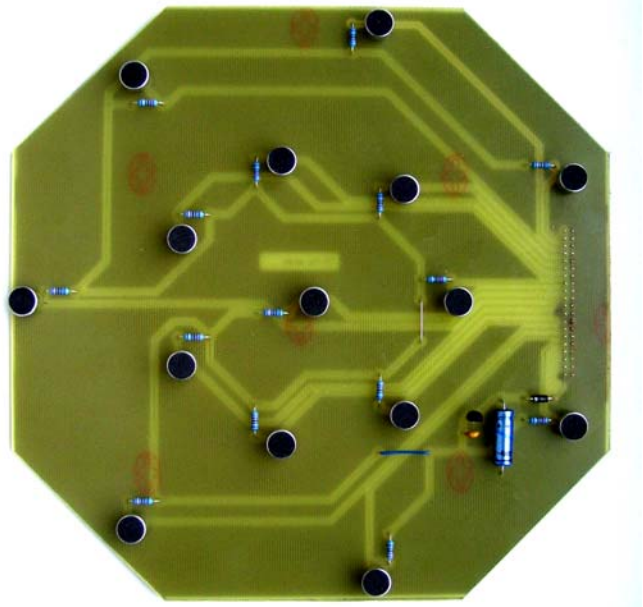

Fig. 6 Photograph of the completed microphone array board.

Bessel-type filter coefficients for both filter stages are provided in the Table II.

Table II. Bessel filter coefficients [8].

Filter order	Stage i	a_i	b_i	Q_i
1	1	1.0000	0.0000	-
2	**1**	**1.3617**	**0.6180**	**0.58**
3	1 2	0.7560 0.9996	0.0000 0.4772	- 0.69
4	1 2	1.3397 0.7743	0.4889 0.3890	0.52 0.81

Practically the easiest way is to choose first capacitors C_1 and C_2 manufactured usually in E6 series and then compute resistor values. Exact resistor value can be reached by connecting more resistors in parallel or in series. Schematic of the amplifier for one audio channel is depicted in the Fig. 7. As can be seen preamplifier consist of the two stages. First one is non-inverting amplifier IC_{1A} with gain of 20 dB which additionally represents low impedance signal source for filter circuit. Second operator IC_{1B} is a part of 2nd order Bessel filter. Its output is directly connected to analog-to-digital converter of the evaluation unit without coupling capacitor.

C. Evaluation unit

Hardware of the evaluation system is based on 32bit Freescale ColdFire V1 MCF51AC128 microcontrollers each providing computational power near 50 DMIPS and low power consumption. These microcontrollers have integrated on the chip 128 KB of the flash memory, 32 KB of static RAM and many peripherals such as 12bit analog to digital converter with up to 24 channels, timer system, serial peripheral interface (SPI), serial communication interface (SCI), controller-area network (CAN) and others [2].

Evaluation unit structure is obvious from Fig.3. Analog signal from microphone units is amplified to voltage range 0 – 5 V suitable for microcontrollers A/D converter. Sixteen analog channels are then uniformly distributed between four microcontrollers which work as slave devices of the master microcontroller. Slave devices function is controlled by 8-bit bidirectional bus DB0-7 connected to rapid general purpose input / output interface (RGPIO) which is available on port F pins. About slave devices actual status is master device informed by BUSY signal which is active in logic high state. In this state master must wait for completion of previous operation before next command will be issued. Data transfers on parallel bus from slaves to master are synchronized by STROBE signal indicating valid data byte on the bus ready for transfer. For high-speed data transfers is utilized serial peripheral interface (SPI) which is fully controlled by main microcontroller in master mode. Operation options of the SPI interface are fully programmable so it is possible to program transmit bit rate, serial clock phase and polarity, MSB first or LSB first shifting and other possibilities. Transmitter and receiver double buffering eliminates possible character losses when high bit rates are used. Maximum clock frequency in master mode is bus frequency (f_{BUS}) divided by 2, in slave mode it is f_{BUS} divided by 4. Serial peripheral communication interface operation is obvious from Fig. 9. Master device, in our case microcontroller unit (MCU), initiates communication by selecting slave device using slave select signal which is active in logic low level. Then interface shifts data from the internal register to the MISO line (Master Out – Slave In) while on the SPSCK line is generated clock signal. At the same time master device receives data from the MISO (Master In – Slave Out) line. Slave select signal is pulled high logic level when communication with slave device is done.

Communication with supervision system is provided by FT232BM USB 1.1 and 2.0 compatible universal asynchronous receiver / transmitter (UART) integrated circuit which is intended for many application areas such as: USB to RS232 converters, smart card readers, bar code readers, USB hardware modems, USB instrumentation and many other applications. It is capable to communicate at TTL levels with data transfer rates up to 3 MBd. On the chip integrated

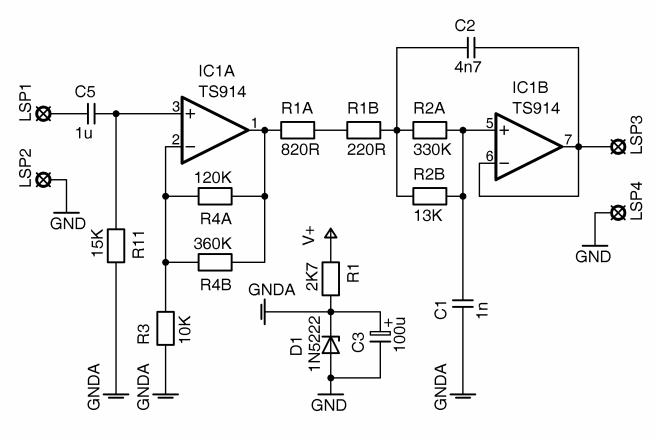

Fig. 7 Microphone array preamplifier schematic for one channel.

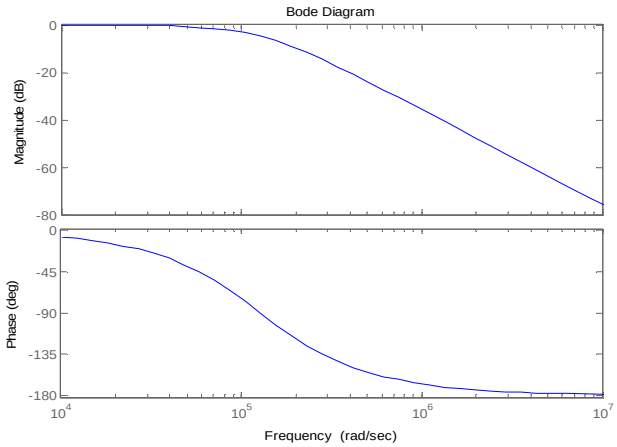

Fig. 8 Filter Bode frequency response simulation.

transmit and receive buffers with capacity of 128 B and 384 B respectively enables high data throughput. IC operates from single power supply with voltage of 5 V. USB input / output interface is supplied from integrated 3.3 V voltage regulator. Due to integrated level converter for UART I/O signals it is possible to connect it with logic circuits operating at 3.3 V or 5 V power supplies [3]. FT232BM is wired in manufacturer recommended wiring for self powered application with 5 V input / output interface. Clock signal is generated externally by crystal oscillator Q_2 with frequency of 6 MHz. Activity of serial interface is indicated by two LEDs LD_1 and LD_2 for receive and transmit mode separately. FT232BM UART signals RxD (receive data) and TxD (transmit data) are cross-connected to pins TxD and RxD of the main microcontroller UART pins which is able to achieve communication speed of up to 1.5 Mbits per second at 25 MHz bus clock. Serial interface control signals RTS (request to send), CTS (clear to send), DTR (data terminal ready), DSR (data set ready) except DCD (data carrier detect) and RI (ring indicator) are connected to general purpose input / output pins of the microcontroller enabling utilization of hardware flow control in case of need.

Microcontroller's UART interface supports full-duplex operation utilizing standard non-return-to-zero (NRZ) format. Transmitter and receiver can be enabled separately allowing lower power consumption. Their double buffering enables high speed communication without problems with received characters losses. Main features of the UART interface are [2]:

- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Programmable baud rates
- Interrupt-driven or polled operation

To the FT232BM is connected 1 Kbit EEPROM memory 93C46 with 64 x 16b internal organization. It is used for storage of USB vendor identification (VID), device class definition for physical interface devices (PID), serial number and product description strings. Memory can operate at wide power supply voltages – low voltage (1.8 V to 5.5 V) or standard voltage (2.7 V to 5.5 V). Its connection with UART IC is provided by 3-wire synchronous serial interface operating up-to 2 MHz clock rate at 5 V power supply.

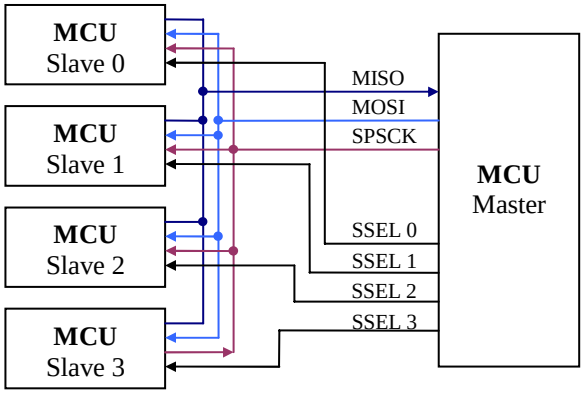

Fig. 9 Serial peripheral interface operation.

LCD display MC1604B is connected to master MCU using 8 bit wide bidirectional data bus connected to port D pins. LCD signals RS, R/W and E are controlled by port C pins PTC0 to PTC3. Backlight intensity can be adjusted by MCU generated PWM signal on pin PTG4. Variable resistor R_{14} set display contrast.

Microcontrollers have one common external Pierce clock generator with frequency of 32.768 kHz which is in each MCU by internal FFL unit multiplied to 50.33 MHz clock frequency. This solution grants that A/D converters work at the same clock frequency and internal real-time clock has exact one second period.

Photograph of realized evaluation unit is in the Fig. 10 its complete schematic is depicted in the Fig. 11.

IV. Software Implementation

Microcontroller's firmware was developed with respect to their limited system resources. So all implemented algorithms such as FFT, convolution and others must be fully optimized for memory usage and computational efficiency. Next problem is absence of the hardware floating point unit causing low arithmetic performance with this representation of real numbers. Due to this fact fixed point number representation was used. In this format is reserved fixed number of bits before and after decimal point. Big advantage is that all operations work with standard integer arithmetic which is very fast. In our case was used Q22.10 format which means 22 bits integer bits and 10 fractional bits.

Software was written in C language in Freescale CodeWarrior for Microcontrollers development studio version 6.3 with utilization of Processor Expert tool [4], [9].

A. Slave microcontrollers

All slave microcontrollers have exactly same firmware so software description will be focused to only one slave microcontroller function of others is identical.

After power on sequence microcontroller initializes all necessary internal hardware modules such as clock generator module, analog-to-digital converter and serial peripheral interface. During these operations is BUSY signal set to high state informing the master microcontroller that it is not ready processing commands.

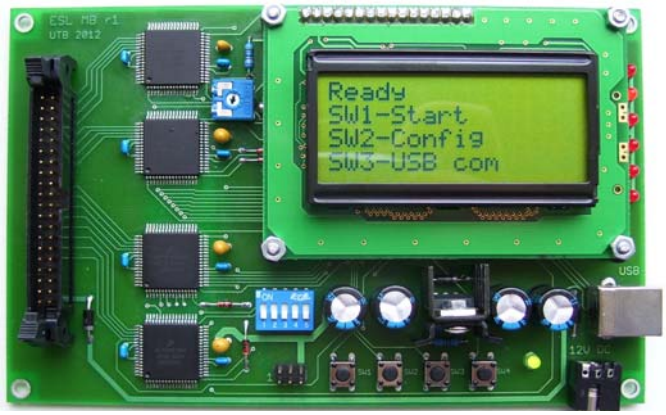

Fig. 10 Photograph of the realized evaluation unit.

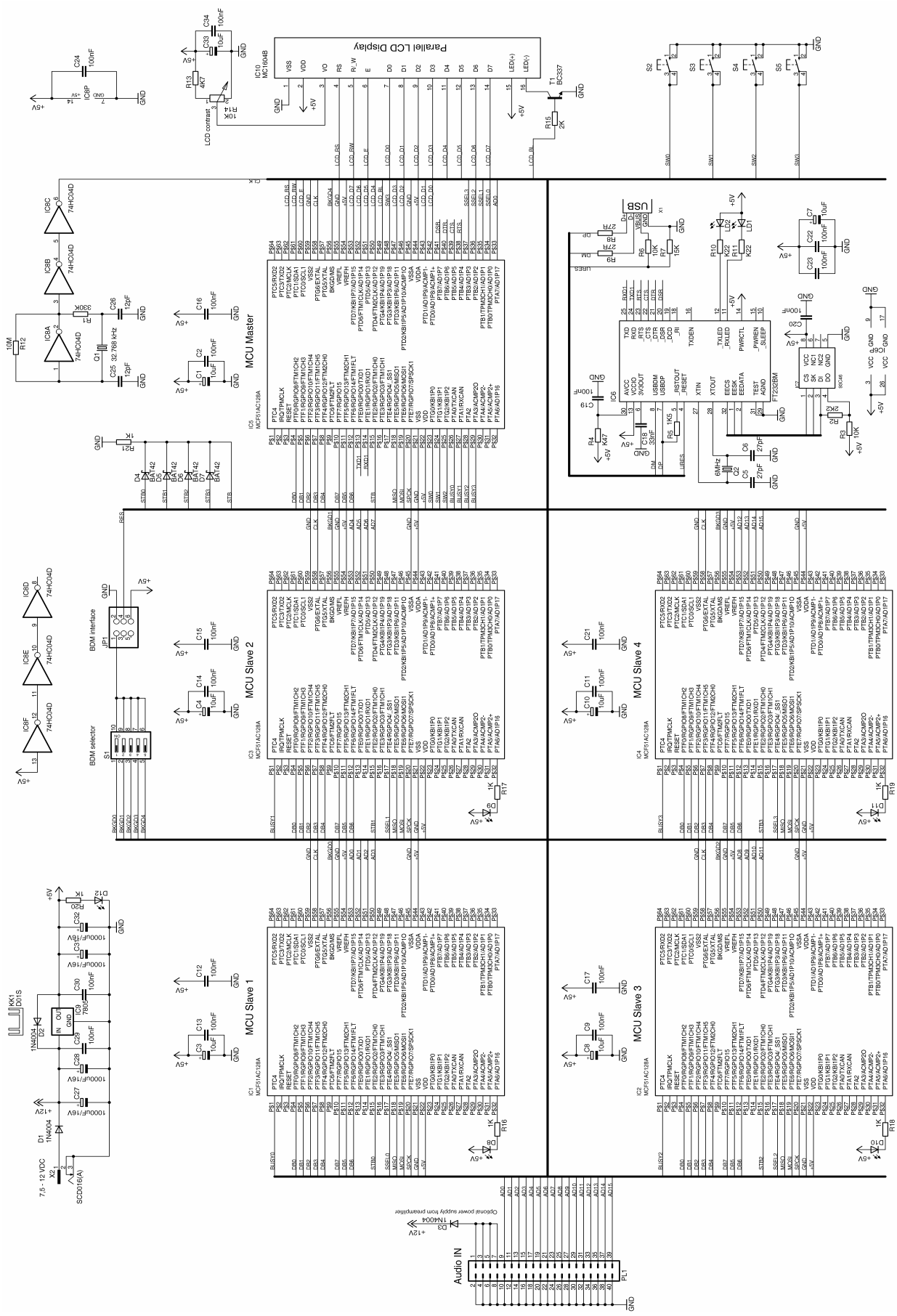

Fig. 11 Evaluation unit schematics.

After success initialization process BUSY signal is cleared and microcontroller waits for command for synchronized start of A/D conversions. This command is transferred via parallel data bus and has code of 0x01. After command reception BUSY signal is set and A/D conversions of the four analog channels are immediately initiated. Conversions are processed at full converter speed with 12bit resolution. Sampling frequency of each channel at maximum bus clock frequency of 25.17 MHz is approximately 65 kHz. Conversions are stopped when 768 samples of each channel are stored to internal buffers. Remaining free space of 1024 samples length buffers is filled with zeros. Then takes place FFT computation of sampled input signals using DIT2 algorithm and multiplication of its results with 256 samples length Fourier-transformed band-pass filter kernel. On the multiplication result is applied inverse Fourier transform resulting in band-pass filtered input signals ready for next processing. Digital filtering stage is finished be clearing BUSY signal. At this moment microcontroller waits for commands initiating partial four channel beamforming on filtered signal. Each command from master must contain four bytes of data containing information about required time-delay applied to the corresponding channel. Results of summing off all four channels are immediately transferred via SPI interface to the master microcontroller. Beamforming stage is processed for all examined angles required by master microcontroller. It is terminated by command containing data 0xffffffff. Then BUSY signal is set to zero and whole cycle is repeated at the A/D conversion start point.

B. Master microcontroller

Similarly as slave microcontrollers master MCU after power on sequence initializes all necessary peripherals including display. On the LCD is displayed main menu from which can user select required action. There are three available possibilities:

- SW1: Start locator
- SW2: Configure basic parameters
- SW3: USB communication enable

At this moment microcontroller waits for user entry. If SW1 button was pushed evaluation unit is switched to autonomous localization mode. Microcontroller continuously analyzes one audio channel with maximum possible sampling frequency and waits for an audio event which triggers localization process. Before localization process can be started microcontroller must check if all slave microcontrollers are ready – BUSY signals must be in low state. If so synchronized A/D conversions start command is issued on the data bus. At this moment microcontroller waits for the completion of data acquisition and digital filtering stage in slave devices by monitoring BUSY signals. When they are in ready state beamforming takes place. Master MCU on the basis of microphone array geometrical configuration generates commands for 4 channel partial beamforming and sums results received from slave microcontrollers. From summed results of partial beamforming is computed RMS value of the signal and stored to the array. When all examined source angles are processed beamforming is terminated by sending 0xffffffff command to slave devices. Finally in RMS values array MCU find maximum value which index directly indicates sound source azimuth in case of angle step variable of the algorithm is set to one degree. Localization result is with audio event time recorded to memory for future use and the last one displayed on the LCD. Then whole cycle is repeated from the point of waiting on audio event.

V. Conclusion

Paper deals with design of compact intelligent sensor for audio source localization with focus on teleconferencing, security and robotics applications. Hardware design is fully adapted to the high processing speed with preservation of low power consumption. This was achieved by utilization of five Freescale ColdFire V1 microcontrollers each concurrently executing part of the localization algorithm. Slave microcontrollers perform data acquisition, digital filtration and partial four channel beamforming. Master microcontroller coordinates all evaluation unit operations and does final calculations of acoustic source azimuth angle. It also provides communication with user by means of LCD display and four push buttons. Implemented USB interface is intended for connection with supervision system which can using simple ASCII-based communication protocol control device functions and transfer locator results. Evaluation unit firmware was completely written in C language in Freescale CodeWarrior IDE and successfully tested on evaluation unit hardware.

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