Exploiting the Vth behavior to design CMOS Voltage References and Temperature Sensors

Wellington Avelino do Amaral, José Antônio de Siqueira Dias, Wilmar Bueno de Moraes

***Abstract*—** The objective of this work is to design a CMOS voltage reference and a temperature sensor based on threshold voltage summation. An original circuit architecture was used. The circuit uses a threshold voltage extractor, a start-up and an operational amplifier. The circuit was fabricated using a 0.35 µm CMOS technology and presented a variation of 11 ppm/^{0}C in the 27 ^{0}C to 120 ^{0}C temperature range. The temperature sensor presented a sensitivity of 1mV/ ^{0}C when operated in the same temperature range.

***Keywords*—** CMOS; Threshold Voltage; Threshold Voltage Extractor; Trimmers; Voltage reference.

I. Introduction

THE necessity of stable and reliable voltage references is well known in integrated circuit design. In ADC [1] and DAC [2] converters, voltage regulators, Frequency Doublers [3] and other circuits where the temperature influence is a limiting factor, the voltage references play a fundamental role.

Bandgap circuits have been extensively used in this kind of application. In CMOS integrated circuits the vertical bipolar transistors can be used to design a bandgap reference or an all CMOS technique can be used to make the voltage reference, as it will be presented in this paper.

To study the drain current dependency of the MOS transistor with temperature it is necessary to consider two parameters; the threshold voltage (Vth) and the mobility (µ). The threshold voltage of the MOS transistor is modeled using equation (1) [4].

$$V_{th} = \Phi_{MS} - \frac{Q_{SS}}{C_{ox}} + 2 \cdot \Phi_F - \frac{Q_B}{C_{ox}} \tag{1}$$

Where;

- ΦF is the Fermi potential of the substrate. It's modeled by equation (2).

$$\Phi_F = \pm \frac{kT}{q} \cdot \ln\left(\frac{C_B}{n_i}\right) \tag{2}$$

- Q_B is equal the quantity of charges per area unit within the superficial depletion region. This quantity is found using equation (3).

$$Q_B = \pm q \cdot C_B \cdot xd_{\max} = \pm\sqrt{2 \cdot K_S \cdot \varepsilon_0 \cdot q \cdot C_B \cdot 2 \cdot |\Phi_F|} \tag{3}$$

- Q_{SS} is the charge density in superficial state per area unit.
- Φ_{MS} is the difference of the work function between metal and semiconductor.
- C_{ox} is the oxide capacitance per area unit. It is found using equation (4).

$$C_{ox} = \frac{K_0 \cdot \varepsilon_0}{x_e} \tag{4}$$

- C_B is the magnitude of the impurity concentration of the substrate.

Deriving Vth with temperature it's possible to found equation (5).

$$\frac{dV_{th}}{dT} = \frac{d\Phi_F}{dT} \cdot \left[2 - \frac{1}{C_{ox}} \cdot \frac{Q_B}{2 \cdot \Phi_F}\right] \tag{5}$$

Where;

$$\frac{d\Phi_F}{dT} \cong \pm\frac{1}{T} \cdot \left[\frac{E_{G0}}{2 \cdot q} - |\Phi_F|\right] \tag{6}$$

So, observing equation (5) it is possible to see that Vth is proportional to 1/T. Exploiting this characteristic it is possible to obtain voltage references stable in temperature, as well as temperature sensors. In the following sections will be shown the design of a voltage reference using this characteristic of dVth/dT.

II. Proposed Voltage Reference

The developed circuit is shown in Fig. 1, where it is possible to see three basic blocks: the threshold voltage extractor, the start-up circuit and the operational amplifier.

The Vth extractor generates the bias current through the transistor M1Vth. In this transistor, the Vgs voltage is the Vgs voltages summation of the transistors M1B and M2B minus the Vgs voltage of the transistor M1A. Therefore, through the correct currents choice in these three transistors, a voltage equal Vth is obtained in the Gate/Source terminals of the transistor M1Vth. So, the bias current of the Vth extractor is a function of the Vth voltage. As the bias voltage is generated inside this circuit and it is not a direct function of VDD, the circuit may not start. Therefore, it is necessary to use a start-up circuit to guarantee that the circuit will not stay in a 0V condition. The operational amplifier is used as a current buffer, to improve the output current drive capacity.

The bias current of the Vth extractor is mirrored to transistor MG206. So, in the gate of the transistor MG211 it is generated a voltage equal 2Vth, resulting in a current proportional to Vth, as showed in equation (7). The same occurs in transistor MG111.

$$I_{2Vth} = \frac{K_P}{2}\cdot\left(\frac{W}{L}\right)_{MG211}\cdot\left(2\cdot Vth_P - Vth_P\right)^2 = \frac{K_P}{2}\cdot\left(\frac{W}{L}\right)_{MG211}\cdot\left(Vth_P\right)^2 \qquad (7)$$

The currents flowing in transistors MG211 and MG111, proportional to Vth, are mirrored to transistors MG25 and MR25 and added in node V25. The transistor MG25 is in the linear operation condition and its drain current is found using equation (8). The voltage Vgs_{MR25} and the current I_{MR25} can be found multiplying the current I_{2Vth} by the coefficients of the current mirrors. So, through the substitution of these values in equation 2, it's possible to find equation (9). Equations (10) and (11) describe the coefficients used in equation (9). Equation (12) models the mobility variation with temperature [5]. It is possible to observe that, as the temperature increases, the mobility decrease, thus, V25 increase.

$$I_{MR25} = \mu_N\cdot C_{ox}\cdot\left(\frac{W}{L}\right)_{MR25}\cdot\left(Vgs_{MR25} - Vth_N\right)\cdot V25 \qquad (8)$$

$$V25 = \frac{(\gamma-1)}{C_{ox}\cdot\left(\frac{W}{L}\right)_{MR25}\cdot\left[\sqrt{\frac{2\cdot\lambda}{C_{ox}\cdot\left(W/L\right)_{MD24}}}\right]\cdot\left(\frac{\sqrt{\mu_P}}{\sqrt{\mu_N}}\right)\cdot\mu_N\cdot R27} \qquad (9)$$

$$\gamma = \left(1+\sqrt{\frac{\left(W/L\right)_{MG30}}{\left(W/L\right)_{MD111}}\cdot\frac{\left(W/L\right)_{MG111}}{\left(W/L\right)_{MD30}}}\right) \qquad (10)$$

$$\lambda = \frac{\left(W/L\right)_{MG32}}{\left(W/L\right)_{MD211}}\cdot\frac{\left(W/L\right)_{MG24}}{\left(W/L\right)_{MD32}}\cdot\frac{C_{ox}}{2}\cdot\left(\frac{W}{L}\right)_{MG211} \qquad (11)$$

$$\mu(T) = \mu(T_0)\cdot\left(\frac{T}{T_0}\right)^{-m} \qquad (12)$$

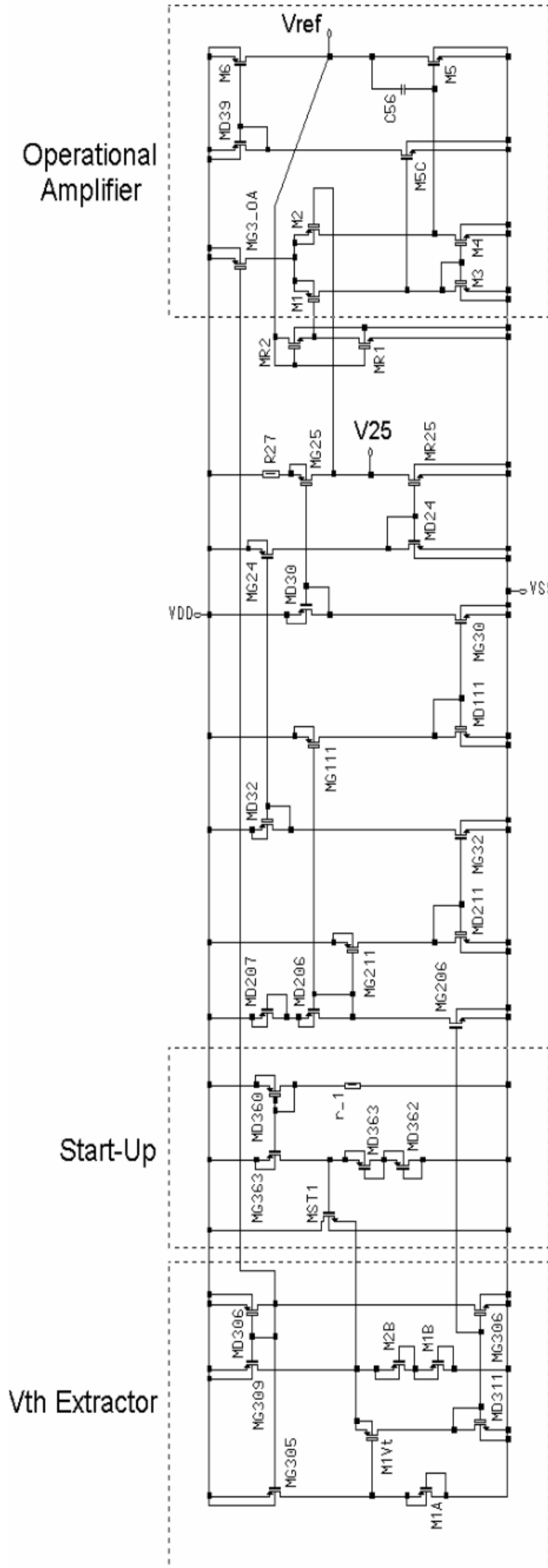

Fig.1 Voltage reference schematic.

So, in V25, a voltage with positive temperature coefficient is obtained (equation 8) and it's possible to adjust its slope using the current mirrors of the circuit.

Equation 13 models the output voltage Vref. As showed, the voltage Vthn decrease as temperature increases. So, as the voltage Vthn has a negative temperature coefficient and the voltage V25 has a positive temperature coefficient, it's possible to adjust the parameters of the transistors to make Vref stable with temperature.

$$V_{ref} = Vthn + V25 \cdot \left(\frac{1}{1 - \sqrt{\frac{\left(W/L \right)_{MR1}}{\left(W/L \right)_{MR2}}}} \right) \qquad (13)$$

III. Trimmers

Some structures were used in the circuit to work as trimmers. In Fig.2 is shown the schematic of the trimmer. The complete schematic of the voltage reference, using the trimmer structures, is shown in Fig 3. In the circuit of Fig 2 it is possible to increase or decrease the current passing through MD30 connecting MT1_D in MG30_D or in MD111_D, respectively.

The same occurs with MT2_D, MT3_D, MT4_D and MT5_D. This way, it is possible to adjust the curve inclination in V25.

MT1, MT2, MT3, MT4 and MT5 were designed to produce different slopes in V25 and they can be used in parallel to produce even more combinations.

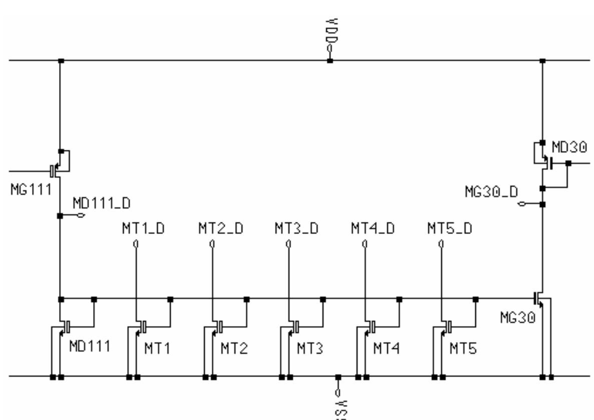

Fig.2 Trimmer Schematic.

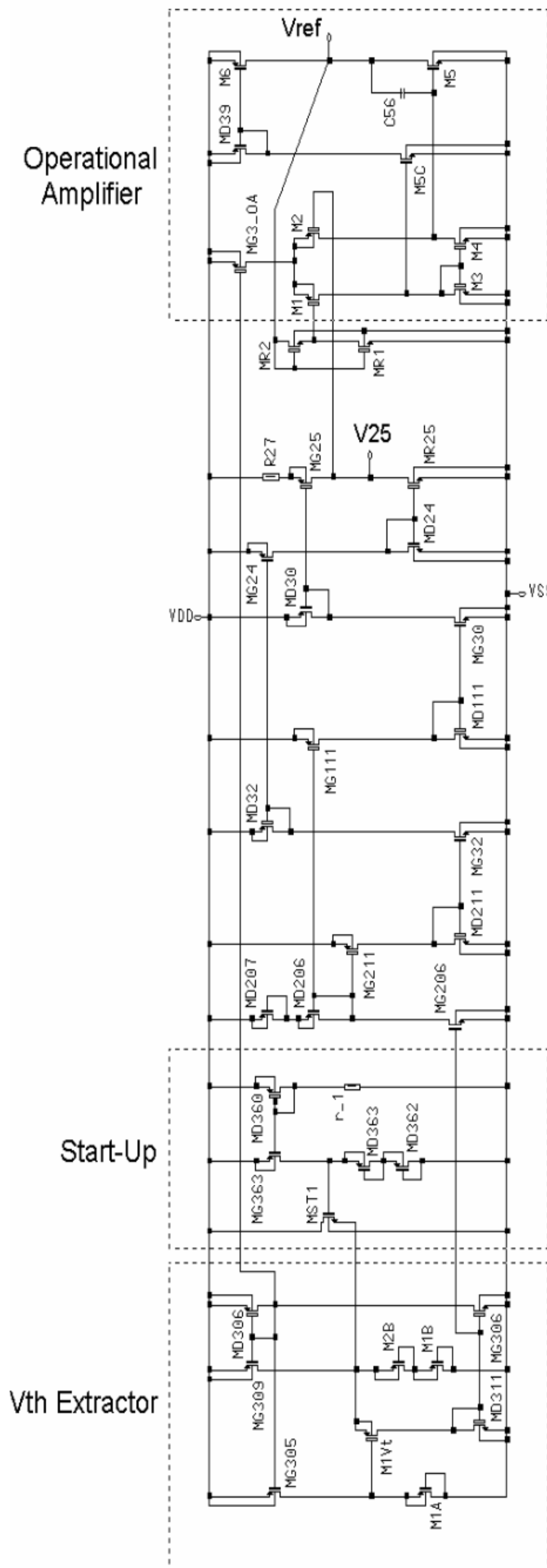

Fig.3 Voltage Reference schematic (with trimmers).

IV. Layout

The circuit was designed and the layout was made using the 0.35µm AMS (Austria Micro-Systems) technology. High voltage transistors were employed, allowing the circuit to operate using VDD = 5V.

Three micrographs of the circuit are shown in Fig.4 to Fig. 6. The total circuit area is 0.74mm^2. Inter-digitated transistors were used in some points of the circuit to save area.

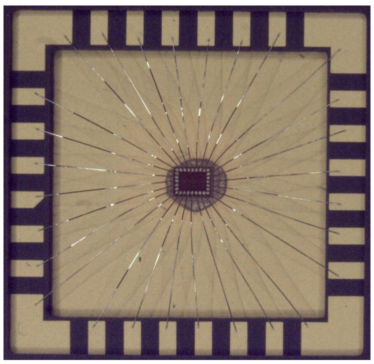

Fig.4 Voltage reference layout (View 1).

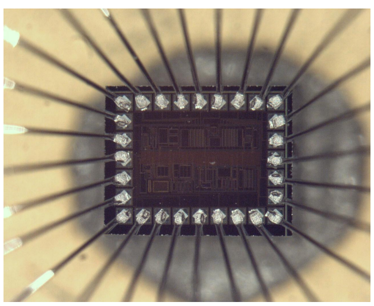

Fig.5 Voltage reference layout (View 2).

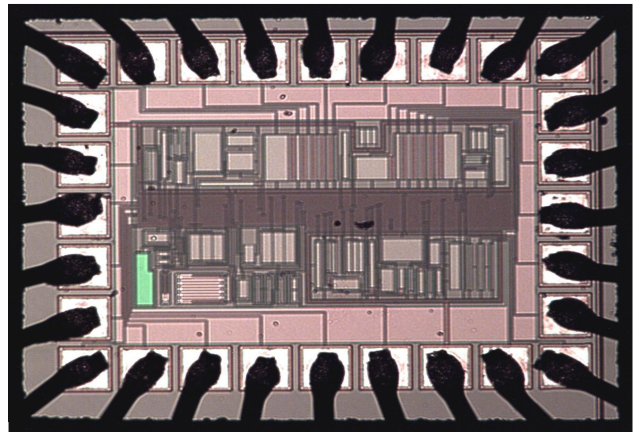

Fig.6 Voltage reference layout (View 3).

V. Experimental Results

The circuit achieved a 1mV of variation when tested in a temperature range of 27^{0}C to 120^{0}C. This variation is equivalent of 11 ppm/^{0}C. The entire circuit consumption was 91µA using VDD = 5V. In Fig. 7 it is shown four results of the variation of Vref with temperature using four different combinations of the trimmers.

Fig.8 shows the measurements made in node V25. It is possible to observe the linear behavior of this voltage in temperature. This characteristic can exploited to design temperature sensors.

In Fig.9 it is shown the output voltage was measured using different values of VDD. The voltage reference stopped working when a VDD of 3.25V was used.

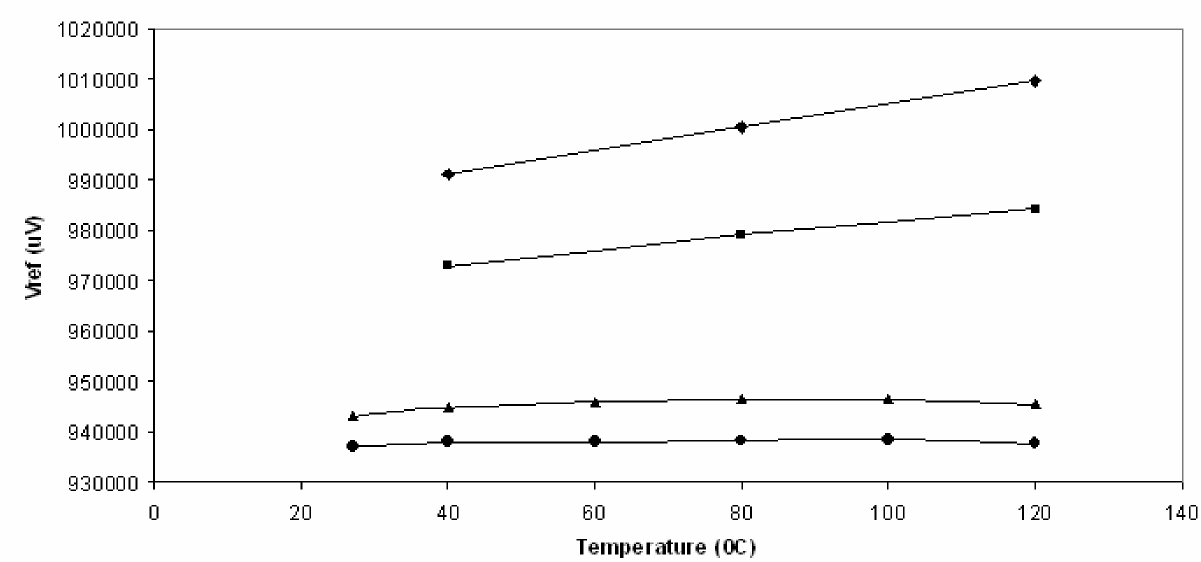

Fig.7 Experimental results (Trimmers).

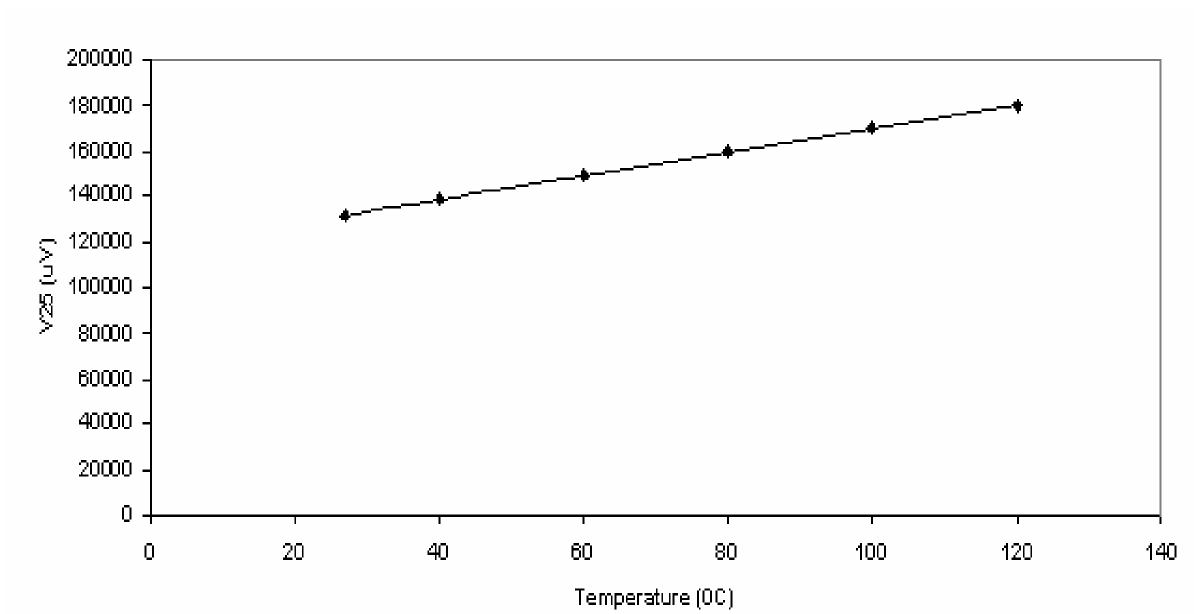

Fig.8 V25(μV) x Temperature (^{0}C).

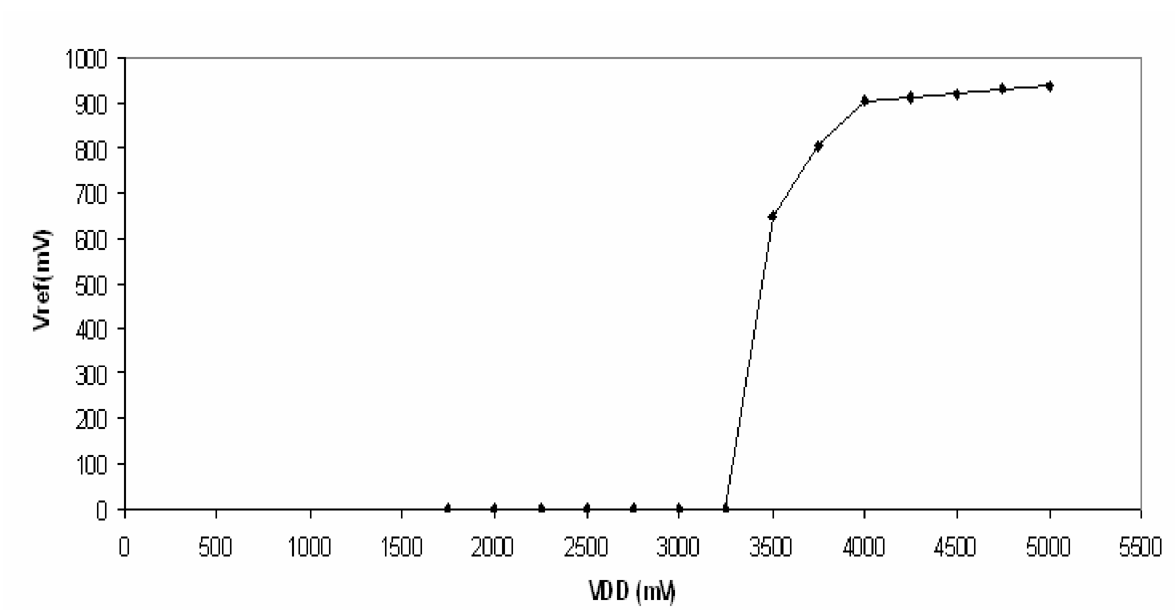

Fig.9 Vref (mV) x VDD (mV).

VI. Proposed Temperature Sensor

The proposed temperature sensor is shown in Fig.10. Its layout is shown in Figs. 11 to 13.

It uses the well defined characteristics of the threshold voltage of the CMOS transistor to generate an output proportional to the temperature. In equation (5) it is shown how the threshold voltage behaves as a function of the temperature. So, the most important part of the circuit is the threshold voltage extractor. It generates its bias current through the transistor M1Vth. In this transistor, the Vgs voltage is the Vgs voltage summation of the transistors M1B and M2B minus the Vgs voltage of the transistor M1A. So, it is possible to obtain equation (14).

$$Vgs_{M1Vth} = \sqrt{\frac{2 \cdot I_{D1}}{\mu.Cox \cdot \left(W/L\right)_{M1A}}} - \sqrt{\frac{8 \cdot I_{D2}}{\mu.Cox \cdot \left(W/L\right)_{M1B}}} + Vth \qquad (14)$$

Analyzing equation (14) it is possible to conclude that using the same aspect ratio in M1A and M1B and a current I_{D1} four times higher than I_{D2} a voltage equal Vth is generated in M1Vth. Another possibility is to use the M1B aspect ratio four times lower than M1A and equal current values in I_{D1} and I_{D2}.

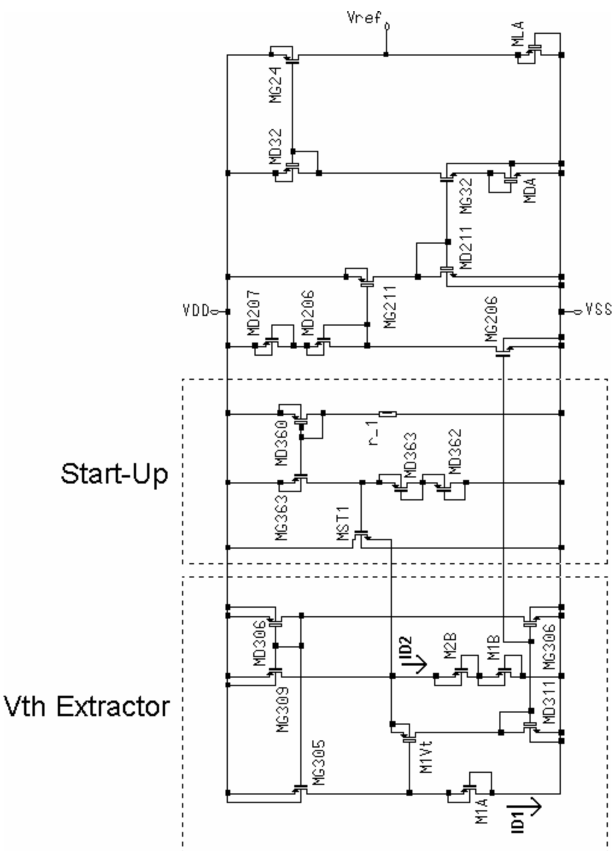

Fig.10 Temperature Sensor schematic.

As the bias voltage is generated inside this circuit and it is not a direct function of VDD, the circuit may not start and it is necessary to use a start-up circuit to guarantee this circuit will work properly.

In Fig.14 is shown the response of the circuit in a range of 27 to 120 degrees Celsius. This variation is equivalent of $1mV/^0C$.

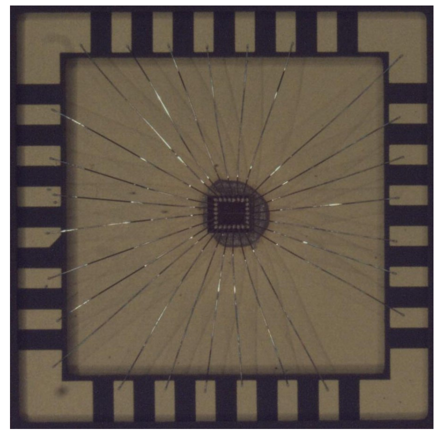

Fig.11 Temperature Sensor layout (View 1).

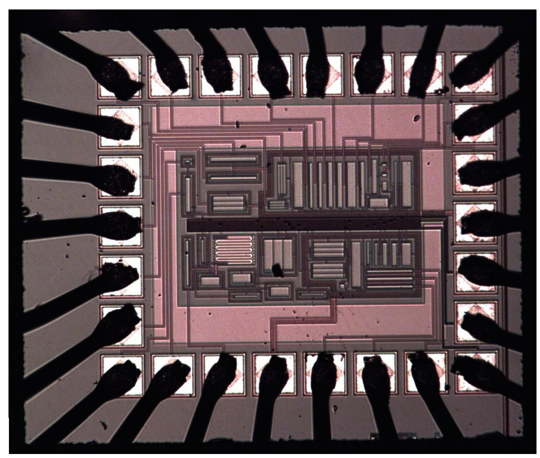

Fig.12 Temperature Sensor layout (View 2).

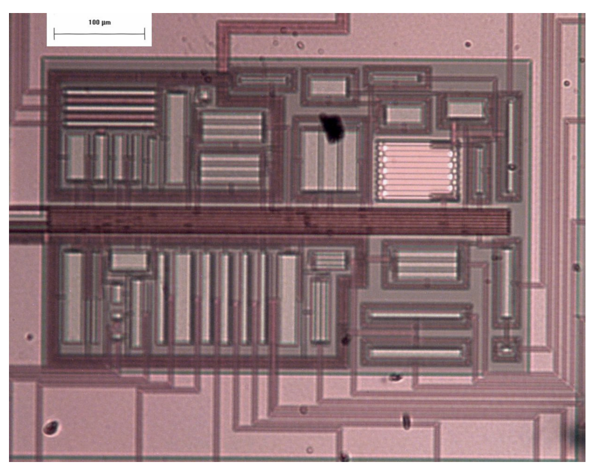

Fig.13 Temperature Sensor layout (View 3).

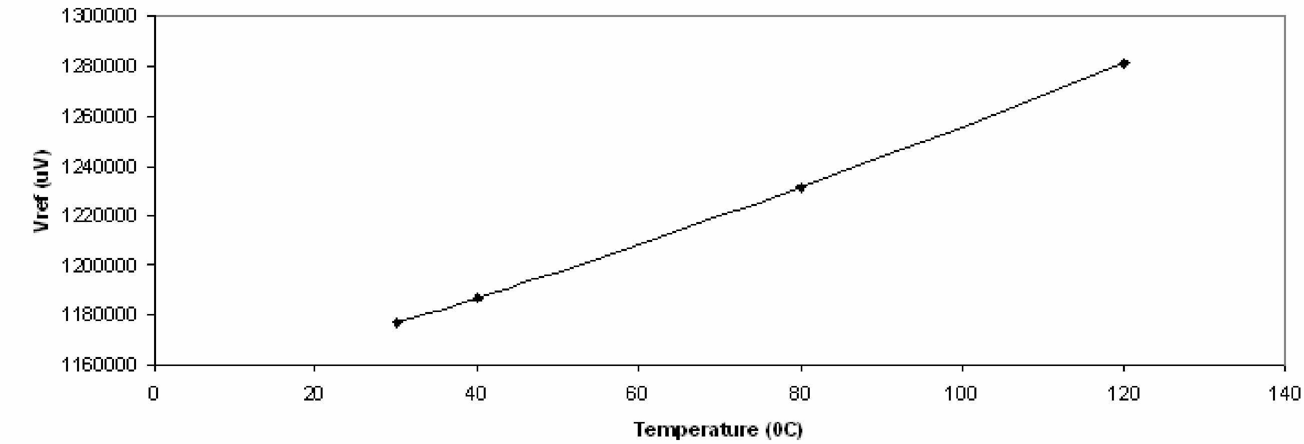

Fig.14 Experimental results.

VII. CONCLUSION

The layout was designed aiming a maximum density to avoid temperature gradients.

In both circuits it was not used ESD (electrostatic discharge) protection in the bonding pads. The reason for that was to avoid any kind of influence from protection devices.

High resistivity poly resistors were used because of two reasons: its low area consumption, and its non-linearity. It was verified in simulations the non-linearity of the poly resistor improves the reference voltage stability in temperature.

The measurements showed that the proposed voltage reference presented a performance comparable to the bandgap references [6].

The temperature sensor achieved a linear response with temperature. This feature shows its potential as an on-chip sensor. The trimmer circuitry can be used to adjust the curve inclination. In the case showed in Fig.14 it was adjusted to a coefficient of $1mV/^0C$.

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