# Low Power Semiconductor Devices at 65nm Technology Node

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***Abstract***: This paper attempts to analyze the performance of 65 nm CMOS device structures for low power applications. It indicates that the historical trend of scaling of MOS devices can be sustained by innovative CMOS Structures such as Ultra-thin body SOI devices and multiple gate MOSFETS (such as FinFETS), that can withstand the adverse effects of Scaling. A particular issue of great concern in logic design is the power dissipation. For high-performance logic with increased leakage currents, chip static power dissipation is expected to become a bottleneck to meet aggressive targets for performance scaling. Innovations in circuit design and architecture for performance management as well as utilization of multiple transistors on chip are required for chip design. Multiple transistors having different threshold voltages ($V_t$) are used selectively with the low $V_t$, high leakage devices being used mainly in the critical paths and higher $V_t$, lower leakage devices being used in the rest of the chip area to control static power dissipation. This paper presents the low static power dissipation CMOS devices at 65 nm technology node and compares the performance of SOI CMOS with the conventional planar Bulk CMOS and establishes that SOI CMOS is better suited for low stand-by power applications. A low leakage current of 0.2 pA/µm for NMOS and 0.1 pA/µm for PMOS was observed for SOI devices at a supply voltage of 1.5V as compared to 10nA/µm for bulk CMOS devices at a supply voltage of 1.2V.

***Keywords***: Bulk CMOS, SOI MOSFET, MOS Scaling and Leakage currents.

## *1. Introduction*

After more than three decades of relentless scaling of CMOS devices to nanometer dimensions for faster circuit operation, higher packing density and lower power dissipation, CMOS technology has now become the prevailing technology for VLSI applications. This scaling is driving the industry towards major technological innovations, including material and process changes such as Metal gates and High- k dielectrics(1) and also new structures such as Ultra-Thin Body SOI and FinFETs. With Scaling of planar Bulk MOSFETs, Significant challenges such as high channel doping, Junction leakage due to band-to-band tunneling and various Short channel effects (SCE) need to be addressed(2). Also, random doping variations in the channel in extremely small MOSFETs lead to variability of threshold voltages (3). Another challenge for highly scaled MOSFETs is the increase in the Source/ Drain series resistance due to shallow junctions [4]-[6]. Due to the challenges with scaling of planar bulk MOSFETs, Novel device structures such as ultra-thin body SOI MOSFETs and multiple gate structures such as FINFETs are becoming attractive alternatives.

SOI CMOS involves building MOSFETs on very thin layers of crystalline Silicon. The thin layer of Silicon is separated from the substrate by a thick layer ( 100- 200 nm) of buried $SiO_2$ film, thus isolating the devices from the substrate. The Subthreshold slope of long channel fully depleted (FD) SOI

MOSFETs can be near ideal 60 mV/dec because the effective gate depletion width is very large and the body effect coefficient given by m, where $m = 1 + 3t_{ox}/W_{dm}$, will be very nearly equal to 1. Fig 2a. Shows the SOI MOSFET structures with 65 nm physical gate length which features 1) A thin Si channel of 50 nm thickness; 2) An increased doping in the source/ Drain extension regions to control the depletion width and 3) an undoped polysilicon gate to control the channel current. The use of thin body over the buried oxide helps in controlling SCEs but the resistance of the channel increases thereby reducing drive currents.

***2. Proposed Devices for low power applications*: ** A major portion of the semiconductor device production is devoted to digital logic. For low power logic, control of static power dissipation with scaling is the critical goal. To meet this goal, transistor leakage current is projected to be much lower than that of high-performance logic. High- performance logic refers to chips of high speed and high power dissipation, such as Microprocessor unit chips. Low power logic refers to chips for mobile systems where the allowable leakage currents are limited by battery life. There are two major categories in low power i.e. Low operating power (LOP) and Low standby power (LSTP) logic [7]. LOP chips are used for relatively high performance mobile applications such as notebook computers and the focus is on reduced dynamic power dissipation. LSTP chips are used for lower performance, lower cost consumer applications such as cellular telephones. LSTP chips are characterized by low operating frequency and lower battery capacity. The main focus of LSTP chips is to have the lowest possible static power dissipation that means lowest possible leakage current. According to ITRS roadmap, the leakage current is projected at 30pA/μm for LSTP chips and is held relatively constant while for LOP, it is 9nA/μm and it increases slowly with scaling.

***3. 65 nm Simulation results and discussion***: NMOS and PMOS devices at 65 nm technology node were simulated using Synopsys TCAD device simulator(8-10). The Drift diffusion carrier transport model was used to carry out the simulations. The maximum supply voltage used for Bulk CMOS device simulations is 1.2V and for SOI MOSFETS it is 1.5V.

***Bulk CMOS***: The Bulk NMOS and PMOS devices at 65 nm were simulated with process enhancements such as retrograde channel doping and Halo implants to control short channel effects [11] .The leakage currents for these devices have been optimized for 10nA/um. The sub threshold slope was found to be approximately 150 mv/dec that indicates slow switching between logic states. Fig .1 shows the structure of the 65 nm bulk devices along with the Id-Vg curves that shows a good on current and an off current of approximately 10 nA/μm.

***Bulk CMOS 65 nm:***

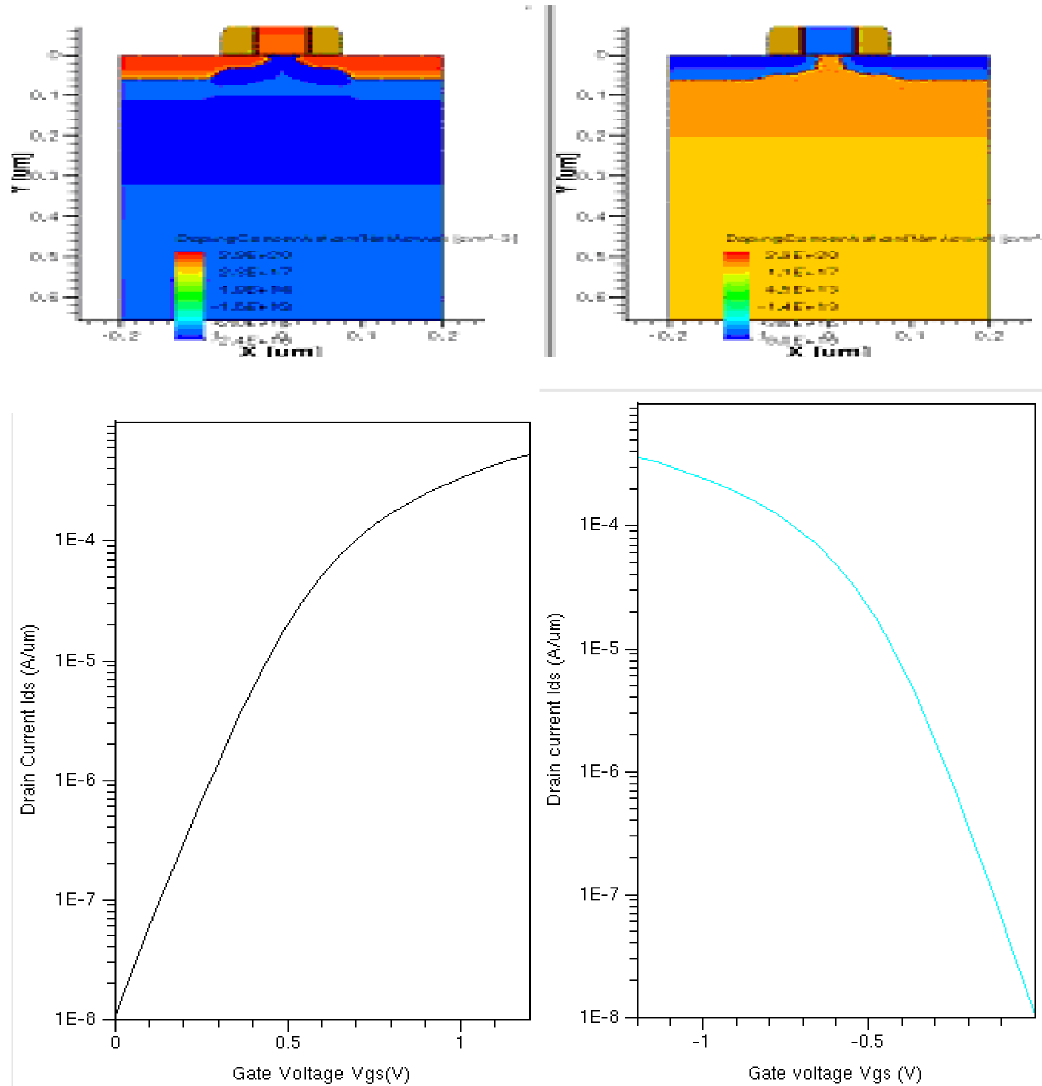


fig.1: Bulk planar NMOS and PMOS device structures with 65 nm gate lengths. The I-V curves show a leakage current of 10nA/µm at a supply voltage of 1.2V.

***SOI CMOS***: Fig .2a shows a 100nm buried oxide layer implanted in the silicon substrate for reduced SCE and a 50 nm silicon body implemented for fully depleted SOI device with minimal doping in the channel for enhanced mobility. A higher doping in the range of 5e+17/cm$^3$ was implemented in the source/ drain extension regions to lower the off current and at the same time maintain the drive current. This doping has been introduced to minimize the width of the depletion layer and to control short channel effects. Different doping levels were introduced and simulated to find the optimum value which lowers the leakage current and also does not reduce the on state drive current. Fig 3a shows a graph of the Leakage current against the Doping Concentrations $N_E$ in the Source/ Drain extension regions . It was found that a Boron Concentration of 7e+17/cm$^3$ was optimum for NMOS and Phosphorus concentration of

$4e+17/cm^3$ was optimum for PMOS. Further increasing the Doping concentration leads to drastic reduction in the drive current as is shown in table 1. A low sub threshold slope of 80 mV/dec for PMOS and 70 mV/dec for NMOS indicates good control of SCEs as seen in Fig.2b. A low leakage current of 0.2pA/µm for NMOS and 0.1pA/µm for PMOS makes these devices suitable for LSTP applications. Due to the thin silicon body thickness for these devices, the resistance in the channel is high resulting in reduced drive currents.

## *SOI CMOS 65 nm:*

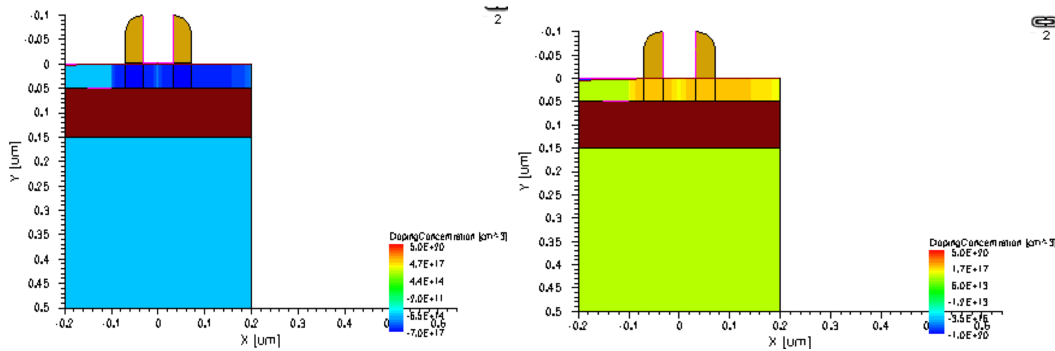


fig.2a: SOI NMOS and PMOS device structures with 65 nm gate lengths.

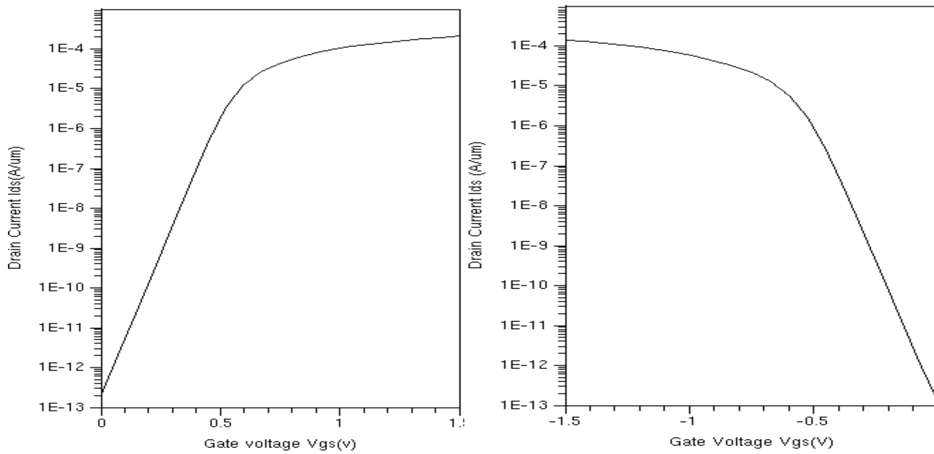


fig.2b: The I-V curves shows a leakage current of a few pA/µm at a supply voltage of 1.5V

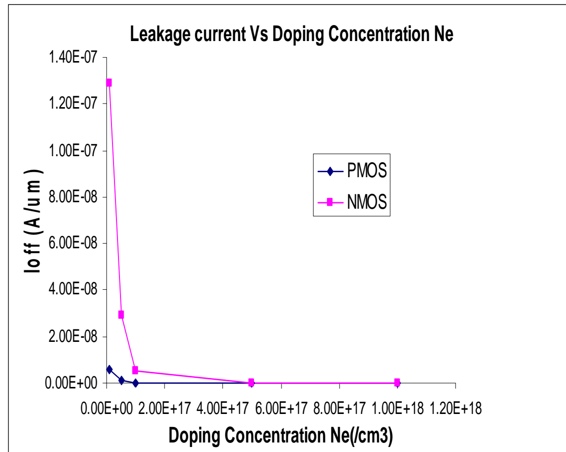


fig 3a. Leakage Current (A/um) Vs Doping Concentration (atoms/$cm^3$) in the Source/ Drain extension regions

Fig 3b. Depicts the variation in threshold voltage with the Doping concentration $N_E$ in the Source/Drain extension regions. This shows that multi threshold voltage devices can be implemented by careful selection of $N_E$ (12). Drain Induced Barrier Lowering (DIBL) is observed to improve with the increase in Doping Concentration as seen in Fig. 4, thus indicating a good control on Short Channel Effects. As seen in Fig.5, the Subthreshold Slope is also shows remarkable improvement with the doping levels. The various values of Leakage Current, Threshold Voltage, DIBL, Subthreshold slope against Doping Concentration $N_E$ has been tabulated as seen in Table1, Table 2, Table 3, Table 4, respectively for PMOS and NMOS SOI devices.

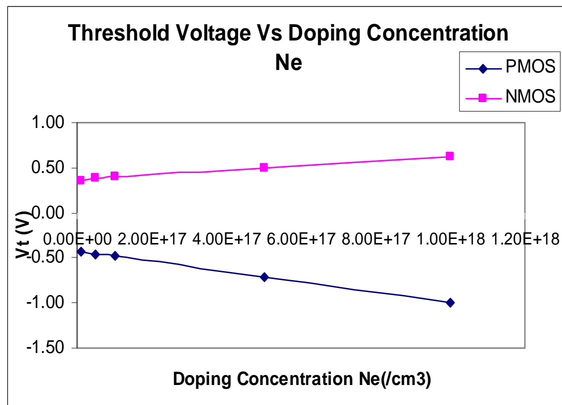


fig 3b. Threshold Voltage (V) Vs Doping Concentration (atoms/$cm^3$) in the Source/ Drain extension regions

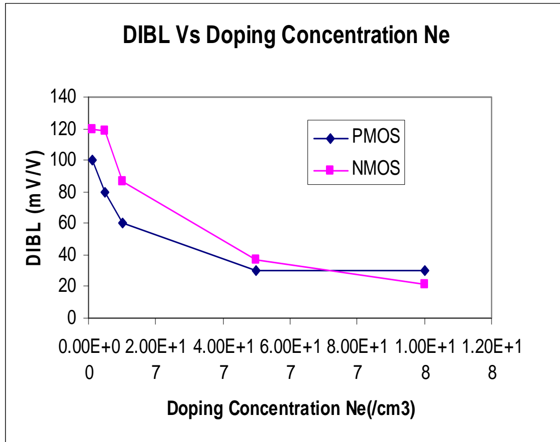


fig 4. DIBL (mV/V) Vs Doping Concentration (atoms/$cm^3$) in the Source/ Drain extension regions

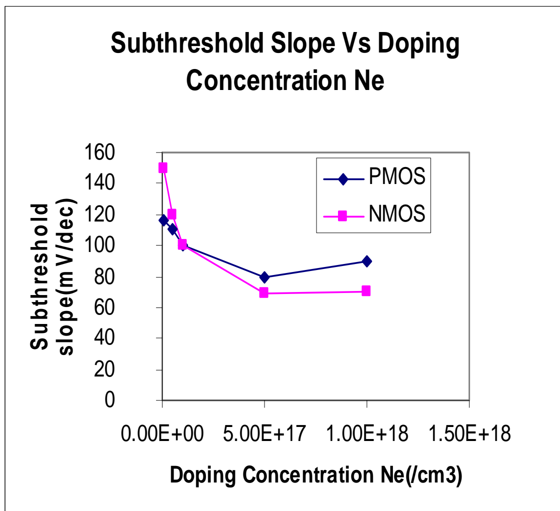


fig 5. Subthreshold Slope (mV/dec) Vs Doping Concentration (atoms/$cm^3$) in the Source/ Drain extension regions

Table 1. A table showing the values of leakage currents Vs the doping concentration for SOI MOSFETS .

| Doping Concentration $N_E$ (atoms/ $cm^3$) | 1e+16 | 5e+16 | 1e+17 | 5e+17 | 1e+18 |
|---|---|---|---|---|---|
| PMOS | 6nA/µm | 1nA/µm | 0.16nA/µm | 0.03pA/µm | 0.002 pA/µm |
| NMOS | 129n A/ µm | 30nA/µm | 5nA/ µm | 1pA/ µm | 0.04p A/µm |

Table 2. A table showing the values of Threshold voltage (V) Vs the doping concentration for SOI MOSFETS

| Doping Concentration $N_E$ (atoms/ $cm^3$) | 1e+16 | 5e+16 | 1e+17 | 5e+17 | 1e+18 |
|---|---|---|---|---|---|
| PMOS | -0.43 | -0.46 | -0.48 | -0.72 | -1.0 |
| NMOS | 0.36 | 0.38 | 0.4 | 0.5 | 0.62 |

Table 3. A table showing the values of DIBL (mV/V) Vs the doping concentration for SOI MOSFETS

| Doping Concentration $N_E$ (atoms/ $cm^3$) | 1e+16 | 5e+16 | 1e+17 | 5e+17 | 1e+18 |
|---|---|---|---|---|---|
| PMOS | 100 | 80 | 60 | 36 | 30 |
| NMOS | 119 | 117 | 87 | 37 | 21 |

Table 4. A table showing the values of Subthreshold Slope (mV/dec) Vs the doping concentration $N_E$

| Doping Concentration $N_E$ (atoms/ $cm^3$) | 1e+16 | 5e+16 | 1e+17 | 5e+17 | 1e+18 |
|---|---|---|---|---|---|
| PMOS | -0.43 | -0.46 | -0.48 | -0.72 | -1.0 |
| NMOS | 0.36 | 0.38 | 0.4 | 0.5 | 0.62 |

## 4. Conclusion:

65 nm P-channel and N-channel fully depleted SOI Devices with a body thickness of 50 nm were simulated and compared with bulk planar NMOS and PMOS devices for low power applications. It was found that SOI devices require very light doping in the channel and short channel effects are controlled better in spite of lower channel doping. To control the short channel effects and to reduce the leakage currents, a constant doping in the range of 5e+17 was introduced in the source/drain extension regions. This was found to be effective in reducing the off currents. The off current for the SOI devices are about a few pA/µm whereas for bulk devices it is in the range of nA/µm. Thus it is shown in this paper that these low leakage current SOI devices can be used for LSTP chips used in mobile applications. Further, To improve the drive current Strained Silicon Channels may be used.

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