Phasor Measurement Unit Reliability Enhancement Using Real-Time Digital Filter

A. Ouadi, H. Bentarzi, and J. C. Maun

***Abstract*—**Phasors and frequency of three-phase power system may be measured with high speed and accuracy using modern power instruments such as Phasor Measurement Unit (PMU). However, this accuracy may be affected by several power disturbances such as fast and slow dc offsets decaying due to sudden current changes, inter-harmonics, etc. To avoid these effects for improving the quality of measurements, this work proposes a new method of real-time filter for removing the unwanted DC offset and hence improving SDFT algorithm. To validate the present method, the performance of developed PMU is tested using the data generated by Simulink/MATLAB simulator. The obtained simulation results are very encouraging.

***Keywords*—**Power system, Phasor Measurement Unit, Real-time digital filter, SDFT algorithm.

I. Introduction

THE Accurate and fast measurement of the phasors of the fundamental components and frequency in three-phase power systems that may be investigated by a Phasor measurement unit (PMU) is very important in modern power instruments/meters, digital relays, control apparatus, and power quality analyzer (PQA). In PMU instrumentation and relaying scheme, discrete Fourier transform (DFT) is the most widely used filtering algorithm [1-3] for computing the fundamental frequency components. However, The fault currents of a transmission line may contain a DC offset which decays exponentially with time (time constant of the line inductance to resistance ratio L/R), or a large number of unwanted sub-synchronous frequency or decaying DC components due to the thyristor-controlled switched capacitor (TCSC) compensated lines [4]. This latter always needs few cycles for decaying DC component or 10– 20 cycles for sub-synchronous frequency component to obtain the accurate fundamental phasors by discrete Fourier transform DFT algorithm. From the evaluation performed using the ideal network [5], the DC offset may have an effective impact on the Fourier algorithm and if no correction is applied, the relative error of the real amplitude from the Fourier algorithm may reach 20%, which purely caused by this decaying offset. For a high performance control and protection applications such a large relative error is not allowed. The performance of the techniques employed directly determine the functions of this equipment and affect their behaviors under various service conditions. Hence, the real-time accurate phasor measurement of the fundamental component and/or symmetrical components is essential and crucial to the safe and economic running of modern electric power systems [6], [7].

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For an ac input signal that is associated with a DC offset component, a constant DC and exponentially decaying signal, Gu and Yu [8] propose a modified Fourier filter algorithm using a data window of one cycle plus two samples to compute and perform compensation to remove the unwanted DC offset. The idea behind this algorithm is that the decaying component can be completely removed from the original signal once its parameters are determined. The weakness of the proposed algorithm is that more calculation is needed for eliminating the DC offset. The data window is relevant when implementing this algorithm for the real-time application. A digital mimic filter has been proposed [9], to suppress the effect of an exponentially decaying component over a wide range of time constant (0.5 to 5 cycles and larger) and then apply the DFT algorithm to compute the phasors. A good performance is obtained with this mimic filter when its time constant is identical to the time constant of the exponentially decaying DC component. Another way where the Taylor series expansion is used to approximate the decaying direct component, then the fundamental phasors are estimated by means of curve fitting technique, using least error squares [10]. To enhance the computation speed, the recursive least squares computation curve fitting algorithm is introduced [11]. In addition, a DFT algorithm and least error square technique are combined to estimate the phasor without DC offset signal. Another method was proposed to identify the magnitude and the time constant of the decaying DC offset component [12]. In this method, the residual terms caused by some harmonics are ignored in the estimation procedure. The assumption that these residuals are negligible should not be taken for granted, and needs to be investigated further [5]. The performance of Kalman filters is evaluated in [9]. It was concluded that the third-order Kalman filter is sensitive to variations of the DC offset time constant. A kalman filter should only be superior in removing the DC-offset if its time constant is the same as one modeled in the state transition matrix [9].

This work proposes a method that can correctly extract the phasors of the fundamental components as well as symmetrical components from voltage or current waveforms and then estimate their instantaneous amplitude, phase angle, and frequency with good accuracy and in real-time, even when disturbances occur in large scale and complex power systems. The proposed algorithm is a real-time processing system since a sample by sample basis instead a frame or cycle basis (data window) to obtain the accurate fundamental phasors. This is to fulfill the high-speed measurement and detection feature required by the PMU and other applications such control and protective system [13], [14]. The approach consists first of removing unwanted dc components of the input measured signal using a fast digital filter algorithm, which is suitable for such a real-time application, and then provide the filtered signal to the Smart DFT [15] algorithm to accurately generate the filtered phasor measurement components as shown in Fig.1

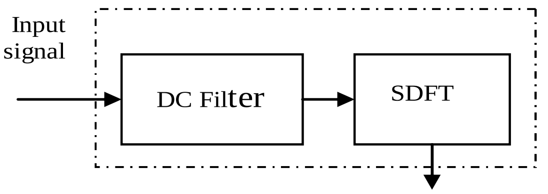


Figure 1 PMU enhancement computing algorithm

II. DC Offset Removal Filter

Three real-time digital filters are generally used for DC components removal as shown in Fig.2 [16].

Ignoring the constant gains of those DC-removal filters, all three filters have identical performance with the general DC component removal filter structure. Their characteristics can be obtained from a z-domain transfer function:

$$H(Z) = \frac{Y(Z)}{X(Z)} = \frac{1 - Z_{-1}}{1 - \alpha Z_{-1}} \quad , \qquad (1)$$

It is not immediately obvious that the filters in Fig.2(c) and (d) are equivalent [16]. We can verify that equivalency by writing the time-domain difference equations relating the various nodes in the feedback path. After that, those equations will be converted to z-transform expressions and solved for obtaining Y(z)/X(z). If the last DC-removal filter model (Fig.2(d)) is chosen, the general filter's frequency magnitude and phase responses may be provided as shown in Fig.3 (a) and (b) with α = 0.95.

The filter's pole/zero locations are given in Fig.3, where a zero resides at z = 1 providing infinite attenuation at DC (zero Hz) and a pole at z = α making the magnitude notch at DC

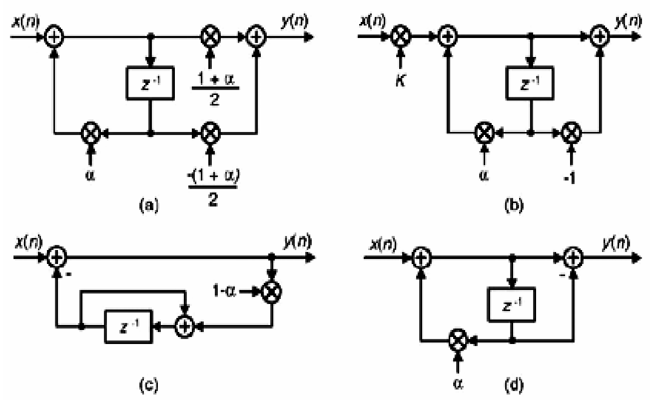
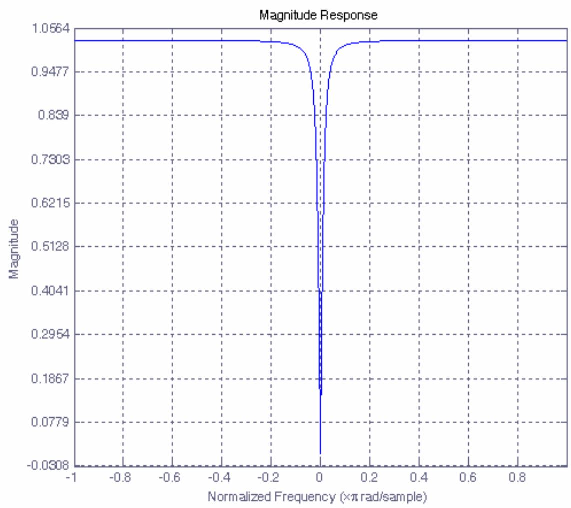


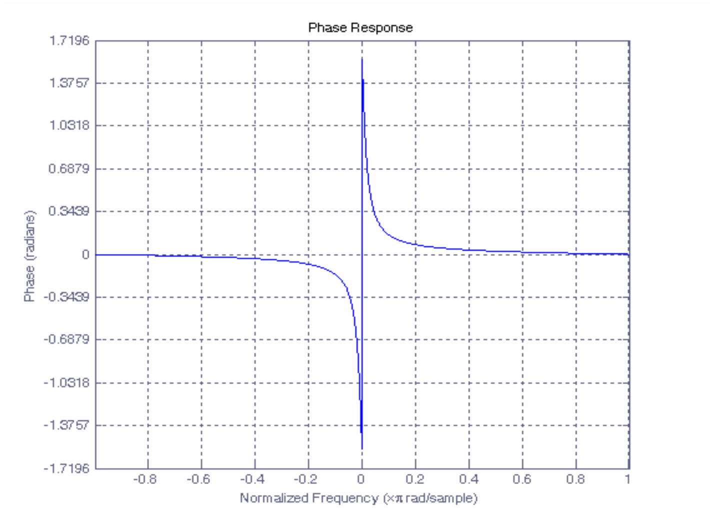
Figure 2 Filter structures for DC offset removal.

very sharp. The closer α is to unity, the narrower the frequency magnitude notch centered at zero Hz. Fig.3(d) shows the general filter's unit-sample impulse response.

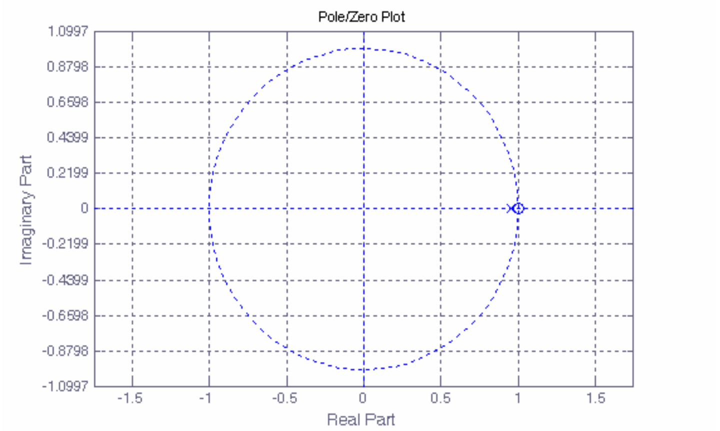
Figure 3 shows the time-domain input/output performance of the general DC-removal filter (with α = 0.95). When filter input is fed by a sinusoid suddenly contaminated with a low frequency DC signal (solid line), that is thee fundamental components decaying exponentially having a long time constant of about five cycles, its output (dashed line) decays exponentially but with short time constant. The amplitude overshoot appears for short duration (portion of a cycle) with a small steady state error.

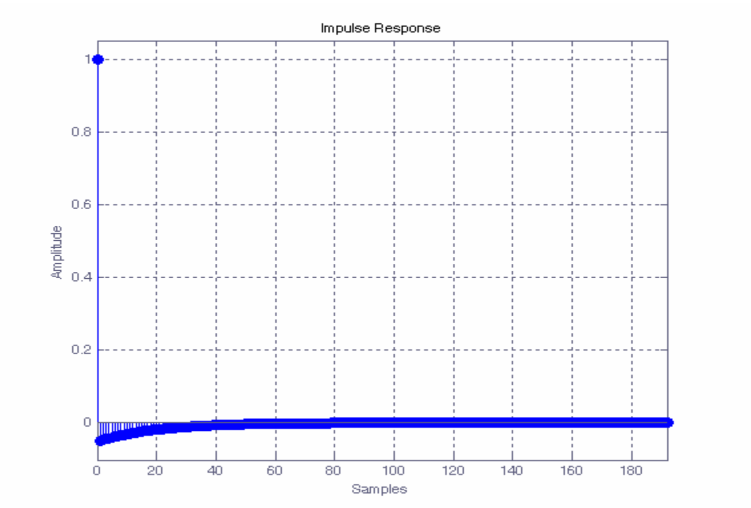


(a)



(b)





(d)

Figure 3 DC removal filter, α = 0.95: (a) magnitude response,(b) phase response, (c) pole/zero locations; (d) impulse response.

The filter consists of two processing blocks: the integral-differentiator first order IIR filter block for removing dc offset and an all-pass filter for the group delay equalization or phase shift compensation.

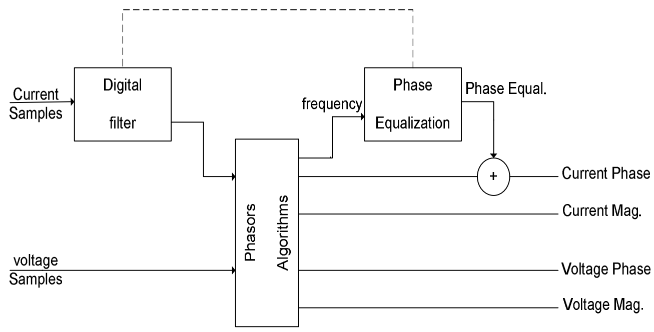


Figure.4 Phase equalization in frequency domain.

This latter block can be cascaded with the first block filter, to alter the phase response while leaving the magnitude response unaffected. Several techniques may be used for an optimal design of a group delay or phase equalization filter over the pass band interval of the main filter, for application where the time domain signal is of importance. In fact, this method is relatively complicated and need more computing power.

However, for frequency domain application the frequency of the signal is known, the phase equalization may alternatively be computed where simple operations are used to adjust the phase shift. As shown in Fig.9 after the current samples are filtered out by means of the IIR filter, the output samples feeding the phasor algorithms to determine the magnitude and phase of the measured signal at the fundamental frequency as well as the frequency deviation.

III. PMU Algorithm

The smart discrete Fourier algorithm (SDFT) [6] has been used in PMU as well as in digital relays, which has the ability to track the phasor values of voltage and current synchronously on power system in real time. PMU is a crucial to the detection of disturbances and characterization of transient power swings [1]. The proposed scheme uses the sample by sample basis instead a frame or cycle basis (data window) to obtain the accurate fundamental phasors. This is to fulfill the high-speed measurement feature required by the PMU. Besides, a developed algorithm must harmonize high frequency sampling and low frequency correcting computations to meet the communication requirements of data transfer rate between the PMU and the data center [15].

The SDFT can be mainly described by considering a sinusoidal input signal (current/voltage) of frequency offset in the following form [17] (see appendix):

$$x(t) = \sqrt{2}X\sin[2\pi(f_0+\Delta f)t+\varphi], \qquad (2)$$

Where X : the effective value of the input signal,

f_0 : The nominal frequency,

Δf : The frequency offset,

φ : The initial phase angle of the input signal

The signal is conventionally represented by a phasor,

$$\bar{x}(t) = X \; e^{j(2\pi \; \Delta f t + \varphi)} \;, \tag{3}$$

Assuming that x(t) is sampled N times per cycle of the f_0(Hz) waveform to produce the sample as follows :

$$\tilde{x}(t) = \sqrt{2} X \sin\left[2\pi (1 + \frac{\Delta f}{f_0}) \frac{k}{N} + \varphi \right] \tag{4}$$

The original phasor is then calculated according to the recursive DFT algorithm as follows [6]:

$$\hat{x}(r) = \hat{x}(r-1) + j\frac{\sqrt{2}}{N}\left[\tilde{x}(r+N-1) - \tilde{x}(r-1)\right] e^{-j\frac{2\pi}{N}(r-1)} \tag{5}$$

By defining θ as.

$$\theta = \frac{2\pi \; \Delta f}{f_0 \; N}$$

And Assuming that the sampling rate is m times of the correcting computation frequency, the exact solution of phasor can be obtained by the following equations:

$$\bar{x}(r) = \left[\hat{x}(r) + C_2(r)\right] \frac{N \sin(\theta/2)}{\sin(N\theta/2)} e^{-j\theta(N-1)/2} \tag{6}$$

Where,

$$C_2(r) = \frac{\hat{x}(r-m) - \hat{x}(r)\alpha_{-m}(\theta)}{\alpha_{-m}(\theta) - \alpha_m(\theta) e^{j\frac{4\pi}{N}m}}$$

.

and,

$$\alpha_{-m}(\theta) = f(r-2m) + \sqrt{\left[f(r-2m)\right]^2 - e^{j\frac{4\pi}{N}m}}$$

The frequency can be estimated from the following [18]:

$$f(r-2m) = \frac{\hat{x}(r-2m)/\hat{x}(r-m) + e^{j\frac{4\pi}{N}m} \; \hat{x}(r)/\hat{x}(r-m)}{2} \tag{7}$$

IV. PMU Implementation with DC Offset Filter

Mainly PMU use a synchronized measurement system together with its major components as shown in Fig.5 [19]. The primary power system voltages and currents are transformed by potential and current transformer (PT and CT) filtered by analog anti-aliasing filter, and then converted

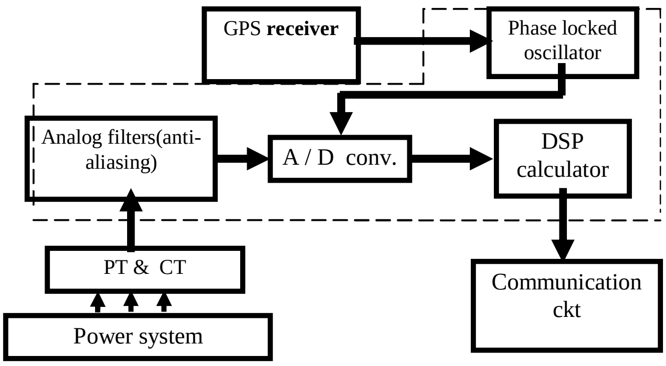


Figure 5. Functional Block Diagram of the

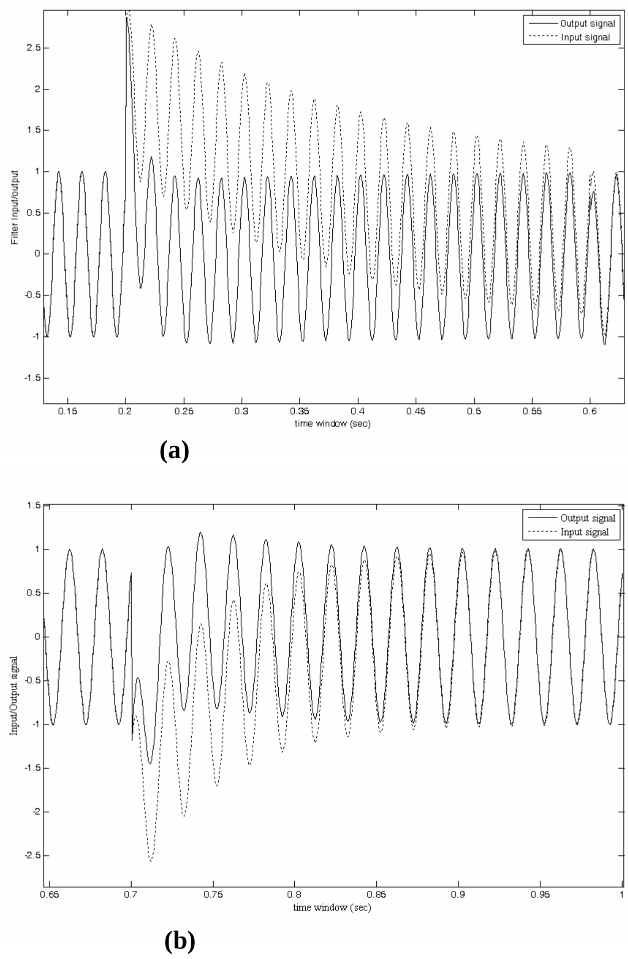


Figure 6 Filter dc removal performances: (a) transient positive and (b) negative dc input signal and filtered output signal.

by A/D converters at sampling clock synchronized by external 1PPS GPS receiver clock.

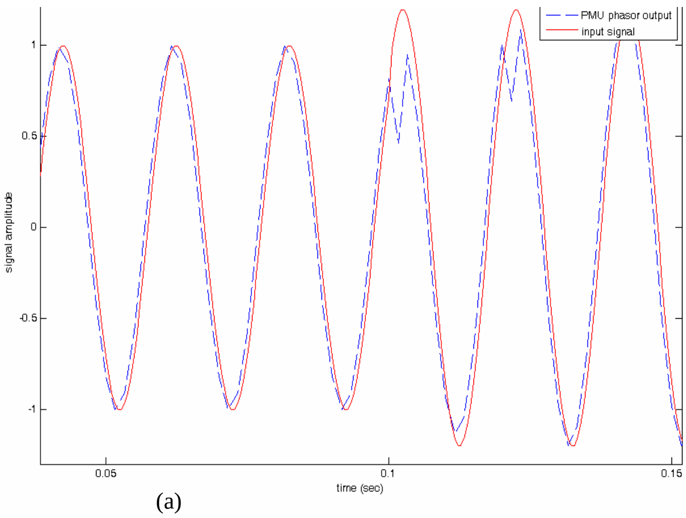
Simultaneous measurements have important benefits as they can be used to analyze the network and form an instantaneous picture of the network which is the basis for all network monitoring, protection and control functions.

Simultaneous sampling of input signals (voltages and currents) are used for computing the phasors and frequency from the sampled data.

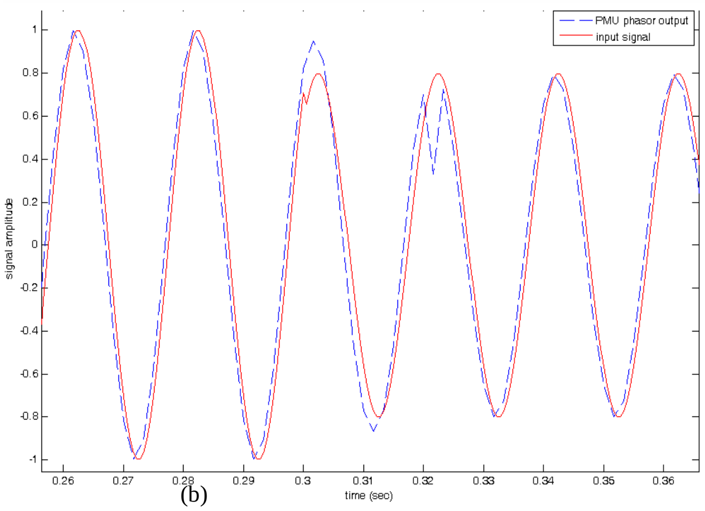
A synchro-phasor is estimated from data samples using a standard time signal as the reference for the sampling processor for the whole system. In our case, the phasor values from remote sites have been determined using common phase relationship.

Synchronized phasor measurements may have the following properties [7]:

- Phasor technology provides time-synchronized data,
- The precise timing of the phasor data makes it useful beyond the local bus,
- Phasor measurements directly provide the phase angles at the high sub-second rate.



(a)



(b)

Figure 7 Change of signal magnitude from nominal level to (a)+20% and (b) to -20%.of the nominal level.

V. PMU Performance Tests

To ensure the reliability of PMU operation, steady state as well as dynamic tests may be undertaken in the developed PMU with new techniques implementation. The performances of a proposed PMU algorithm are tested under transient and dynamic power system conditions, which is important for the protective relaying applications as well as generating of accurate phasor components in the case of wide area measurement system [20], [21].

PMU testing bench consists of PC associated with acquisition card for generating test signal, signal conditioning circuit, and multi-meter.

The experiments have been performed for testing the developed PMU under different conditions such as frequency and amplitude variations. In the first and second case, significant step variation for either magnitude or frequency is applied as shown in Figs.6 and 7 for a time scan of 1 second.. However in the last case, significant step variation for both magnitude and frequency are applied as shown in Fig.8

A. .Amplitude Step Change Response

PMU performance can be determined from response to amplitude step changes that includes voltage/current signal. Step response can be characterized by rising time, overshoot, and steady state error.

.For a phasor input ranges from steady state nominal signal level at nominal frequency (50 Hz) to the magnitude that is instantly changed to +20% of the nominal signal level (Fig.6-a). After a short time, it is changed instantly back to nominal. The test signal is also repeated for 80% of the nominal magnitude as shown in Fig.6-b.

It can be noted that overshoot is very small and the amplitude ranging for both positive signal variation +20% from the nominal and negative variation -20% is of small duration (less than half cycle) as shown in Fig.6.

B. Frequency Step Change Response

Method for determining PMU performance in response to frequency step changes may be investigated by applying a steady state signal at nominal frequency (50 Hz), then instantly changing the frequency to 51 Hz and back after settling time. The test signal is repeated for 49Hz as shown in Fig.7. Step response can be characterized by rise time, overshoot, and steady state error.

It can be noticed that overshoot is very small and the ranging of amplitude for both positive frequency variation (+1Hz) and negative frequency variation (-1Hz) at off nominal frequency (50 Hz), is of small duration (less than a half cycle).

C. Amplitude and Frequency Variations

A complementary worst case waveform senario is developed for PMU performance testing where both step amplitude and frequency variations are present simultaneously. In this case, significant step variation for both magnitude and frequency are applied as shown in Fig.8 for a time scan of 1 second.. The step frequency changes is subjected to variations $50<f<56$ Hz and the signal magnitude is subjected to variations for 4 level step changes from nominal value as shown in Fig.8. It can be noticed that measured values by the PMU, the phasor computed for each sample and not for one cycle, when the variations applied to both frequency and amplitude, are in a good agreement with the actual ones in the time domain even when the frequency offset Δf is high and step amplitude occur at same time. A good accuracy is obtained after one cycle after the step change takes place.

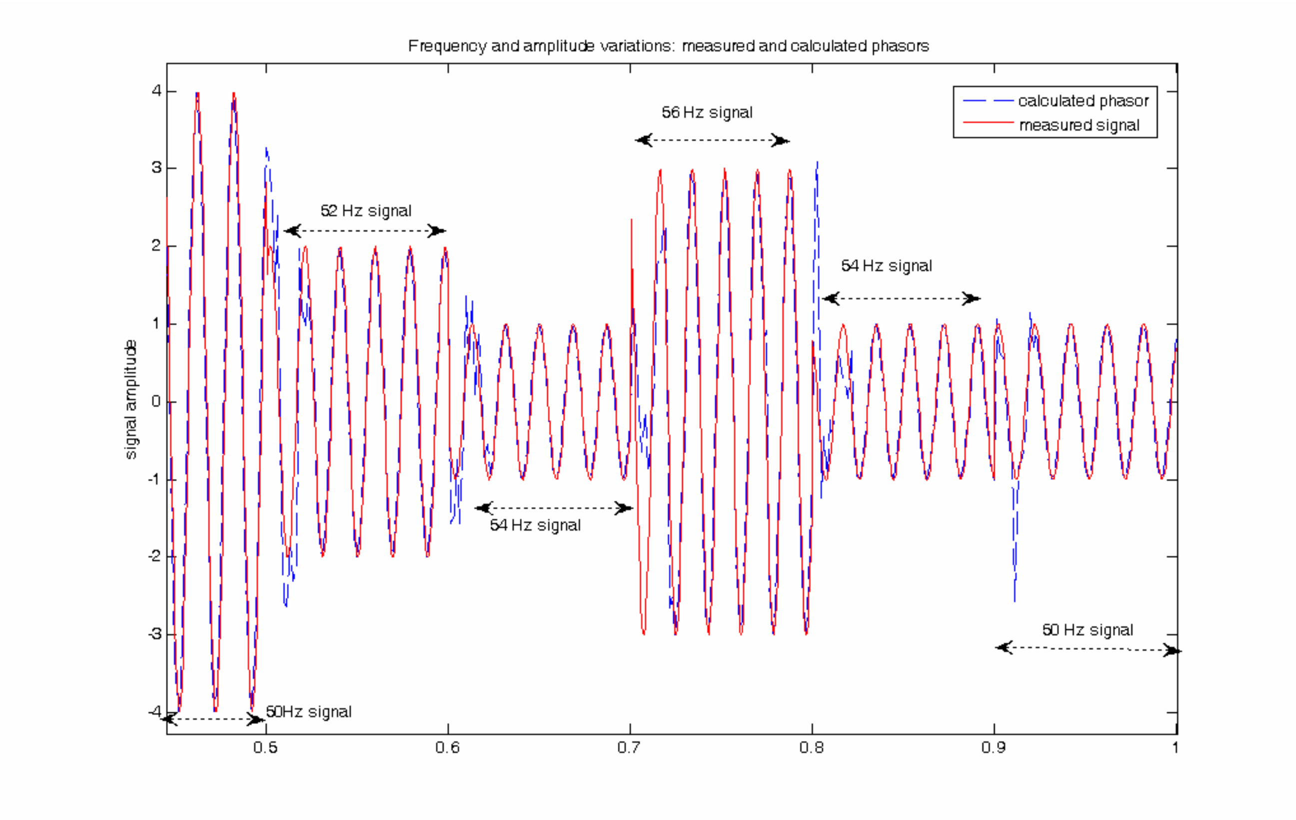


Fig.ure 8 Signal magnitude and frequency step changes from nominal levels.

VI. Conclusion

The power signal frequency is usually near 50 Hz and constantly changing. The phasor derivation technique needs to produce an accurate measurement of amplitude and phase at 50 Hz, and a range of frequency around 50 Hz. The typical amount of deviation from 50 Hz and the rate of change depend on the power system. The unwanted DC offset (due to switching actions, post fault and other power system disturbances) in the power signal can affect on the measurement process. Many techniques have been developed for removing this DC offset. In our work, the modified phasor algorithm pass band around 50 Hz has bee developed and implemented for measuring the signals of interest.

The PMU is tested by applying to it a fault current signal generated by computer simulation. The obtained results show that the used method is capable of completely eliminating the dc offset and thus greatly improving the performance of the full-cycle DFT algorithm.

Important notes deduced from the test results:

-Sampling at off-nominal frequencies leads to incomplete sample sets.

-Even though the amplitude of the input signal is constant, the amplitude of the positive sequence phasor attenuates.

-The angle of the phasor is directly proportional to the frequency.

-When the amplitude is variable and the frequency is kept constant; the measured angle will not undergo changes.

- if the DC offset is removed, more accurate results can be achieved and errors may be reduced.

Finally, the performance of the proposed PMU algorithm has been tested under real transient and dynamic power system conditions, which is important for the protective relaying applications. These tests have been performed for signals as function of time by varying magnitudes and/or frequencies and including DC offset. It can be noticed that the PMU tests results are very encouraging.

Appendix

The synchrophasor representation X of a signal x(t) current or voltage is the complex value given as follows [22]:

$$X = X_r + jX_i , \qquad \text{(A1)}$$

or,

$$X = (X_m / \sqrt{2})(\cos(\phi) + j\sin(\phi))$$

Where $(X_m / \sqrt{2})$ is the RMS value of the signal x(t), and ϕ is the instantaneous phase angle of x(t)

Assuming that the signal $x(t)$ is sampled N times per period of 50Hz waveform to generate the sample set:

$$x_k = X_m \cos\left(\frac{2\pi}{N} k\left(1 + \frac{\Delta f}{f_0}\right) + \varphi_i\right) \qquad \text{(A2)}$$

The original phasor ($\Delta f = 0$) $\bar{X}$ is given by:

$$\bar{X} = \frac{\sqrt{2}}{N}(X_c - jX_s) \qquad \text{(A3)}$$

where:

$$X_c = \sum_{k=1}^{N} x_k cos\left(\frac{2\pi}{N}k\right)$$

and,

$$X_s = \sum_{k=1}^{N} x_k sin\left(\frac{2\pi}{N}k\right)$$

The conventional phasor representation of a sinusoidal signal that it is related to the fundamental component of its DFT can be given by:

$$\bar{X} = \frac{1}{\sqrt{2}}(X_s - jX_c) \quad \text{(A4)}$$

If X_k is the sequence obtained when sampling x(t) at sampling frequency fs = N*fo (N: is the sampling rate), then the recursive DFT of X_k is :

$$X_{rk} = X_{rk} -1 +(2/N)(X_k - X_{k-N})\cos(k) \quad \text{(A5)}$$

$$X_{ik} = X_{ik} -1 +(2/N)(X_k - X_{k-N})\sin(k) \quad \text{(A6)}$$

With:

0 =< k =< N-1

Where:

X-1 ,X-2 ,…………………X-N and Xr-1,Xi-1 are set to zero.

The RMS value of the amplitude and the phase angle of the phasors can be obtained as follows:

$$X_{RMS} = (X_r + X_i)/2 \quad \text{(A7)}$$

$$\phi = \arctan(Xi / Xr) \quad \text{(A8)}$$

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