Impact of rise time driving signal and mismatch threshold voltage MOSFET’s in parallel connection of Push-Pull Power Inverter

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Abstract—Analysis of the dynamic sharing currents at turn-on process in power PWM inverter system with switching Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFET’s) connected in parallel is presented. The inverter circuit presented in this paper is low power inverter which can be used as a charger too. The influence of the different rise time driving signals and parameters mismatch between parallel MOSFET branches, over wide operating ranges is analyzed, resulting in dynamic currents, transition energy unbalance, time delay on switching process of parallel MOSFET’s, and time delay at output voltage of inverter. One of many potential causes of mismatch parameters is the threshold voltage $V_{th}$. Results are presented for the time delays during On switching of the parallel branches in inverter with five power MOSFET’s in each of two legs, selecting same threshold voltage initially, for various rise time driving signals of the two legs of inverter when only one MOSFET in particular leg has lower threshold voltage than others.

Keywords—Dynamic current, Mismatch parameters, PWM-Pulse Width Modulation, Rise time, Switching, Threshold voltage, Time delay.

I. INTRODUCTION

PWM inverters are widely used in industrial applications such as: induction heating, frequency converter, standby power supplies, uninterruptible supplies and the induction machine speed control.

For each inverter many technical and economic parameters are important, such as: DC input voltage ($V_i$), AC output voltage (effective value $V_o$), input current $I_i$, output current $I_o$, frequency of oscillator, power of the inverter, speed of transition from DC to AC and vice versa, power dissipation of inverter and cost etc.

Block diagram of single phase of power inverter is presented in Fig.1.

The inverter circuit presented in this paper is low power inverter (about 1kW).

Most inverters operate performing two main functions: first they convert the DC from battery into AC, and then they step up the resulting AC to main voltage level using a transformer.

The Push Pull PWM inverters use a basic circuit scheme as shown in Fig. 2.

DC voltage from the battery is converted into AC by using a pair of N parallel power MOSFET’s on each leg. The positive 12V DC from the battery is connected to the centre-tap of the transformer primary, whereas each parallel group of MOSFET’s is connected between the edge of the primary transformer and the ground.

When 5 x $Q_t$ (top leg), are turned On, the battery current flows through the upper half of the primary transformer and to ground via 5 x $Q_b$. By switching on 5 x $Q_b$ instead, the current will flow in the opposite direction through the lower half of the primary transformer and to ground. Therefore by switching On the two MOSFET’s legs alternatively, the current is made to flow first in one half of the primary transformer and then in the second one, producing an alternating magnetic flux in the transformers core. As a result, according to the principles of transformer we have on the secondary winding a rectangular wave AC voltage of around 650V peak to peak.

The output voltage regulation is achieved by varying the width of the driving pulses of MOSFET’s, and hence the RMS value of the output voltage. It is usually done by having a
feedback system (Fig. 2) which senses the inverters output voltage. When this feedback senses that the output voltage began to decreased, the MOSFET driving circuit inverters acts to increase the width of the pulses which turn On the MOSFET’s. The MOSFET’s turn On for longer time at each half-cycle, automatically correcting the RMS value of the output voltage in order to compensate any drop in peak-to-peak output voltage. However this regulation is limited in keeping the RMS value close to constant for a long time, because the battery is discharging continuously up to the limit allowed, then additional circuits to disconnect driving circuit is needed.

To realize DC-AC inverter that delivers high power, more parallel connected power transistors are used in each leg, to share leg’s current.[1]

The MOSFET parameters may exhibit potential mismatch during the fabrication process and the worst case is when we use MOSFET’s from different producers to design an inverter. These parameters include the on-state drain-to-source resistance, threshold voltage, the parasitic capacitance (gate-to-source and gate-to-drain), input-to-output transconductance, etc. [1], [2]. Therefore, when two or more power MOSFET’s are connected in parallel, mismatch between these parameters together with rise time of driving signal, may produce serious unbalance with different inherent thermal effects, time delays during transition from DC to AC and vice versa, and in the same time it may affect inverter’s technical performances generally. In this paper, the threshold voltage ($V_{th}$) is used as mismatch parameter and under this condition also we have experimented with different rise time driving pulses of MOSFET’s.

At first glance, each switching device (MOSFET’s) has only two functional states, an “off-state” and an “on-state”. We have to consider how we get from “off” to “on”, the “dynamic” area of the switching waveform (Fig. 3). The dynamic area is only a fraction of the total waveform, but it is by far the most important when it comes to parallel operation [3], [4].

![Fig. 3 Switching waveforms definition [3]](image)

The aim of this paper is researching the left diagrams (Fig. 3), turn On delays, and turn On (rise time) in parallel connection of MOSFET’s in Power Inverter with mismatch threshold voltage.

II. CIRCUIT DESCRIPTION AND IMPACT OF RISE TIME ON PARALLEL BRANCHES

The schematic diagram of the single phase Push-Pull inverter circuit is given in Fig. 2. It has three parts: the control circuit, two legs of switching power elements connected on parallel, and transformer. The Inverter circuit presented in this paper is a low power and is used as a charger too. The PWM technique selected is main factor for switching rate of MOSFET’s, and time delays in every parallel MOSFET’s of each leg and at output voltage when the regime work of inverter is changed from AC to DC.

There are many PWM techniques to drive the MOSFET’s. The control circuit generates driving signals for MOSFET’s. Here is presented PWM technique with rectangular wave signal with constant frequency of 50Hz.

In Single Phase Push-Pull Inverter with this PWM technique, the mismatch threshold voltage and rise time of rectangular pulses together, are main factors in the dynamic processes in parallel branches.

Analyses are focused in top leg of Push Pull Inverter Fig. 2. For reasons of clarity we have shown the applied drive pulse in top legs of inverter with amplitude 6V and frequency of 50Hz (respectively T=20ms), increasing at a relatively slow rate Fig. 4. The same drive pulse is applied in opposite leg, but with shift phase of 180°.

The value of threshold voltage is an electrical parameter which is determined during the MOSFET fabrication process [5]. Differences between power MOSFET’s parameters for a particular device, may result in exceeding its peak current or continuous thermal rating. Some of mismatch parameters can have more effect on the current unbalance and switching time delay than others. Individual or combined mismatch parameters produce serious unbalances in parallel branches, time delays in individual switching elements, and also in output voltage of inverter generally. From all above mentioned parameters, the threshold voltage is major impact in different dynamic sharing currents and time delays [6], [7]. Also, rise time of driving signal together with mismatch threshold voltages of switching elements are main factors for their different switching time and different dynamic sharing currents [7], [8].

![Fig. 4 Driving pulse of top leg MOSFET’s](image)
When switching devices operated in parallel, depend from load types; the resulting current waveforms of branches are sufficiently different to require either different switching devices or the circuit designer may have to change driving circuit to meet the different requirements.

Table 1. shows the parameter range from the datasheet for the selected power MOSFET’s.

<table>
<thead>
<tr>
<th>Threshold Voltage</th>
<th>ON Resistance $R_{on}$</th>
<th>Input Capacitance $C_{iss}$</th>
<th>Output Capacitance $C_{oss}$</th>
<th>Reverse Transfer Capacitance $C_{rss}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2V-4V</td>
<td>0.025Ω-0.036Ω</td>
<td>Typ 0.03 Ω</td>
<td>Typ 1700pF</td>
<td>Typ 460pF</td>
</tr>
</tbody>
</table>

Table. 1 Parameter range of the selected power MOSFET’s

In this case we consider the switching waveforms of all MOSFET’s on parallel branches, for a typical inductive load.

We assume that the load of output transformer in Fig. 2 is considered in drain circuit of each leg of inverter (Fig. 5), treating the transformer as ideal.

In Fig. 5 is presented this situation for top leg of the inverters, while MOSFET’s driving circuit presented with $V_{ GG}$.

Our focused is in dynamic area during turn On delay and turn On rise time in parallel connection of five parallel MOSFET’s for top legs of Inverter.

Capacitors $C_{gs}$, gate-to-drain, and $C_{gd}$, drain-to-source must be charged through the gate, hence, the design of the gate control circuit must take into consideration the variation in these capacitances [5], [7], [8].

During turn-On, the values of these capacitances are nonlinear and a function of device structure, geometry and bias voltages. The values of these capacitances during the analysis are assumed as constant. Let assume initially, all parallel MOSFET’s of the top leg in Fig. 5 are OFF.

**III. THE CASE WHEN ALL MOSFET’S ON TOP LEG HAVE SAME $V_{ in}$**

At $t=t_0$, the voltage $V_{ in}$ is applied as shown in Fig. 4.

For $t_0 < t < t'$, $V_{ GS} < V_{ th}$ and upper parallel same characteristics MOSFET’s, remains in the cut-off region with $I_{ Di}= 0$, regardless of $+V_{ DS}=12V$ from battery.

The time interval $t_0 < t < t'$ represents the first delay turn-on time needed to change voltage on $C_{ GS}$ from zero to $V_{ th}$. The expression for the first time delay interval $\Delta t'$ is given [7].

$$\Delta t' = t' - t_0 = -\tau \cdot \ln \left(1 - \frac{V_{ th}}{V_G}\right)$$  

(1)

Where,

$$\tau = R_G(C_{ GS} - C_{ GD})$$

According to eq. (1), when all MOSFET’s have same threshold voltage, variation of the first time delays ($\Delta t'$), in terms of various $V_{ th}$ is presented in Fig. 4.

![Fig. 6 Variation of the first time delays in terms of threshold voltages during switching On.](image)

For $t > t'$ with $V_{ GS} > V_{ th}$, five upper parallel power switches start conducting, their drain currents given in terms of ($V_{ GS}$, $V_{ th}$) an be approximated as follows,

$$i_{ Di}(t) = g_m \left(V_{ G} - V_{ th} - V_{ G} e^{-\left(t-t'\right)/\tau}\right)$$  

(2)

Where,

$$g_m = \frac{2\sqrt{i_{ DS} I_D}}{V_{ th}}$$

At $t = t'$, $i_{ Di}$ reaches maximum value of $I_{ DS}$. The time interval

$$\Delta t' = \tau \cdot \ln \left(\frac{g_m V_{ G}}{g_m (V_{ G} - V_{ th}) - I_{ DS}}\right)$$

(3)

represents conducting interval.

When $t > t''$ the drain-currents are nearly constant, consequently than the gate-source voltage is also constant.

Fig. 6 shows that when the MOSFET’s threshold voltage increases, this influences the increasing of the first time delay.

Fig. 7 shows waveforms of driving signal of parallel MOSFET’s and drain currents during the turn-on interval when all MOSFET’s have $V_{ th}=2.5V$.

This situation of dynamic sharing currents on each parallel branch is perfect and all time delays turn On are identically. All dynamic currents of MOSFET’s are sharing proportionally and probability to felt any from them is really zero.
Fig. 7 Driving signal, time delays and currents on five parallel branches with $V_{th} = 2.5\text{V}$

**IV. THE CASE WHEN RISE TIME IS $T_R=0\ \text{[ms]}$ AND ONE OF THE UPPER LEGS MOSFET HAS LOWER $V_{TH}$**

This is an ideal situation; drain current of mismatch MOSFET has fast sloping rate than others and any additional time delay will not appear.

Fig. 8 shows waveforms of driving signal with $t_R=0\ \text{ms}$ and Fig. 9 shows drain currents of five top MOSFET’s during the turn-on interval when all MOSFET’s have $V_{th}=2.5\ \text{V}$

Fig. 9 Time delays and currents on five parallel branches with $V_{th1}=2\ \text{[V]}$, $V_{th2,3,4,5}=2.5\ \text{[V]}$ and $t_R \approx 0\ \text{[ms]}$

**V. THE CASE WHEN RISE TIME $T_R=1\ \text{[ms]}$ AND ONE OF THE UPPER LEGS MOSFET HAS LOWER $V_{TH}$**

In the case when one of the upper legs MOSFET has a lower $V_{th1}$, and other four of MOSFET’s have higher $V_{th}$-s, the first time delay during turn-On $\Delta t_1 = f(V_{th})$ is present in all five parallel MOSFET’s, whereas MOSFET’s with higher $V_{th}$ shows an additional time delay ($\Delta t = \Delta t_1 + \Delta t_2$) which influences in later turn-On time.

Disadvantage of parallel connected MOSFET’s with mismatch threshold voltage is time delays switching On. Time delays switching On of parallel MOSFET’s depend from the values of the threshold voltage, whereas different values of threshold voltage will have impact at the different switching time. When difference of threshold voltage between mismatch branch and other MOSFET’s with same characteristics is near $V_{th1}$ (Fig. 11, Fig. 12, Fig. 13), the MOSFET in mismatch branch turns On before others, and this time delay between switching mismatch branch and others is very short. As shown in (Fig. 13) when the difference between $V_{th1}$ and others is higher, the time delay of switching mismatch branch and others is enhanced. These time delays complicate operation of Push Pull Inverter with parallel branches, because MOSFET with $V_{th1}$ carried more current while other parallel group of MOSFET’s is switching On.

Fig. 10 Driving signal with $t_R=1\ \text{ms}$
VI. THE CASE WHEN RISE TIME TR=2[MS] AND ONE OF THE UPPER LEGS MOSFET HAS LOWER VTH

According to results presented in Fig. 11-Fig. 17, can be concluded following: currents in all parallel branches depend from the values of the threshold voltages, and further increasing of the driver voltage, the different threshold voltages will have impact in the current branches. In branch with lower $V_{th}$, the current branch is higher than in the branches with same $V_{th}$. This is a disadvantage of parallel connected MOSFET’s during turn-On process.

If the power MOSFET’s threshold voltage mismatches, the drain currents may have different sloping rates under the same gate-to-source voltage during the turn-On transient. When four MOSFET’s on parallel connection have higher threshold voltage, then an additional time delay will appear.

When this difference of threshold voltage between mismatch branch and other branches of MOSFET’s with the same characteristics, is near $V_{th1}$ (Fig. 11), the difference between current is small, and it leads in the best inverter performance in sharing currents.

When difference of threshold voltage between mismatch branch and other MOSFET’s with the same characteristics is higher (Fig. 13 and Fig. 17), the difference between peak current on mismatch branch and other currents differ around 4 times.

The typical turn-On waveforms for each MOSFET’s in terms of time, when only one of parallel MOSFET’s has mismatch (lower) $V_{th1}$, are represented in Fig. 11, Fig. 12 and Fig. 13. It is assumed that the inductive load will be held at constant value.
VII. THE CASE WHEN RISE TIME $t_R = 3\, \text{ms}$ AND ONE OF THE UPPER LEGS MOSFET HAS LOWER $V_{TH}$

In Fig. 19 the difference of threshold voltage between mismatch branch and other MOSFET’s with the same characteristics the peak currents differ 1.5 times, while in Fig. 21 the difference of threshold voltage is higher the peak current on mismatch branch and other currents differ 4 times.

When difference of threshold voltage between mismatch branch and other MOSFET’s with the same characteristics is higher (Fig. 13 and Fig. 17), the difference between peak current on mismatch branch and other currents differ around 4 times.

The case when difference of threshold voltage is twice, difference of peak currents is three times.
**VIII. THE CASE WHEN $V_{th1}=2[V]$ AND $V_{th 2,3,4,5}=4[V]$**

The worst case in inverter is parallel connection of different MOSFET on one branch of the leg. This extreme case has effect that it gets 90% of load current and other MOSFET’s currents may be very small or may be cut off all the time Fig. 22- Fig. 24.

The current increasing rate in mismatch branch (Fig. 22) is higher then current increasing rate in the same branch (Fig. 24). As result of this mismatch and different rise time of driving signal the MOSFET in mismatch branch can be damaged in the start of transition from AC to DC-Inverter.
IX. CONCLUSIONS

In high power Push Pull Inverters, power MOSFET’s need to be used in parallel as the main switch. In this paper are analyzed: switching transients, time delays and dynamic current sharing issues during conduction states. During the switching transients, the rise time of the driving signal and threshold voltage have main impact on increasing/decreasing time delays of switching-On MOSFET’s.

By selecting the switching elements (MOSFET’s) for two legs of Push Pull Power Inverter circuits with identical threshold voltage and zero rise time of driving signal, we can design the best performance inverter.

When an individual MOSFET turns on just few milliseconds before the others, the delay of the other is significant and the early turned on MOSFET gets the dynamic current load that can damage it.

When the difference of the threshold voltage between mismatched branch and the other MOSFET’s with the same characteristics is 2V, the difference between peak current on mismatch branch and the other currents differs for around (approximately) 4 times.

The inverter circuit presented in this paper is used as a charger too. The time delays during switching on MOSFET’s contribute on total delays during changing the operational mode from charger to inverter.

On the two legs of the Push Pull Inverter presented in this paper, the parallel connection MOSFET’s with the same parameters must be used.

Since mismatch of the threshold voltage has impact in sharing dynamic currents on parallel branches in two legs of the inverter, during circuit inverter implementation, should not be used the MOSFET’s from different manufacturers.

From simulation results from of sections III-VIII, we see that when the rise time of the driving signal is low, then the current increasing rate in mismatch branch is higher, but the switching time delays in all MOSFET’s are shorter. This situation is undesirable mainly for the mismatch branch and the other currents differs for around (approximately) 4 times.

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From simulation results from of sections III-VIII, we see that when the rise time of the driving signal is low, then the current increasing rate in mismatch branch is higher, but the switching time delays in all MOSFET’s are shorter. This situation is undesirable mainly for the mismatch MOSFET but time transition from AC to DC-Inverter is faster. When the rise time of the driving signal is higher, the time delays of switching all MOSFET’s are higher, but current increasing rate in mismatch branch is lower and time transition AC to DC is lower.

REFERENCES