Modelling and Realisation of a Three - Level P.W.M Inverter Using a D.S.P Controller

H. DENOUN, N. BENYAHIA, M. ZAOUIA, N. BENAMROUCHE, S. HADDAD, S. AIT MAMAR

Abstract— To overcome the limitations in voltage and power conventional two-level inverters and in order to improve the spectrum of the output voltage, multilevel inverters are being widely used. In the first part of this paper, the structure and the model of this power inverter are presented. After that, a SPWM control strategy is developed and implemented. Finally, experimental results are presented using a DSP controller.

Key words— — Multilevel inverter, Neutral point clamping, Numerical control, Pulse-Width Modulation. .

I. INTRODUCTION

Multilevel converters are based on the neutral point clamped inverter topology proposed by Nabae[1]. The multilevel voltage source inverter is recently applied in many industrial applications such as power supplies, static VAR compensatory, drive systems, etc.

One of the most significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing frequency, thus three level inverters can be operated at lower switching frequencies (f_{sw} < 500 Hz) leading to smaller commutation losses and hence higher efficiencies. Moreover they have great interests in overcoming the series connections problems [2]. In fact, the three-level inverter is able to generate voltages without output transformer and its harmonic components are fewer than those of conventional two-level inverters at the same switching frequency. In addition, when the blocking voltage of each switching device is half of the dc-link voltage, it is easy to produce high voltage and power inverter systems.
In recent years huge advances have been made in digital control strategies leading to improving the performances of multi-level inverters and thus spreading their use.

In this paper the modelling and the simulation of a three level PWM inverter are carried out using a TMS320LF2407 DSP controller. Emphasis is made on elaborating the PWM control strategy using this DSP programmed using software developed by Texas Instruments *"Code composer"*. Furthermore, its experimental implementation is performed and the built system is tested. The experimental results are used to validate those obtained theoretically. In addition, the performance of this inverter are analysed with respect to its output voltage contents.

This work was supported in part by ATAGE research laboratory, University Mouloud Mammeri, of Tizi-Ouzou, 15000 Algeria.

Hakim Denoun is with the Electrical and Computer Engineering department at Mouloud Mammeri University of Tizi-Ouzou, Algeria, P.O. Box 17, Tizi-Ouzou, Algeria, Tel:+213555185198; email : akim_danoun2002dz@yahoo.fr). Nacereddine Benamrouche is with the Electrical and Computer Engineering department at Mouloud Mammeri University of Tizi-Ouzou, Algeria University, P.O. Box 17, Tizi-Ouzou, Algeria, (tel : +213772314992; email : benamrouchen@yahoo.fr).

II. MODELING OF A THREE-LEVEL INVERTER

A. General structure

The NPC multilevel inverter uses capacitors in series to divide the DC bus voltage into different voltage levels. To produce m-levels in the phase voltage, an m-level NPC inverter needs m-1 capacitors on the de bus. A three- phase three-level NPC inverter is shown in fig.1. The dc bus consists of two capacitors C. For a dc bus voltage Uc, the voltage across each capacitor is Uc/2 and each device voltage stress will be limited to one capacitor voltage level Uc/2 through clamping diodes [3],[4].

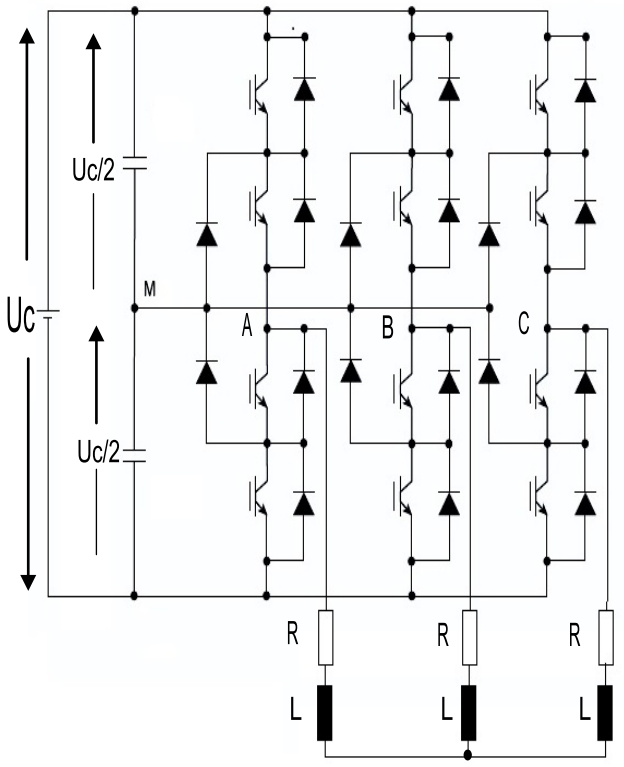

Fig.1. Power circuit of NPC inverter

B. Different configurations of the inverter

To describe the different sequences of the inverter function, let us consider the possible states of the first leg switches fig.2.
The three-level inverter has the advantages that the blocking voltage of each switching device is one half of dc-link voltage whereas full dc-link voltage for two- level inverter.

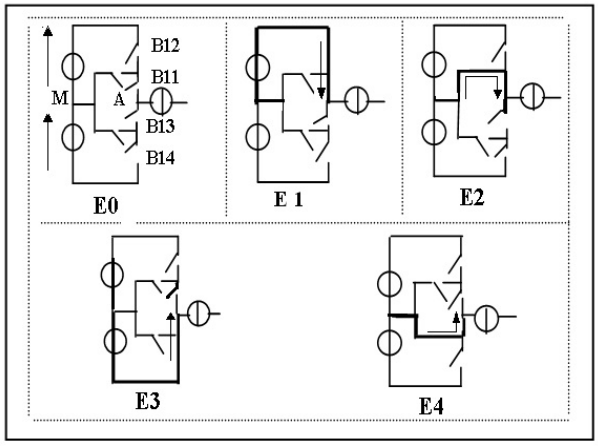

Fig.2. Different configurations of a leg

C. Complementary command

We define the complementary control of the inverter leg as follows [5] :

$$\begin{cases} B_{K1} = \overline{B}_{K4} \\ B_{K2} = \overline{B}_{K3} \end{cases} \quad (1)$$

It was demonstrated [5] that the command given by relationship (1) is the one which gives the three levels U_c , O, $-U_c$, in a optimum way.

Table 1 shows the state of the switches and the corresponding output voltage of the inverter. Where V_k (k = a, b, c) is the potential of the leg.

Table I: Switches states and corresponding voltage

B_{k1}	B_{k2}	B_{k3}	B_{k4}	V_k
0	0	1	1	-Uc2
0	1	0	1	Unknown
1	0	1	0	0
1	1	0	0	Uc1

D. Model control of the three-level inverter - Connection functions

These functions define the state of the switches. They are equal to 1 if the switch is ON and 0 if the switch is OFF. They are defined by following relationship.

$$F_{k1} = 1 - F_{k4}$$
$$F_{k2} = 1 - F_{k3} \qquad (k = 1, 2, 3) \qquad (2)$$

Therefore, the branch voltages V_{AM} , V_{BM} ,V_{CM} are expressed as follow :

$$V_{AM} = F_{11.} F_{12} . U_{C1} - F_{13}. F_{14}. U_{c2}$$
$$V_{BM} = F_{21.} F_{22} . U_{C1} - F_{23}. F_{24}. U_{c2} \qquad (3)$$
$$V_{CM} = F_{31.} F_{32} . U_{C1} - F_{33}. F_{34}. U_{c2}$$

However, the output phase voltages of the inverter can be deduced from equation (3) as follows:

$$V_A = (2V_{AM} - V_{BM} - V_{CM}) / 3$$
$$V_B = (2V_{BM} - V_{CM} - V_{AM}) / 3 \qquad (4)$$
$$V_C = (2V_{CM} - V_{AM} - V_{BM}) / 3$$

And these equations can be rewritten using the voltage branches which give :

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{Bmatrix} F_{11}F_{12} \\ F_{21}F_{22} \\ F_{31}F_{32} \end{Bmatrix} U_{CI} - \begin{bmatrix} F_{13}F_{14} \\ F_{23}F_{24} \\ F_{33}F_{34} \end{bmatrix} U_{C2} \quad (5)$$

III. PWM STRATEGY AND SIMULATION RESULTS

The parameters of PWM control technique are defined as: Amplitude modulation index m_a and the frequency ratio m_f.

$$m_a = A_m / A_c \qquad (6)$$
$$m_f = f_c / f_m \qquad (7)$$

Where A_m is the peak amplitude of the control signal, while A_c is the peak amplitude of triangle signal (carrier).

m_f is the ratio between the carrier and the control frequency.

The PWM three level inverter algorithm of one carrier is given by :

$$\begin{aligned} &\left(\left|V_{ref.1}\right| \le U_p\right) \Rightarrow B_{11} = 1, B_{12} = 0 \\ &\left(\left|V_{ref.1}\right| > U_p\right) \text{et } V_{ref.1} \langle\, 0 \Rightarrow B_{11} = B_{12} = 0 \\ &\left(\left|V_{ref.1}\right| > U_p\right) \text{et } V_{ref.1} \rangle\, 0 \Rightarrow B_{11} = B_{12} = 1 \end{aligned} \qquad (8)$$

Where: V_{ref} is called modulating signal and U_p is the carrier signal

Table II: shows the truth table of the algorithm [5].

A	B		B11	B12
0	0		1	0
0	1		0	0
1	1		1	1
1	0		1	0

Where:

$$A = 1 \text{ when } V_{ref} \rangle 0 \qquad \text{if not } A = 0$$
$$B = 1 \text{ when } \left|V_{ref}\right| > U_p \qquad \text{if not } B = 0$$

The logical expressions of B_{11} and B_{12} are:

$$B_{11} = \overline{B}_{14} = \overline{B} + A$$
$$B_{12} = \overline{B}_{13} = AB \qquad (9)$$

The synoptic diagram of the proposed simulation of the strategy is shown in fig.3 [6], [7].

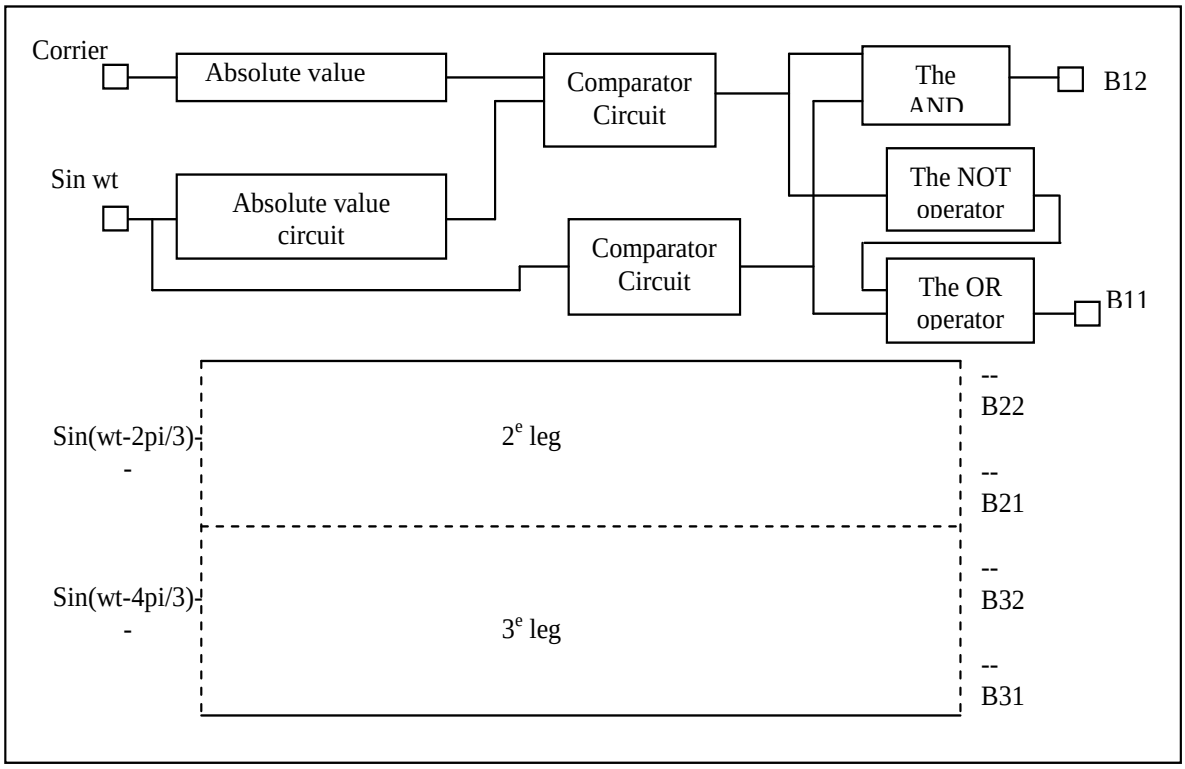

Fig.3 Synoptic of the proposed PWM strategy

To illustrate the performance of the three-level PWM inverter, the system is investigated through computer simulation using a passive load.

By taking the following parameters:

R= 22 Ω, L=340mH, m_f=24, m_a=0.8. Uc/2= 30V, f =50Hz.

And after running the simulation program under *Matlab simulink* environment the following results are obtained. They are presented in figs.4,5, 6, 7, and 8.

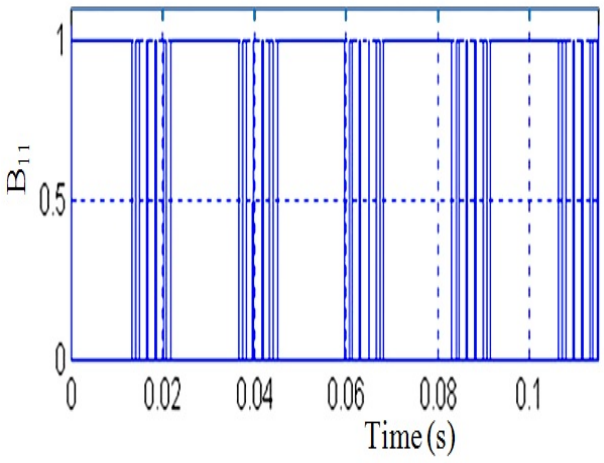

Fig.4 Control pulses for m_f=24 m_a=0.8

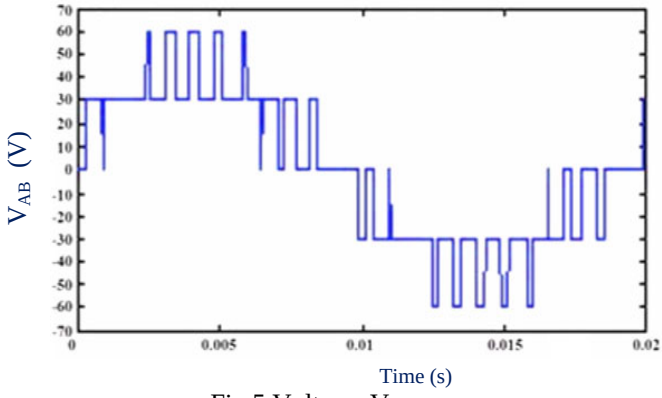

Fig.5 Voltage V_{AB}

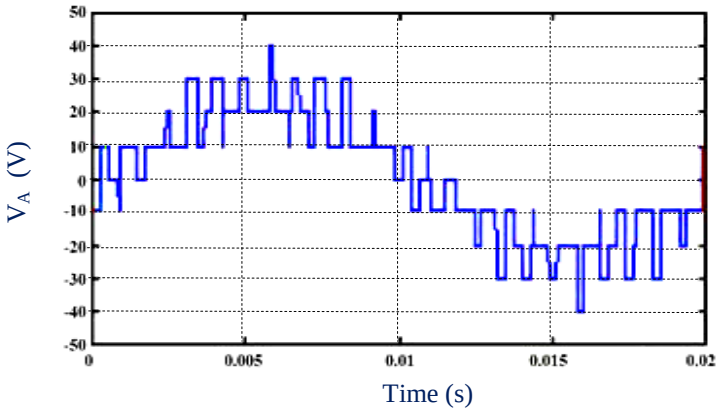

Fig.6 Output voltage of phase V_A

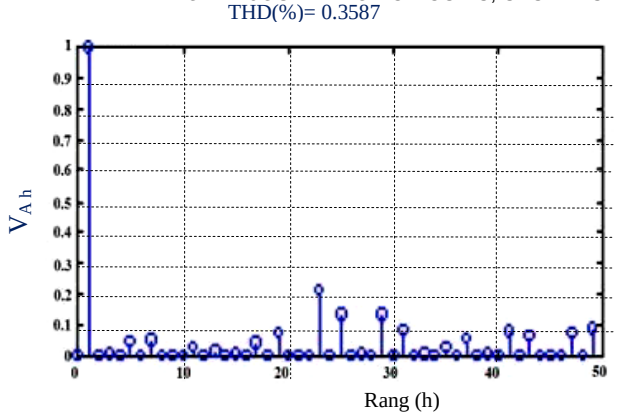

Fig.7 V_A harmonic spectrum and THD

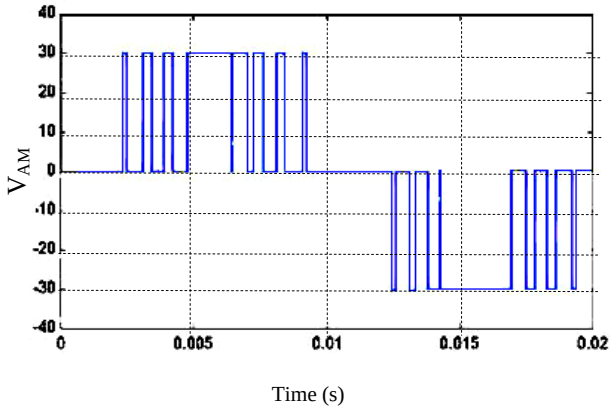

Fig.8 Voltage V_{AM}

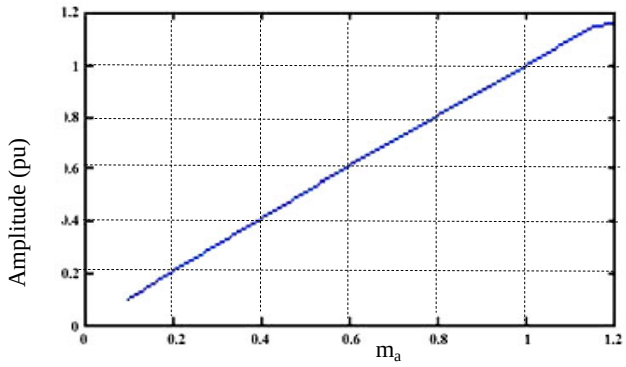

Fig.9 Evolution of the fundamental voltage V_A.

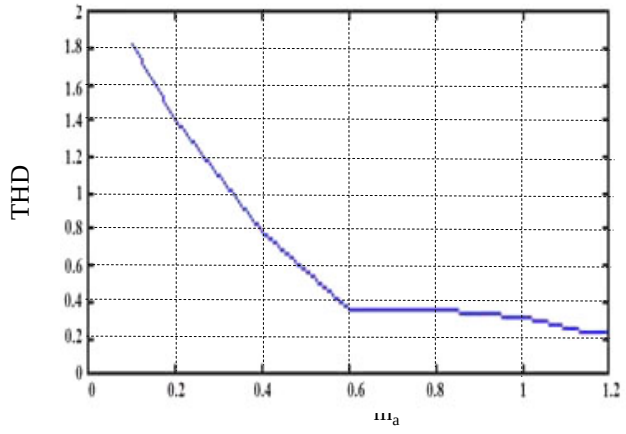

Fig.10 THD of voltage V_A

Fig.4 shows the simulation sequences of the upper-arm.
Fig.5 shows the line voltage Vab, it has five voltage levels Uc, Uc / 2, 0, - Uc / 2, Uc.
Fig.6 shows the output voltage of the first phase of the inverter.
Fig.7 shows the spectral analysis of the phase voltage. The voltage spectrum shows that the harmonics are grouped into multiple frequencies centered around the switching frequency families. Harmonic number 23 and 25 are the most important harmonics present in the voltage waveform.
Fig.8 shows the voltage V_{AM} with the three levels of output voltage of an arm: Uc/2, 0 , -Uc/2.
Fig.9 shows the evolution of the amplitude of the fundamental output voltage V_A versus the modulation index m_a.
Fig.10 shows the THD versus m_a. We note that the harmonics decrease as m_a increases.

These results are much better than those which could be obtained with a conventional two–level inverter as the harmonics content is pushed to their higher order and thus easily filtered. It should be that the comparison of the reference sinusoidal signal with the triangular waveform is done in the PWM generator of the DSP to generate the control signals for the switching devices along with the inverted signals with the required dead band.

IV. Experimental Investigation

The schematic diagram of the converter circuit implemented is given in fig.11. It consists of two parts: the power circuit, and the control circuit.
The power circuit is formed by two arms, formed by twelve transistors I.G.B.Ts and eighteen diodes connected in anti-parallel. The generated control signals are obtained using several control cards such as conditioning, monitoring, D/A conversion cards etc.
The shaded part is the control circuit containing the DSP controller TMS320LF2407 that generates the PWM signals and also provides soft start functions [8]. The DSP programming is based a software developed by Texas Instruments (Code Composer). The control algorithm is written in assembly language in order to optimize the whole tasks cooperation and to ensure communication between the DSP, the converter, anod the passive load [10] [11] [12] [13].
Fig.13 shows a photograph of the experimental bench including the inverter and all the peripheries.

It should be noted that the parameters used in the experimental investigation are similar to those used earlier in the simulation in order to validate the developed models. Furthermore, for the same triangular-sinusoidal strategy, a frequency ratio equals to 0.8 and an index of modulation equals to 24 is taken.

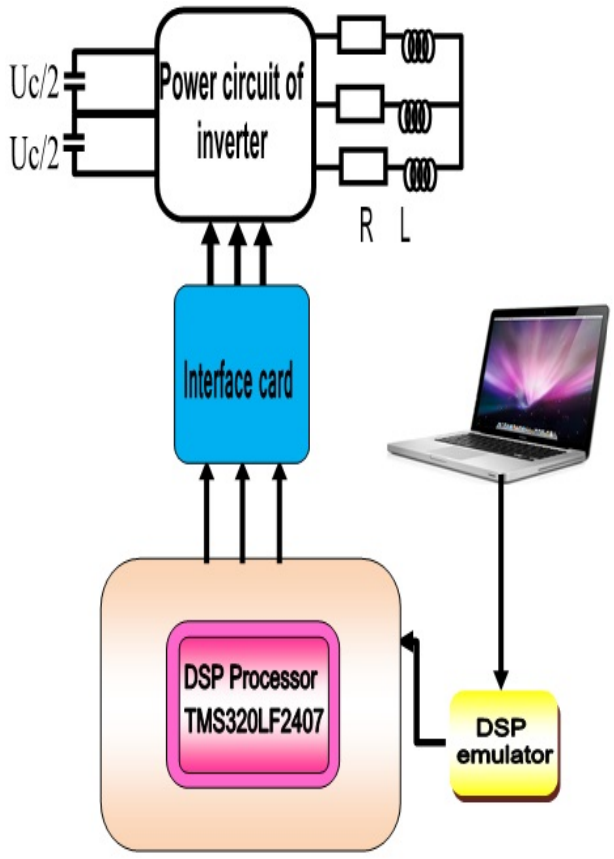

Fig.11.a DSP TMS320LF2407 implementation diagram

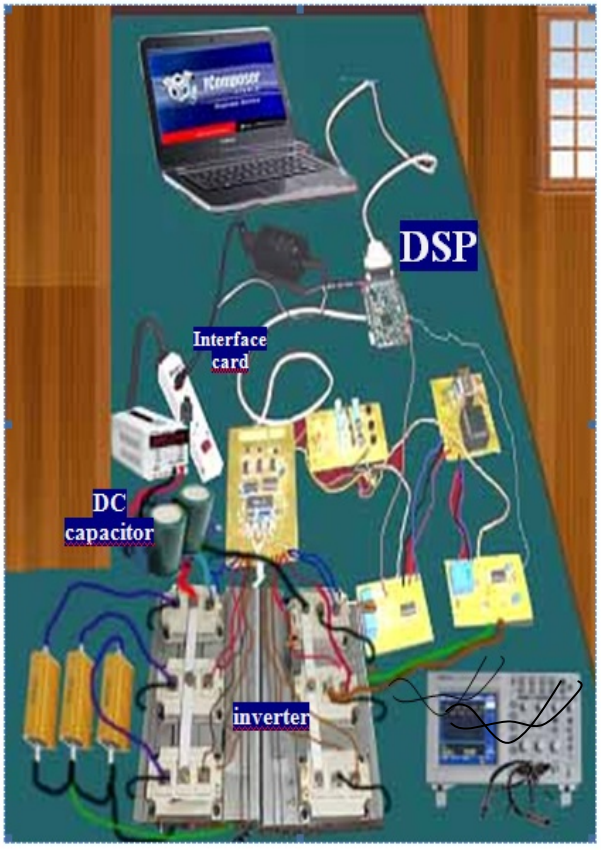

Fig.11.b Experimental bench

After the construction of the various electronic circuits and the development of the software, the three-level converter was tested in the laboratory. It was used as an inverter supplying a passive load formed by a resistance and an inductance. The oscillographic results obtained are given in Figs.12, 13, 14, and 15.

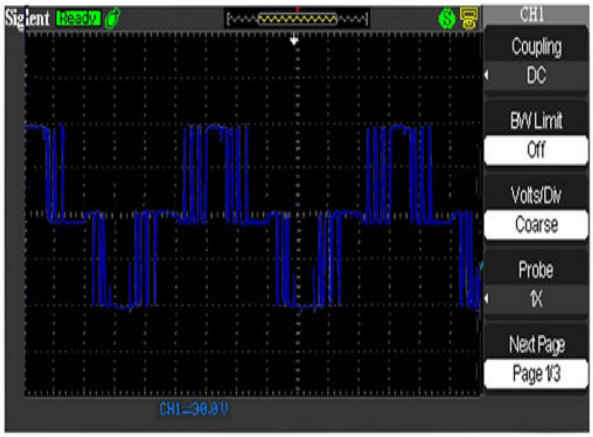

Fig.12 V_{AM} voltage (15V/Div)

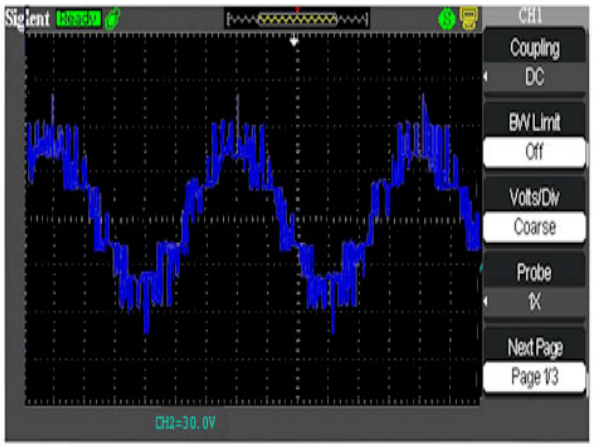

Fig.13 Output voltage of phase VA(15V/Div)

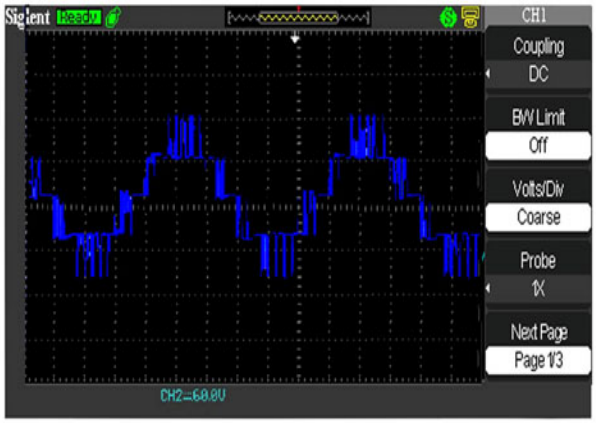

Fig.14 Voltage V_{AB} (30V/Div)

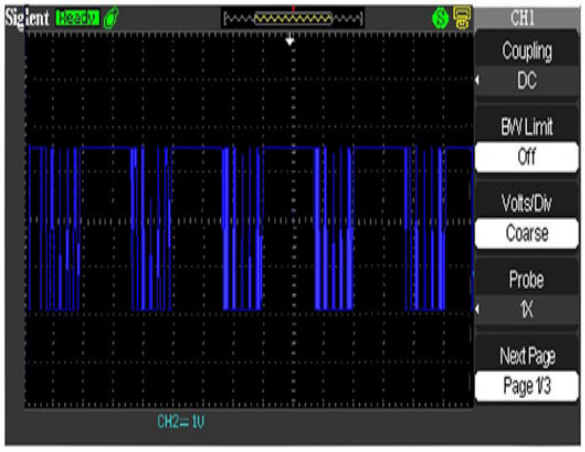

Fig.15 Control pulses (1v/Div)

Fig.12 clearly shows the V_{AM} voltage variation. The waveform of the voltage is similar to that obtained from the simulation, except the small shift observed around the zero level of the voltage. This is may be due to the imbalance of the midpoint.

Fig.13, 14, and 15 show respectively the voltage of the first phase V_A the line voltage and the control pulses obtained experimentally. All the parameters are almost similar to those obtained in the simulation.

V. Conclusion

Simulation and experimental results show that the developed test rig (the hardware and the software) works properly. The low commutation frequency of three-level inverters permits a realisation of an optimal control by relatively simple tools. With a high number of semiconductors devices, current quality can also be improved and weight reduced by avoiding heavy current filters. Moreover, the output harmonic contents of the phase voltage are fewer than those obtained in conventional two-level inverters at the same switching frequency.

The control voltage was controlled by a microcomputer in a much more sophisticated manner than those using analogue circuits. This opens ways to many other investigations. In fact, work is being undertaken to use this system to feed an asynchronous machine and will be published in the near future.

References

[1] A.Nebae, *''A new Neutral-Point Clamped PWM Inverter''*, IEEE Transactions on Industry Applications, Vol.IA-17, N°.5, Sept/Oct 1981, pp 518-523.

[2] R.Bows, S.Grewal and D.Holliday, High frequency PWM technique for two and tree single - Phases inverter s, *IEE, proc. Electro. Power apllication*, May 2000.

[3] Yo- Han Lee, Bum-Seok and Dong-Seo Hyun , A Novel PWM Scheme for three-Level Source Inverter With GTO Thyristors, *IEEE Transactions on Industriel Electronics, Vol.32, N°2, Mars/April*, 1996.

[4] P. Rioual , H. Pouliquen , and J.P.Louis, Regulation of a PWM Rectifer in the Unbalanced Networrk state using Generalized model , *IEEE Transactions On Power Electroniocs, Vol. 11, No 3*, pp. 495-499, 1996 .

[5] E. M. Berkouk, Contribution à la conduite des machines asynchrones monophasées et triphasées alimentées par des convertisseurs directs et indirects. Application aux gradateurs et onduleurs multiniveaux. *Thèse de doctorat, C.N.A.M*, Paris 1996.

[6] M. Gaad, E. M. Berkouk, K. Aliouane, Contribution à la réalisation de la commande d'un bras d'onduleur à trois niveaux, *2ème conf, intern sur l'électrotechnique*, Oran 2000.

[7] H. Denoun, contribution à l'étude des convertisseurs AC/DC à MLI à facteur de puissance unitaire, application à la conduite de la machine asynchrone. *Thèse de Magistère, E.M.P* 2001, Alger.

[8] F. Bouchafaa, E.M.Berkouk and M.S.Boucherit, Analysis and simulation for nine-Level voltage source inverters application to the speed control of the PMSM, *Elmectromotion, Vol.10 N°3* July - September 2003 pp.246-251.

[9] H. Denoun, N.Benamrouche, S. haddad, S. Meziani and S. Ait Mamar, *''A DSP (TMS320lf2407) Based Implementation of PWM for Single-phase AC-DC Bipolar Converter with a Unity Power Factor''*,WSEAS International Journal of Circuits, Systems and Signal Processing, Vol 5, 2011, pp 354-361 ISSN-1998-4464

[10] H. Denoun, N.Benamrouche, S. haddad, S. Meziani and S. Ait Mamar**,***''A DSP (TMS320lf2407) Based Implementation of PWM for Single-phase AC-DC Bipolar Converter with a Unity Power Factor''*, WSEAS Procceding of the 10th International Conference on signal Processing, Cobridge, UK February 20-22, 2011, pp-289-295,ISSN 1792-8192.

[11] C. Panoiu, Baciu, M.Panoiu, and C.Cuntan, ''Simulation results on the currents harmonics mitigation on the railway station line feed using a data acquisition system'' WSEAS Trans. On Electronics, Vol.4, No.11, pp.228-236, 2007.

[12] H.Tatizawa, E. S. Netsuo, ''Calibration of high voltage transducers for power quality measurements,'' WSEAS Trans. On systems, Vol.8, No, 3, pp.400-409. 2009.

[13] I.Ghadbane,M. T. Benchouia, ''Feed back linearised control based three Phase shunt active power filter,'' WSEAS Trans. On systems, Vol.7, issue 1, pp.18-25. 2013.

H. Denoun was born in Algiers, Algeria. He received his Bsc degree in electrical engineering from the Mouloud Mammeri University, Tizi-Ouzou, Algeria, and the D.E.A degree from Paris 6, France and the Magister degree from Polytechnic School, Algiers, Algeria in 1998 and 2001 respectively. He got his PhD degree in Electrical Engineering from The University of Mouloud Mammeri University, Tizi-Ouzou .

He is currently a senior lecturer at the same university. His research interests include electrical machines and drives, power electronics and control systems.

.