Low-cost Access System Application Based on Educational Microprocessor Development Kit

Tomas Sysala, Petr Neumann, Filip Zanka, and Lubomir Vasek

***Abstract*—**Article is reporting on a cheap access system option implemented within an educational microprocessor development kit environment. That development kit serves generally for programming skills training aimed at microprocessor and PLC application for real processes control in our faculty curriculum. The basic system takes advantage of Atmel microprocessor. The user identification is accomplished with iButtons by Maxim Integrated. That iButton represents a computer chip encapsulated in a steel case.

***Keywords*—**Microprocessor development kit, Education, Access system, Microprocessor programming.

I. Introduction

Microcomputers and microcontrollers constitute a common ingredient in our daily life. We are meeting them without noticing it.

Microcomputers as a cheap and small form of digital devices (computers) lived through their rapid development in early 80-ties of the last century. Those microcomputers were first in 8-bit version and later in 16-bit version then. The model Intel8080 [1] and/or Zilog Z80 [2] may be mentioned as the most popular models at that time.

Microcomputers in 32-bit version with the ARM core gained popularity in more challenging application during 90ties of the last century [3].

One of our former projects was aimed at the 32-bit version of a development kit with a color display and many options oriented in the multimedia application field [4].

The low cost attribute of this project prefers the 8-bit processor.

II. Goal and Specifications

Many subjects taught at Tomas Bata University, Faculty of Applied Informatics, are oriented at technological processes control. The microcomputer presents one of alternatives for such processes control.

The goal of one our project was to design a development kit based on a 8-bit microcontroller with the AVR core which should comply with following requirements:

- Low costs,
- Extended peripheral equipment for interfacing technological processes,
- Extended peripheral equipment for various communication modes,
- Dual line text display unit (2 x 16 characters),
- Peripheral modularity for a flexible expansion and/or modification according to the particular purpose.

On the first phase is whole system based on modular system MLAB. [16]

III. Microprocessor Development Kit

A. Microprocessor

Processor is a core of each development kit. In our case, we have opted for 8-bit processor from Atmel product range, namely the Atmel® AVR® ATmega128.

This processor is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega128 achieves throughputs approaching 1MIPS per MHz allowing system design engineer to optimize power consumption versus processing speed.

The Atmel® AVR® core combines a rich instruction set and 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers [5].

The ATmega128 provides the following features: 128Kbytes of In-System Programmable Flash with Read-While-Write capabilities,

- 4Kbytes EEPROM,
- 4Kbytes SRAM,
- 53 general purpose I/O lines,
- 32 general purpose working registers,
- Real Time Counter (RTC), four flexible Timer/Counters with compare modes and PWM,

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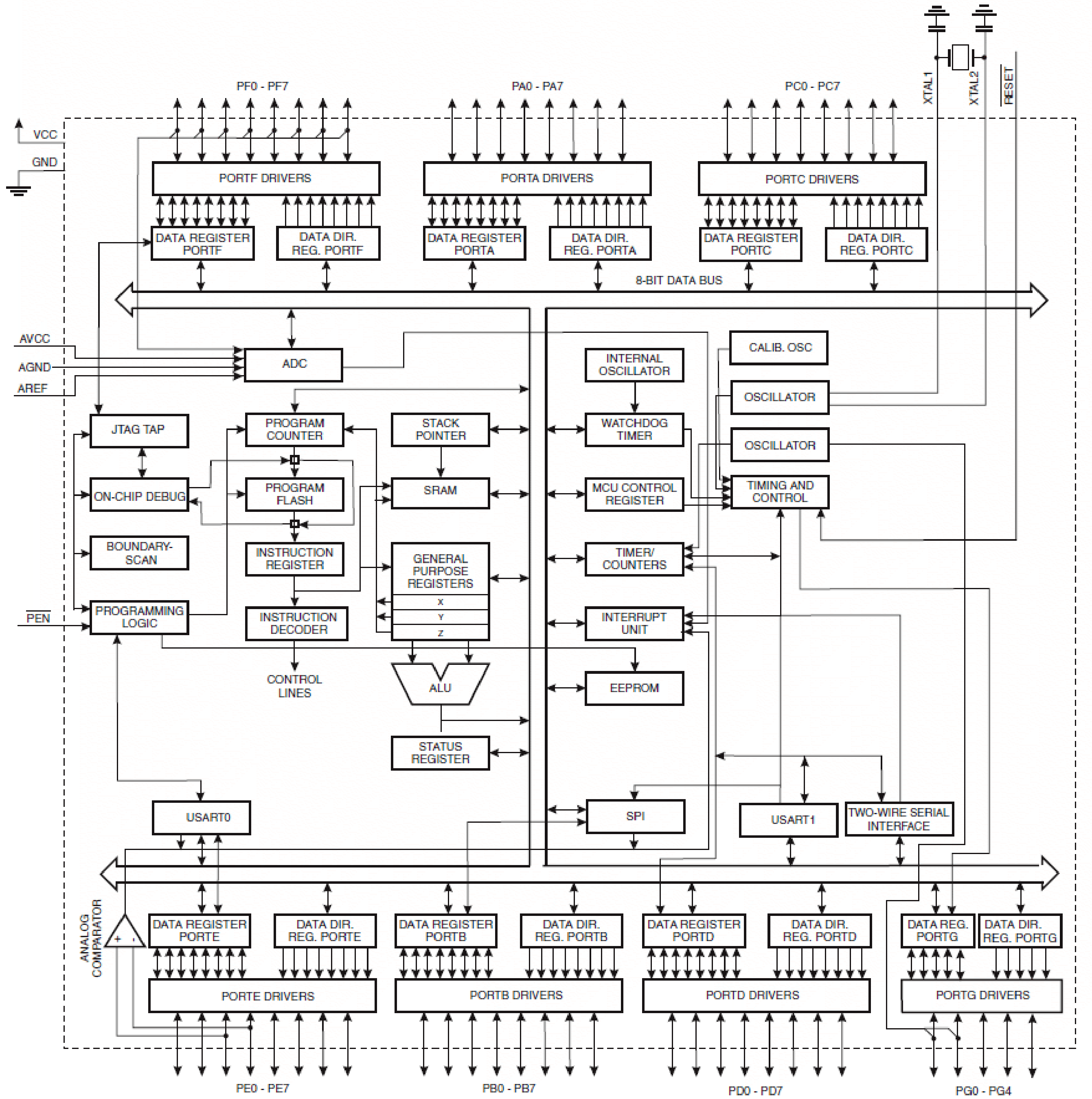


Fig. 1 Block Diagram of the AVR Architecture [5]

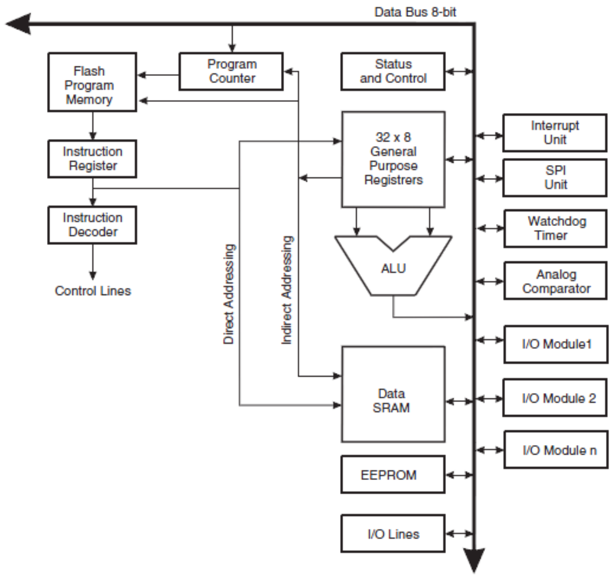
- 2 USARTs, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain,
- programmable Watchdog Timer with Internal Oscillator,
- an SPI serial port, IEEE std. 1149.1 compliant

The device is manufactured using Atmel's high-density nonvolatile memory technology. The Onchip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega128 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications [5].

The ATmega128 device is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

A. AVR CPU Core

The ATmega128 has AVR® core architecture. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals and handle interrupts.



7Fig. 2 Block Diagram of the AVR Architecture [5]

In order to maximize performance and parallelism, the AVR uses Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

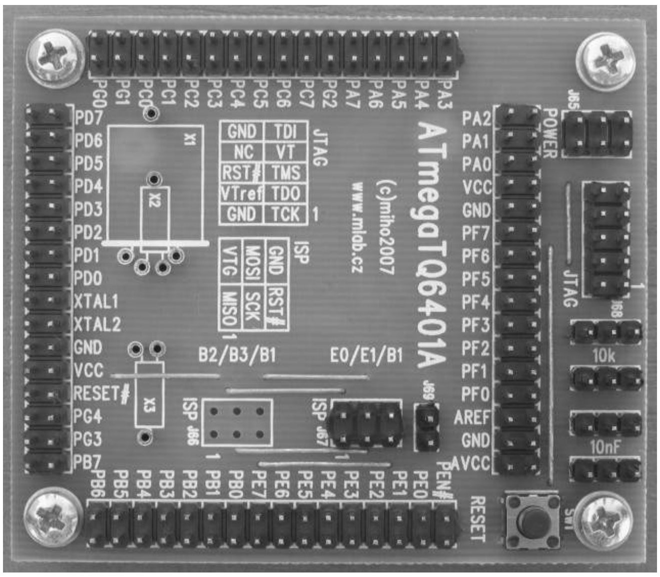


Fig. 3 ATmega128 MCU module [16]

The fast-access Register file contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register file, the operation is executed, and the result is stored back in the Register file – in one clock cycle [5].

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

B. LCD Display

For the sake of device compactness, low price, and availability, the LCD2L4P02A [6] module has been selected as a device management unit and as an input interface for simple user data entering. That module is equipped with a dual line text LCD display (2 x 16 characters), and it is controlled by the Hitachi HD44780 controller. The user interface consists of four buttons and of a piezoelectric element for pertinent sound signalization what is well sufficient for basic operation.

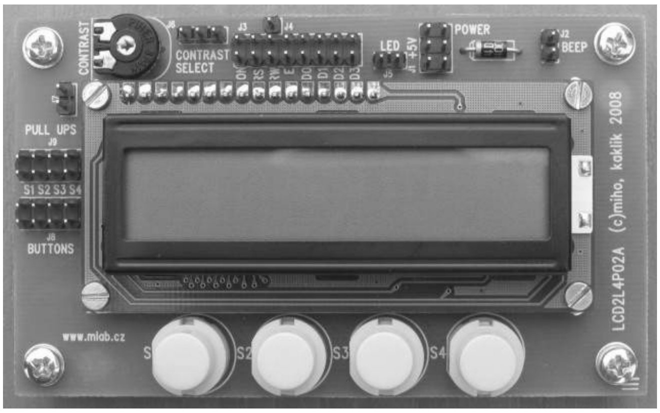


Fig. 4 LCD module with control buttons [17]

C. Real Time Clock Module

The RTC module for actual datum and time retention is not a part of that microcontroller. It was necessary to design and realize it. The integrated circuit DS1307 by Maxim Integrated Products seemed to be a convenient basic element for the RTC module. The circuit design has respected the application circuitry recommended in the data sheet [7]. The RTC beat is controlled by an external crystal with the resonance frequency of 32.768 kHz. When the power supply is off, the time and data memory content is secured with a battery. In such back up mode, the current consumption is only 500 nA what means that the time and memory content can be kept for more than 10 years (the battery capacity 48 mAh at the room temperature +25 ºC).

The ease availability of datum and time represents a remarkable advantage of that circuit family. They are coded in the BCD, and it is possible to read the from internal shift registers.

There is possible to arrange an output rectangular signal of various frequencies (1 Hz, 4.096 kHz, 8.192 kHz a 32.768 kHz) using control register. That is why the module is equipped with transistor and jumpers for occasional use in other projects.

Table 1. RTC module Internal registry details

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	CH	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12 24	10 Hour PM/AM	Hours	Hours				Hours	1-12 +AM/PM 00-23
03H	0	0	0	0	0	DAY			Day	01-07
04H	0	0	10 Date		Date				Date	01-31
05H	0	0	0	10 Month	Month				Month	01-12
06H	10 Year				Year				Year	00-99
07H	OUT	0	0	SQWE	0	0	RS1	RS0	Control	-
08H-3FH									RAM 56 x 8	00H-FFH

The CR 2032 button battery (see Fig. 5) ensures the clock and calendar functionality backup.

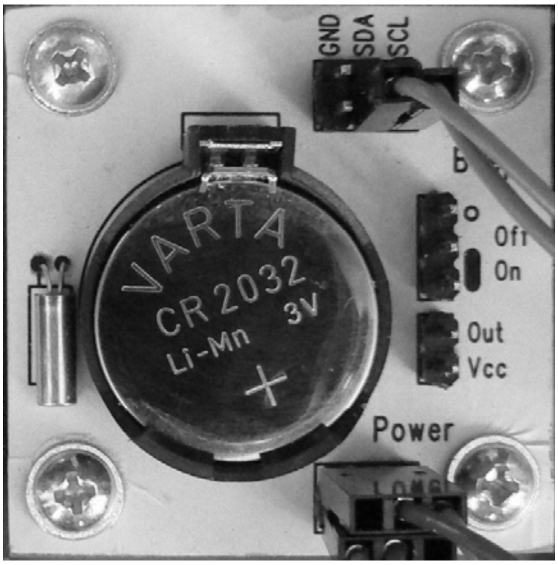


Fig. 5 RTC module [16]

D. Access Transactions Storing – Memory Card

SDcard01B serves as a memory card. There is basically a prepared socket for SD/MMC insertion. Inputs are protected against over voltage with resistors in series. Considering the cards operational voltage of 3.3 V, and the module integral supply voltage stabilizing, there is necessary to insert a voltage level converter between the microcontroller and the card as described in the following chapter.

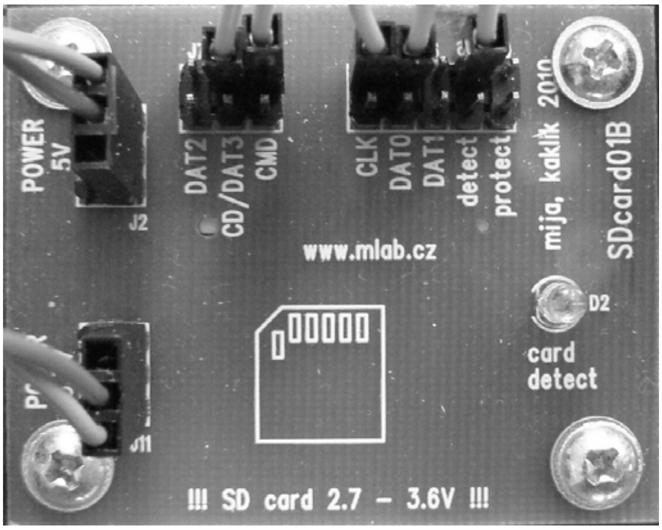


Fig. 6 Memory card module [16]

E. Voltage Level Converter

The voltage converter 5/3.3 volts is based on the TXB0108 integrated circuit by Texas Instruments [17]. It is an eight bit bidirectional voltage converter with automatic data flow direction recognition and ESD protection.

There exists also a four bit converter variant. Nevertheless, the eight bit converter is more versatile, and it can be used also for another projects. That circuit is composed of two interfaces each of them representing one voltage level. Port A can be operated in the range between 1.2 volts and 3.6 volts (the memory card is connected to this port). Port B can be operated in the range from 1.65 volts to 5.5 volts (the microcontroller is connected to this port).

The circuit design corresponds with the data sheet recommended application circuit. The converter is connected to the microcontroller via pins PB0 to PB3 (card is operated in the SPI mode). Card detection uses pins PE6 and PE7. Card side connection occupies pins CMD (MOSI), CLK, DAT0 (MISO) a DAT3.

F. Power Switch

The output actuator is represented with a common electromagnetic lock (electromagnetic doorkeeper) which needs 12 volts DC or AC for operation. The peak current is up to 2 amps so that taking into account the microcontroller low power output, there was necessary to design a corresponding power switch.

The MLAB kit [16] incorporates such switches in a module form with 2 up 4 transistors. That is more than necessary for our project because we need just a half of the NFET2X01A module. Our new module is set with one N-FET transistor, with a protection resistor R1, and with a high resistance resistor R2 ensuring the transistor OFF-sate in and inactive state. That module is set also with a protection diode D1 which limits the collector voltage during an inductive load switching off process when the reactive voltage increases and could damage the switching transistor.

G. Power Supply Voltage

The power supply voltage for individual modules should deliver DC voltages of 3.3 volts, 5 volts and 12 volts. That supplying branch for 12 volts can be delivered directly from a suitable source which does not need to be stabilized because an electromagnetic lock is not demanding for supply voltage stability.

There is necessary to have 5 volts stabilized for modules majority and 3.3 volts for the memory card. Providing 5 volts source is available, it is possible to get 3.3 volts directly in the memory card module because it is fitted with a relevant stabilizer.

MLAB [16] includes several modules of that kind one of them is LM108601A with output voltage adjustable from 1.25 volts to 5.5 volts.

H. Other Development Kit Parts

That designed device set includes some other modules, namely:

- The power switch for external devices control
- The USART/USB conversion module.

The whole device set is of a modular design. That corresponds with the low cost requirement because only relevant modules for a particular application are connected and installed.

IV. Low-Cost Access System

A security oriented composition was created for the developed kit functionality and applicability evaluation. That composition represented an autonomous system for access security control. That security control application is oriented at family houses and apartment houses where it attends one entrance point (the electromagnetic gate). There is up to 20 such entrance points with a prospect for future increasing. It is supposed that each device has a different approved set of identification elements (tokens), and that it operates independently. The memory stored identification elements counts in tens at maximum.

A. The System Requirements

The above mentioned security application identification elements selection asks for a mechanically robust, cheap and passive design. From the security point of view, such ID elements counterfeiting should be much more complicated than key imitating, and the ID elements misinterpretation should be also quite unlikely during authorization process.

The access history evaluation, in case of a theft in commonly shared rooms, for instance, should be possible with current design because it could retrospectively specify the access ID and access time. The device control should be simple, preferably without necessity to connect any other devices, like programmers, computers, etc. However, that device is supposed to be placed near the entrance point so that the authorization interface should be protected correspondingly. Further requirement relates to the device operability in case of energy supply drop-out.

The device power supply is either the public electricity distribution network, or alternatively the building local electricity distribution and/or battery back-up power supply, for instance.

If we summarize the above mentioned requirements, the developed device should fulfill the following features:

- Exploitation of microcontroller technology.
- User friendly design.
- Lost ID element quick and simple removal and new ID element registration.
- ID elements selection with regard to counterfeiting prevention.
- Storing data about authorized and unauthorized accesses.
- Unauthorized access to the control interface protection.
- Emergency access alternative without identification, for instance protected emergency button, or a remote electronic gate keeper.
- Price is comparable to the common door lock replacement in case of a lost key.

B. System Block Diagram

The system block diagram has been created for particular device component interconnection design:

- Microcontroller
- Programmer
- USART/USB converter
- Control interface – LCD display
- Real time clock (RTC)
- Access transactions storing – SD card
- Voltage Level Converter
- iButton reader
- Access point interface – power switch
- Power supply

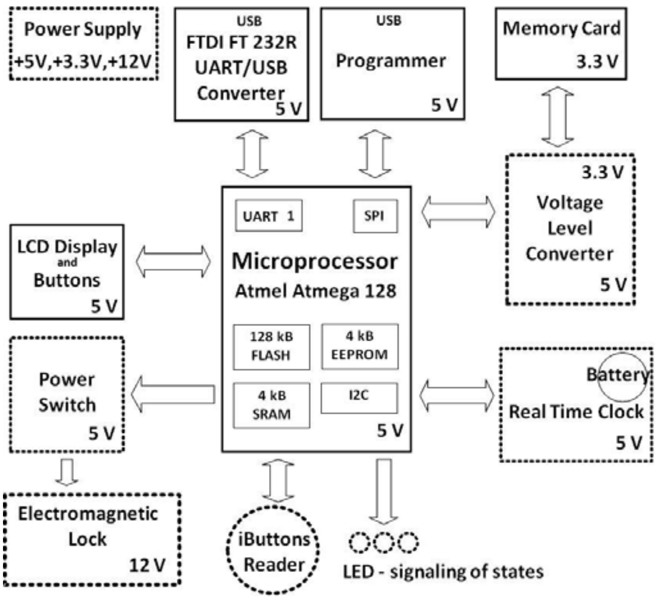


Fig. 7 Block Diagram of the Access System

C. Identification Element

The iButton contact elements have been selected because of their interesting price to utility value ratio [8]. The only disadvantage of those elements is the absence of direct communication with microcontroller possibility. Those elements exploit the “1-Wire Bus” which is to be emulated by software.

Fig. 8 ID element iButton [9]

Maxim Integrated Products produces a wide assortment of identification elements (tokens) under iButton family name. The scope of application covers various access control system, attendance systems, etc. Such element consists of a microcontroller chip encapsulated in a stainless steel package with the diameter of 16 mm. The iButton elements make use of their metal packages as an electrical contact interface to 1-Wire bus and for power supply. Each element is identified with a unique 64 bit identification code which is laser engraved in the package surface.

The particular token identification safety provides the CRC check sum with X8+X5+X4+1 polynomial. The authorization reading is valid if the first 56 bits check sum is coincident with the value stored in the byte seventh.

The iButton elements [8] are produced in about twenty variants, and besides the ID number they can hold further functions. The ID element basic version iButton DS1990A holding ID code only has been selected for our project.

D. 1-Wire Communication Interface

1-Wire is a bus designed by former Dallas Semiconductor acquired by Maxim Integrated Products in 2001 [8, 18]. It is a serial bus possessing the ability of interconnecting one Master and several Slaves controlled by the Master via only one data transmission wire and a common ground.

The bus communication is bidirectional and asynchronous in a half duplex mode. The bus operates at data rate of 15.4 kbps or 125 kbps respectively (Overdrive mode). Although that bus is originally designed for close devices connection, the overall length depends on topology nowadays, for instance, the Master/Slave distance can be 750 meters.

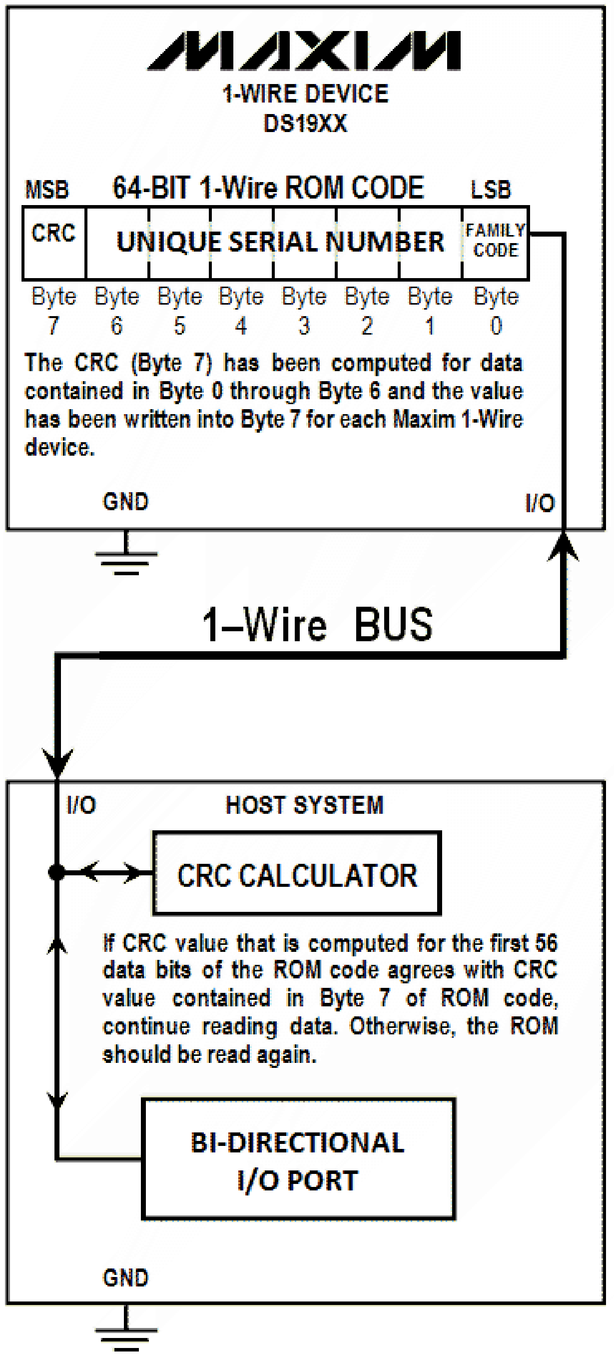


Fig. 9 The iButton checksum read up [18]

The most commonly applications are using distances of about few meters. Sensors can be fed directly via bus (Parasite-Power) what is optimal for 1-Wire bus security applications. Unfortunately, the 1-Wire bus is not implemented in ATmega microcontrollers. Nevertheless, it can be relatively easily emulated with software for it requires only four basic operations: Entry 1, Entry 0, Read and Reset. On the other hand, timing is a key operation for software emulation. 1-Wire defines time slots for one wire channel communication. The data wire is connected to supply voltage via a resistor, and this arrangement determines the high logic state. The ground voltage level determines the low logic state. The more detailed communication explanation is a little bit more difficult and it can be accessed at the producer´s website [18].

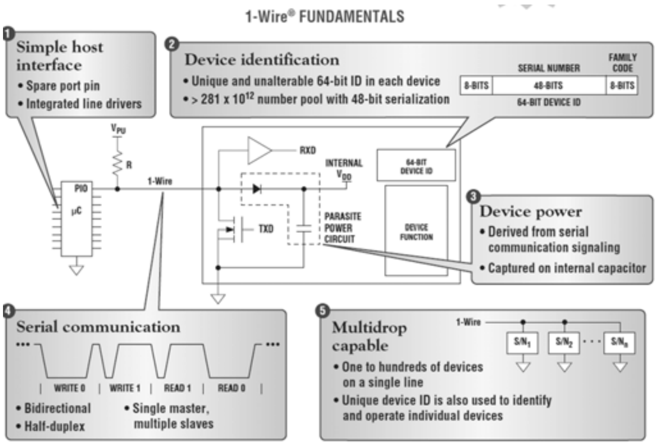


Fig. 10 1-Wire Bus basic circuit [19]

E. Access Point Interface

The access point interface is comprised of an iButton sensing module and of an electromagnetic lock (door open system). With regard to 1-Wire bus software emulation, the sensing module does not need to be equipped with data processing logic. It could be just an electromechanical contact. An arbitrary electromagnetic lock system with direct current power supply of 12 V is convenient for the access point unlocking. It is not important whether there will be used a lock system with memory (activated by an impulse and deactivated mechanically after door is open), or if there will be used a standard lock system (deactivated with the electromagnet supply termination).

F. Other Part of System

Although there is possible to use a standard two wire serial communication interface for the device management like many other systems do, we have decided differently in this case. There is necessary to connect a PC in standard situations mentioned above. Such manipulation is not always user friendly. In our case, we are using the serial interface only for special and rare diagnostic purposes. Any regular device management in our case is realized LCD display with a few buttons.

The process of storing transactions data (entrance permission or entrance denial) is realized as a data storing in a text file on a SD/MMC memory card.

V. Secure User Identification

Any system user identifies himself with his iButton. The system reads his number and compares it with authorized tokens in its memory. Providing the number is correct, system release the lock. A potential intruder has a few possibilities how to gain access. If he has no genuine token, he has to possess a device being able to simulate an authorized token. Such device would be possible to create even though it is not an easy process. Nevertheless, such device application does not mean automatically an access gain. It has to know either the correct token number or all possible token combinations, or to try generation of all possible combinations. Such approach is called a rough force attack in information security terminology.

A. User Token Authentication

The 64-bit ID number entry process was described in chapter IV/C. The ID transfer and entry is successful in case the first 56 bit entry checksum corresponds with the last entry byte. It means that an intruder cannot rely on successful access either via unregistered token or providing MCU transfer fault occurs or in case 1-Wire bus is artificially jammed. Any intruder has to know either any particular IButton ID or has to guess it right.

B. Protection against Rough Force Attack

Would it be that an intruder tries to trace the ID number combination by testing it individually. His success probability depends on one attempt processing time. There has been evaluated with a simple counter that an item ID processing is performed a few hundred times per second. That is advantageous for a legitimate user because he can touch the reader for an arbitrarily short time, and he is let into. From the security point of view, it is not an acceptable situation because of quick successive entry attempts possibility. It is so desirable to halt ID processing for certain time in case of ID discrepancy. To keep the system user friendly, there is a 1 second halt set for case of incorrect ID. We can estimate time to intrusion under such conditions set.

iButton exploits the 64-bit ID number with last byte used as CRC [8]. It means that we have 56 bits for individual combinations representation. It offers 2^{56} variants (more than $7x10^{16}$). If an intruder is lucky and hits the right combination in the centre of investigated time span and his speed is 1 combination per second, he would get the access in 1 142 462 658 years. To make it a little bit more complicated for him and to be able to read LCD message, we can set the process halt time after identification failure up to 5 seconds.

C. Other Selected Functions

From security reasons, there is an urgent need to arrange passage for authorized persons even in case of energy drop-out. That can be ensured either with a centralized sector and its energy backup or with a local USP and/or a backup battery.

Administrator has to keep an updated register of issued token ID codes with regard to lost token cases and token blockage process. An urgent blockage minimizes the risk of token misusing, however, the ID code records are to be protected against theft or copying because an emulator can be created with the knowledge of them.

Same strict measures apply to control interface administration access PIN. Provided the administrator forgets that PIN, it is possible to reset it by RTC battery removal after the device cabinet opening.

In case of a security incident, there is possible to analyze that data stored on a memory card and gain an overview about individual entering a protected area. The memory card can be removed even during a device operation. That device continues in operation mode and serves users. It is of course unable to record transaction data. Such memory-less state is indicated by a quickly flashing blue LED [15].

The device can be switched off with a button at any time. No action is necessary to perform before switching off.

VI. Conclusion

The project main goal was to design and create a kit for the verification of microcomputer programming student education possibilities.

That designed device was verified for a security application, namely for an autonomous entrance guard system. The result corresponds with task assignment, and it fulfills the economic goal as well. Our design is cheaper and carries more functionality than commercial ones. The task solution composes from two parts, the hardware part and the software part. The software part has been created in the AVR Studio 4 development environment in C language.

The hardware part is realized as a complete set including electromagnetic lock system and iButton reader.

An economic analysis proved that our device set can be manufactured with half of the costs of those existing commercial products, and its functionality can be even better. In comparison with a standard security lock, our device set is more expensive, but it is true only until the first key loss.

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