CITIROC High-Level Analog Front-End Model Implementation and Simulations

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***Abstract*—This work reports the high-level implementation and PSPICE simulation results of the CITIROC fully-analogue front-end model, to investigate its main characteristics and demonstrate its practical effectiveness when driving the active silicon photomultiplier (SiPM) detector signals. The circuit models of all functional blocks of the circuit are first described. Frequency and dynamic features of all electronic front-end sections are addressed, and the relevant key design mathematical equations are derived as well. Subsequently, PSPICE simulations of each single block are carried out to analyze and confirm its own analogue behavior. Finally, the transient responses for the global circuit front-end are simulated under a SiPM pulse-wise single-channel input.**

***Index Terms*—Analogue circuits; front-end model; SPICE simulations; silicon photomultipliers.**

I. Introduction

CITIROC (Cherenkov Imaging Telescope Integrated Read-Out Chip) is a new Application-Specific Integrated Circuit (ASIC) produced by OMEGA and designated as front-end of the camera at the focal plane of the ASTRI telescope. ASTRI is a flagship project of the Italian Ministry of Education, University and Research, aimed to build a prototype for the small-size telescopes of the Cherenkov Telescope Array (CTA) [1].

ASTRI will adopt innovative technological solutions in terms of mirror structure, focal plane sensors and read-out electronics. For the first time in CTA designs, the ASTRI prototype will be characterized by a dual-mirror, Schwarzschild-Couder optical system arranged in a compact layout configuration, allowing the exploitation of a low-cost, low-power and light-weight camera at the curved focal surface of the telescope [2].

The focal plane of the ASTRI telescope is based on silicon photomultiplier (SiPM) detectors, and requires a proper front-end electronics which is able to catch the very fast pulses of the Cherenkov light [3], [4].

CITIROC is essentially a 32-channel fully-analog front-end ASIC dedicated to the gain trimming and read-out of SiPMs. Its analogue core is sensitive to positive SiPM signals. For each channel, two parallel AC-coupled voltage pre-amplifiers ensure the read-out of the pulse charge. Two tunable slow-shapers are implemented to reduce the noise components amplitude out of a specific pre-determined frequency range; each shaper provides an adjustable output peaking time from 25ns to 175ns to allow for noise reduction depending on the final application. A trigger line is available on both low-gain and high-gain pre-amplifiers, which is formed by a 15-ns peaking time fast-shaper cascaded to an open-loop discriminator producing the trigger signal, with a tunable threshold provided by a dedicated digital-to-analogue converter exploited as a reference voltage.

The availability of a high-level circuit model of the CITIROC analog core is fundamental for an in-depth understanding and a reliable interpretation of the physical interactions between the SiPM detection system and the conditioning electronics to help choose the optimal front-end architecture. On the basis of such a model, reliable circuit-level simulations can be performed on the SiPM detector coupled to the front-end electronics, and the main characteristics of the resulting signals can be conveniently related to the model parameters of SiPM detectors and front-end electronics. In addition, a simulated front-end model may also be profitably exploited for choosing the optimal front-end architecture for the particular application requirements before executing experimental measurements on the real chip.

The present paper is devoted to the realization and simulation of the fully analog model of CITIROC as a read-out system at the focal plane of the ASTRI telescope, so as to promote some additional understanding of the signal conditioning electronics for the optical sensors of the camera, and confirm its theoretical effectiveness in driving its output signals. The complete circuit implementation of the chip model hereby proposed can serve as a simple and effective approach for performing preliminary circuit-level simulations of the SiPM electronic front-end.

The article is organized as follows. In section II the implemented analog front-end is depicted. In particular, after a brief description of the SiPM electrical model for the generation of the input pulses, subsections IIA and IIB respectively address the dual-line pre-amplifier and the slow noise-shaping section models; in subsection IIC the high-gain line fast-shaper model is discussed, along with the trigger generation circuit; subsection IID is then devoted to the design and implementation of the double chain models of the sample-and-hold and peak detector memory blocks for digital data acquisition. Finally, section III summarizes the authors conclusions and outlook.

II. Analog Front-End Model

The entire simulated analog front-end is illustrated in Fig. 1. It basically consists of a pre-amplifier section including a pair of adjustable low-gain and high-gain capacitive-feedback amplifiers modulating the pulse voltage amplitude in accordance with specific sensitivity requirements, a noise-shaping section for noise filtering, composed of a bipolar fast-shaper and two

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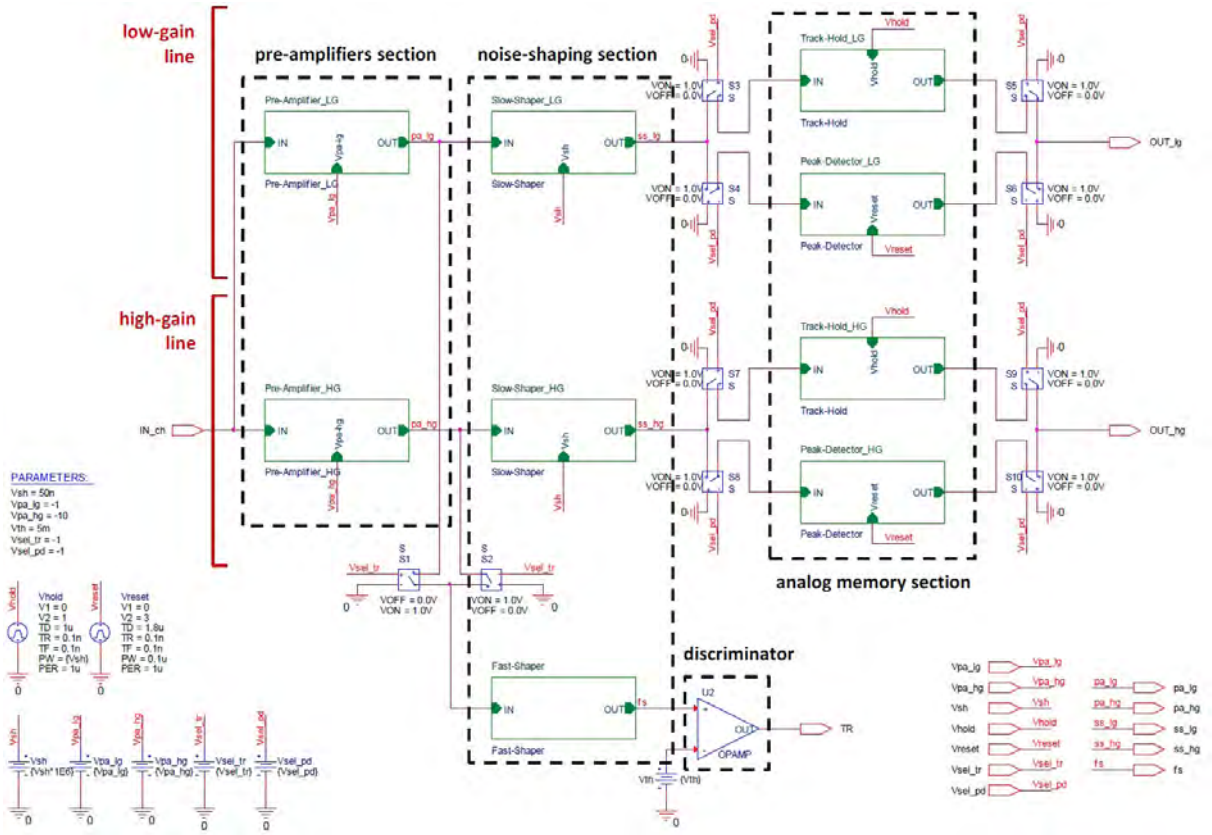

Fig. 1. Fully-analog CITIROC high-level front-end circuit schematic model used for simulations.

tunable shaping time slow shapers, a fast single-threshold discriminator for the trigger generation, and an analogue memory section implementing both sample-and-hold and peak detection approaches for digital data acquisition.

A few additional control voltages are introduced in the full simulated front-end model, which allow the user to selectively choose the desired design parameters and offer the versatility of launching parametric analyses to plot family curves for different design conditions. More specifically, the programmable parameters by means of which the realized model can control the analogue signal processing of the input detectors, act upon:

- the closed-loop gain of the low-gain pre-amplifier;
- the closed-loop gain of the high-gain pre-amplifier;
- the shaping time of the slow-shapers;
- the sampling frequency of the track-and-hold cells;
- the reset signal of the peak detectors;
- the low-gain/high-gain trigger line selection;
- the track-and-hold/peak detector line selection;
- the reference threshold of the discriminator.

The parameter values controlling the above mentioned issues may even be simultaneously changed to achieve different performance levels. However, when launching parametric simulations, the tuneable parameters need to be individually selected to obtain different curve plots.

The photon detection system chosen for the ASTRI camera is based on a small monolithic multi-pixel detector produced by Hamamatsu, consisting of a 4×4-pixel SiPM array. The single pixel has a 3×3-mm actual dimension and is composed by 3600 50×50-µm single-photon avalanche photodiodes operating in the so-called Geiger mode by setting a reverse biasing voltage greater than the nominal breakdown voltage.

The electrical SiPM model reported in [5], here sketched in Fig. 2, is employed to generate the input voltage pulses on the basis of the behaviour of each single microcell composing the whole detector structure.

The above equivalent model simulates the discharge of N_f cells in a SiPM consisting of a total number N_{tot} of microcells. The circuit is formed by an active part (on the left), representing the number N_f of fired microcells connected in parallel, and a passive block (on the right) for the remaining $N_p = N_{tot} - N_f$ unfired cells. The dashed box outlines the pulse generation.

Referring to the circuit, C_d is the capacitance of the reverse-biased diode, R_d is the series resistance of the avalanche photodiode, R_q is the quenching resistor, and C_q is its associated stray capacitance. The switch is implemented in such a way that it closes at a preset time, thus marking the start of a breakdown event. The switch then monitors the photodiode current flowing through the diode (i.e., through R_d and V_{BD}) and opens when it drops below a predefined threshold current.

The SiPM output voltage pulses which are mimicked by the adopted electrical model when closed on a 50-Ω load resistor R_L are characterized by the following dynamic features:

- rise time constant $\tau_{rise} \approx 1$ns;
- fall time constant $\tau_{fall} \approx 50$ns.

For the sake of simplicity, the external bias voltage is selected so as to produce a peak amplitude $V_{peak} \approx 100$µV.

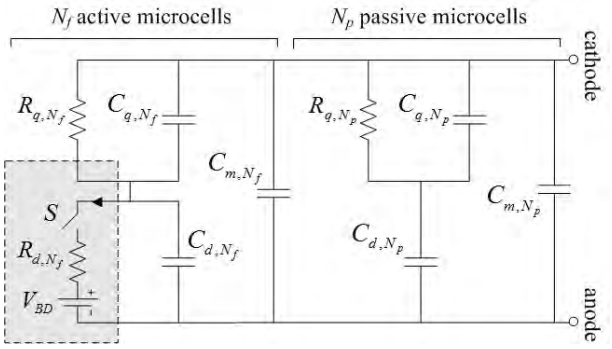

Fig. 2. Simplified equivalent electrical model for the input SiPM detectors. The dashed box highlights the current pulse generation.

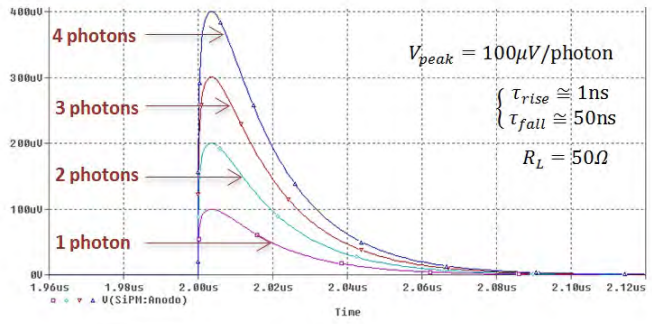

Fig. 3. Simulated time response of the PDM SiPM circuit model for a different number of detected photons.

A parametric time simulation of the SiPM model for different values of N_f is reported in Fig. 3, showing a plot of waveforms with different amplitudes related to the number of input photons detected by the input SiPM detectors. As can be inspected, the peak voltage of the simulated pulses linearly rises as a function of the fired microcells.

These output-generated pulse signals now feed the CITIROC single-channel input, and are then processed by the subsequent blocks of the front-end model. The following subsections will describe the architecture and simulate the performance of each single part of the analyzed electronic front-end in response to the input voltage pulses generated by the SiPM model.

A. Pre-amplifier Section Model

Each analog channel of the CITIROC chip embeds a pair of independently-programmable variable-gain pre-amplifiers ensuring a versatile coverage of the dynamic range depending on the specific application purpose. Both low-gain and high-gain pre-amplifiers can be adjusted by the back-end digital control circuitry (FPGA), allowing a negative gain range variation from -1 to -15 for the low-gain pre-amplifier, and from -10 to -150 for the high-gain pre-amplifier.

A simplified schematic model of the variable-gain capacitive-feedback operational amplifier embedded in the CITIROC chip is depicted in Fig. 4. The above circuit architecture is employed to generate both a low-gain and a high-gain closed-loop transfer function $A_V(s)$ by means of the tunable feedback capacitance C_F. Assuming an ideal open-loop amplifier yields

$$A_V(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{C_S}{C_F} \tag{1}$$

The circuit models of low-gain and high-gain pre-amplifier sections are implemented as illustrated in Fig. 5 and in Fig. 6, respectively. The adjustable feedback capacitance is henceforth realized by exploiting a combination of parallel circuit branches including the series connection between a fixed-valued capacitor and a voltage-controlled switch. The PSPICE library model employed for the ideal switches relies on a 1-Ω equivalent on-resistance and a purely-passive 1-MΩ off-state impedance.

As a consequence of the adopted connection, the resulting transfer function is strongly related to the amplitude of the DC voltage signal controlling the switches, and can be expressed as a function of the digital switch state

$$A_V(s) = -\frac{C_S}{\sum_i C_{Fi} S_i} \tag{2}$$

where C_{Fi} is the i-th feedback branch capacitor and S_i is the logic value associated with the i-th controlled switch S_i.

More specifically, referring, for instance, to the low-gain pre-amplifier model in Fig. 5, when the sole switch S_15 is closed, capacitor C_F_15 turns out to be the sole contribution to the total feedback capacitance, and a voltage gain of -15 is obtained. Similarly, when the switch S_7.5 is in the on-state, the equivalent feedback capacitance is given by the parallel connection of C_F_15 and C_F_7.5, thus decrementing the resulting negative gain to -7.5. When all switches are turned on, the feedback loop capacitors in all branches are parallel-connected with an overall contribution of 1.5pF, implying a minimum achievable gain of -1. Seven theoretical gain values can be accomplished for the adopted low-gain and high-gain pre-amplifier models, as also indicated in the right-side tables in Fig. 5 and Fig. 6. Of course, the off-state threshold voltages of the feedback switches are designed to avoid overlapping commutations.

The tunable signals controlling the feedback switches for the low-gain and high-gain pre-amplifiers are modeled by two DC voltage sources of adjustable values, whose labels are included in the list of the PSICE parametric global variables. Therefore, to achieve a specific gain value for each input pre-amplifier, the user simply has to assign the corresponding DC voltage values to their global parameters $\{V_{pa}$-lg$\}$ and $\{V_{pa}$-hg$\}$ directly from the display property windows of the relevant voltage sources.

A parametric transient sweep analysis is carried out for both input pre-amplifiers by setting up all the available voltage gains

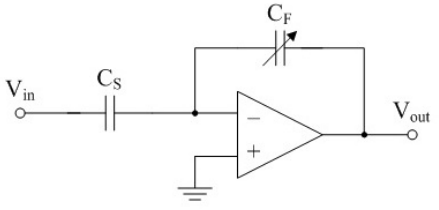

Fig. 4. Simplified schematic of the variable-gain operational amplifier embedded in the CITIROC chip.

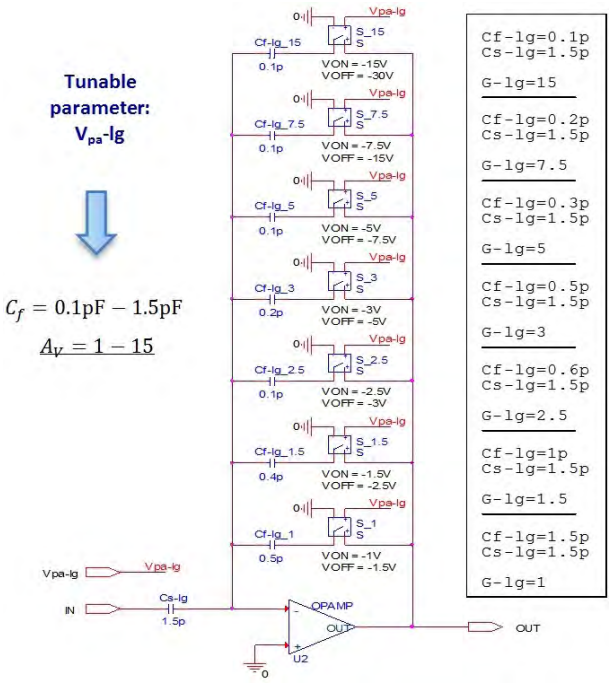

Fig. 5. Schematic model of the CITIROC low-gain pre-amplifier section. The inset table relates the selected capacitance values to the achieved gain.

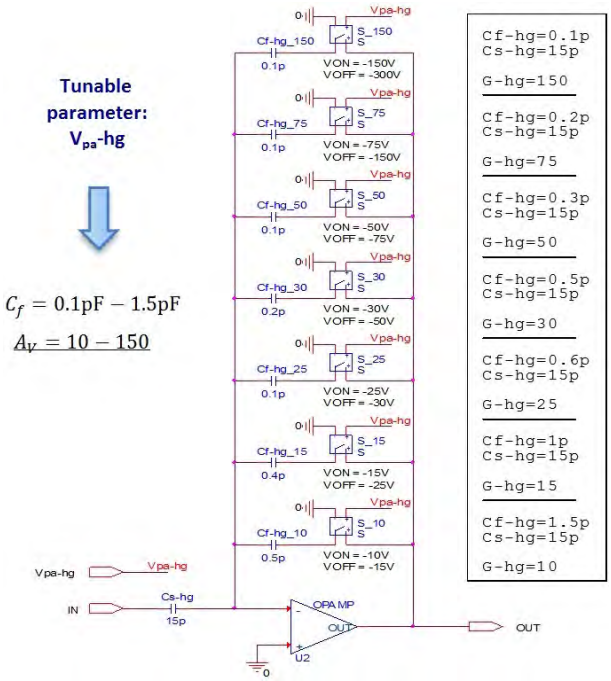

Fig. 6. Schematic model of the CITIROC high-gain pre-amplifier section. The inset table related the selected capacitance values to the achieved gain.

through the dedicated global variables and plotting the related family curves. The time response of each pre-amplifier model to a single input pulse is illustrated in Fig. 7. The collected amplified waveforms are phase-inverted compared to the input signal pulse, owing to the inverting amplifier feedback configuration. The negative peaking voltages of the output pulses are found to raise up linearly with increasing values of the amplifier gain A_V

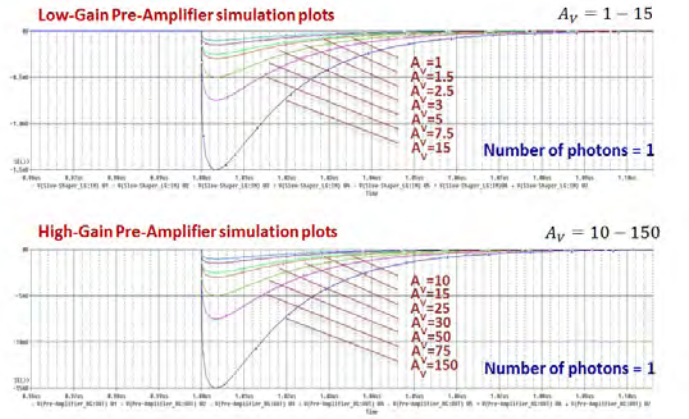

Fig. 7. Simulated transient sweep responses of the low-gain (on top) and high-gain (on bottom) input pre-amplifier models for all achievable gain values, in response to a single input photon.

for both low-gain and high-gain pre-amplifiers, thus confirming the accuracy of the adopted model.

It should finally be remarked that, in case of multiple overlapped pulses, the maximum achievable high gain is limited by the amplifier negative saturation voltage.

The amplified pulse signals at the output of the pre-amplifier sections are then applied to the input of the noise-shapers.

B. Slow-Shaper Section Model

A slow noise-shaper section with selectable shaping time is integrated in each single channel of CITIROC to provide charge measurements. A dual-active slow-shaper line is inserted at the output of both low-gain and high-gain pre-amplifiers.

The simplified schematic of the programmable shaping time slow-shapers of CITIROC is depicted in Fig. 8.

The circuit topology is composed by a common passive RC integrator cascaded with an active band-pass filter. A unity-gain buffer is introduced between them to avoid loading effects. All time constants of the above circuit are designed to be identical by means of a suitable choice of the passive elements, and can be varied by adjusting capacitances C_1, C_2 and C_3 in such a way to maintain a constant product with the relevant resistances R_1, R_2 and R_3, respectively. Seven slow shaping times can be selectively generated by the CITIROC digital control system, in a range from 25ns to 175ns with a 25-ns linear increment.

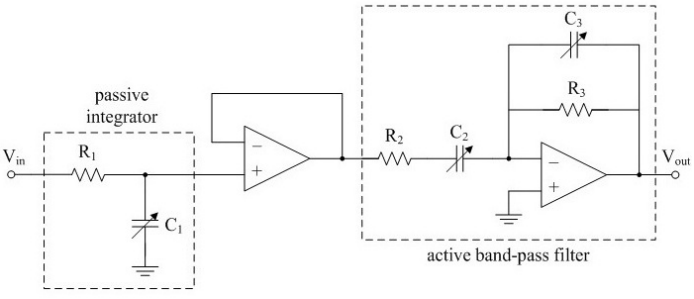

Fig. 8. Schematic of the variable shaping time slow-shapers embedded in the CITIROC chip.

Assuming ideal operational amplifiers for both slow-shaper architectures in Fig. 8, the circuit small-signal transfer function is found to be expressed by a third-order polynomial

$$A_V(s) = \frac{V_{out}(s)}{V_{in}(s)} = \\ = -\frac{sR_3C_2}{(1+sR_1C_1)(1+sR_2C_2)(1+sR_3C_3)} \quad (3)$$

Under the following design condition on the passive elements

$$R_1C_1 = R_2C_2 = R_3C_3 = \tau \quad (4)$$

the above transfer function can be more conveniently rewritten as a function of the shaping time τ, thus yielding

$$H(s) = -\frac{R_3}{R_2}\frac{s\tau}{(1+s\tau)^3} = -\frac{C_2}{C_3}\frac{s\tau}{(1+s\tau)^3} \quad (5)$$

The slow-shapers have a triple-pole transfer function, with a zero at the origin of the complex s-plane generated by the series capacitor C_2. The frequency of the third-order multiplicity pole is determined by the reciprocal of the time constant in (6).

The magnitude of $H(s)$, calculated at the purely-imaginary complex frequency $s = j\Omega$, can be easily derived as

$$|H(j\omega)| = \frac{R_3}{R_2}\frac{\omega\tau}{\sqrt{\left[1+(\omega\tau)^2\right]^3}} = \frac{C_2}{C_3}\frac{\omega\tau}{\sqrt{\left[1+(\omega\tau)^2\right]^3}} \quad (6)$$

Nullifying the first derivative in (6) with respect to the angular frequency ω, yields the left half-plane pole frequency ω_{peak} at which the magnitude of the previous slow-shaper transfer function achieves the highest value

$$\omega_{peak} = \frac{1}{\sqrt{2}\tau} \quad (7)$$

Substituting this peak frequency into the original slow-shaper transfer function expression in (5), the amplitude of the maximum obtainable gain is established

$$|H(j\omega_{peak})| = \frac{4}{3\sqrt{3}}\left(\frac{1}{2}\frac{R_3}{R_2}\right) = \frac{4}{3\sqrt{3}}\left(\frac{1}{2}\frac{C_2}{C_3}\right) \quad (8)$$

A maximum constant gain independent of the shaping time τ and related to a resistance or capacitance ratio is thus achieved in the adopted slow-shaper topology. This can involve an additional gain component for the pre-amplified input pulses when processed by the noise-shaping sections of the CITIROC front-end, depending on the spectral content of the input pulses.

The circuit schematics of both low-gain and high-gain slow-shapers are implemented as illustrated in Fig. 9. Three circuit branches including parallel-connected capacitors and voltage-controlled switches are exploited for adjusting the shaping time constant τ. In particular, the switching signals in each branch are synchronized to each other in order to control the three RC constants simultaneously.

As a result, the tuneable shaping time τ of the adopted slow-shaper models can be expressed as

$$\tau = R_1\sum_i C_{1i}S_{1i} = R_2\sum_i C_{2i}S_{2i} = R_3\sum_i C_{3i}S_{3i} \quad (9)$$

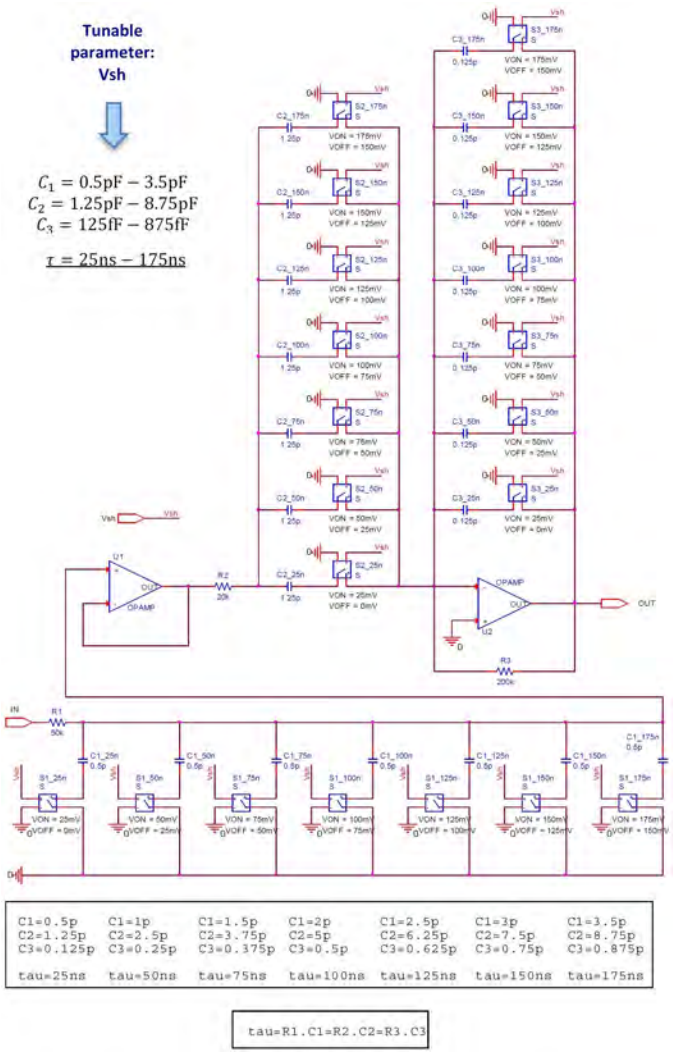

Fig. 9. Schematic circuit model of the tunable shaping time slow-shapers of the CITIROC chip (on the left) and tuneable capacitor values and relevant shaping times for the adopted slow-shaper model (on the right).

in which C_{1i}, C_{2i} and C_{3i} are the fixed capacitances in the i-th branches while S_{1i}, S_{2i} and S_{3i} are the digital states of the i-th controlled switches.

More specifically, when only switches S1_25n, S2_25n and S3_25n are on, capacitors C1_25n, C2_25n and C3_25n turn out to be the unique contributions to the overall parallel capacitances, and the slowest time constant is set for all RC branches. Similarly, when switches S1_50n, S2_50n and S3_50n enter the on-state as well, the equivalent branch capacitors get raised accordingly, thus increasing the resulting shaping time. When all switches are turned on, then all capacitors become parallel-connected, yielding the slowest time constant value in all three branches. Seven theoretical shaping times can be accomplished for the employed low-gain and high-gain slow-shaper models, as tabulated in Fig. 9. To this purpose, the off-state thresholds deactivating the voltage-controlled switches are properly synchronized to avoid undesired overlap.

The above operation mode is similar to that occurring when selecting the voltage gains of the low-gain and high-gain pre-amplifiers, except for the inverted polarity of the static control

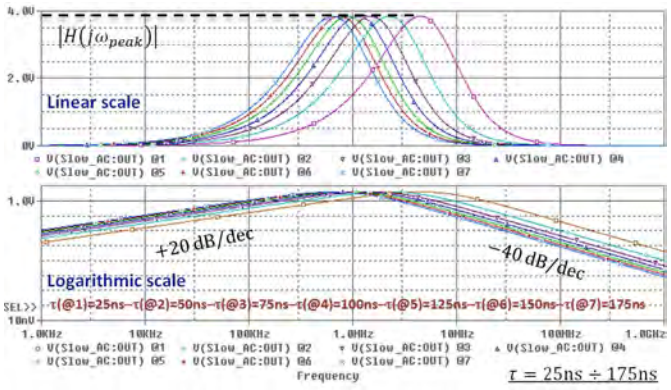

Fig. 10. Simulated frequency responses of the CITIROC slow-shaper circuits in both linear scale (on top) and logarithmic scale (on bottom).

signals. In fact, the highest shaping time is obtained when all switches are enabled, that is for the corresponding maximum control voltage value. Conversely, the lowest pre-amplifier inverting gains (-1 or -10) are achieved when the highest DC voltages (-1V or -10V) are applied to the control signals.

The tuneable signal controlling the slow-shaper switches is realized through an adjustable DC voltage source, whose absolute numerical value can be selected by the parametric global variable $\{V_{sh}\}$ defining the value of the shaping time constant. It should be remarked that an arbitrary scaling factor of 10^6 is opportunely added when outputting the voltage control signals enabling and disabling all the controlled switches, in order for these values to be compliant with the PSPICE specifications of the switch model (excessively small voltage thresholds cannot be recognized as switching signals).

Parametric frequency and transient sweep analyses are performed on the implemented slow-shaper model by varying the shaping time constant τ as well as the number of input pulses. To get the time constants ranging from 25ns to 175ns with the capacitor values listed in Fig. 9, resistors R_1, R_2 and R_3 of both CITIROC low-gain and high-gain slow-shapers are chosen to be 20kΩ, 50kΩ and 200kΩ, respectively.

To evaluate the spectral response of the proposed slow-shaper model and validate the frequency analysis, AC magnitude simulations are carried out as functions of the tunable shaping times. Parametric sweep results for all the available values of the slow-shaper time constant are reported in Fig. 10 in both linear and logarithmic scales.

As expected by the theoretical pencil-and-paper evaluation, all spectral curves linearly raise up with a positive 20-dB per-decade excursion until the third-order pole frequency, and afterwards decrease by a negative 40-dB per decade linear slope. The system cut-off frequency is proved to be inversely proportional to the shaping time constant, in perfect agreement with expression (7), hence ranging between 640kHz (for $\tau = 175$ns) and 4.5MHz (for $\tau = 25$ns). On the other side, the magnitude at the peak frequency is found to be independent of the particular shaping time, and reaches a maximum value of 3.85 according to relationship (8). Therefore, as previously already remarked, the noise-shaping section of the analog front-end can introduce an additional gain component to the pre-amplified input pulses, whose amplitude is strictly related to the spectral content of the SiPM pulse signals.

To confirm the effectiveness of the adopted read-out model when processing the SiPM pulses from the pre-amplifier sections of the analogue front-end, parametric transient sweeps are performed as well. Fig. 11 depicts the time-domain responses of both slow-shapers to an input photon pulse, and turns out to be particularly helpful to evaluate the correlation between the slow-shaper time constant and the peaking time of its transient response (i.e., the time delay from the instant in which the input pulse begins to rise and that in which the slow-shaper amplitude reaches its output peaking value).

Observing these curve plots, it can be inferred that greater shaping time values produce the effect of modulating the slow-shaper output waveform by decreasing its peak amplitude and delaying its peaking time.

In order to illustrate the functional relationship between the slow-shaper time constant and the peaking time of the circuit transient response to a single voltage pulse, Table I summarizes the simulated peaking times of both shapers for all available shaping times. The listed results refer to both slow-shaper responses to a single input pulse under a minimum pre-amplifier gain; however, equivalent peaking time values are obtained by increasing the number of input photons. Table I also collects the gain factors introduced by the slow-shaper circuit models for the voltage peak amplitude.

By inspection of the listed values, it turns out that a 50-ns shaping time for the slow-shaper models achieves the closest correspondence to the relevant output peaking time as well as an almost unity gain factor for the peak amplitude of the pulse signals. This feature will later emerge from the simulated curves of the sample-and-hold section. Of course, the optimal shaping time has to be considered for each type of SiPM.

Fig. 12 reports the parametric simulations of the slow-shaper transient responses to a few different input pulses, for a shaping time of 25ns (on the left) and 50ns (on the right). As previously remarked, the amplitude of the output waveforms linearly rises with increasing values of the input peak pulse voltage; nevertheless, the peaking times of the shaping circuits are found to have the same values regardless of the number of photons detected.

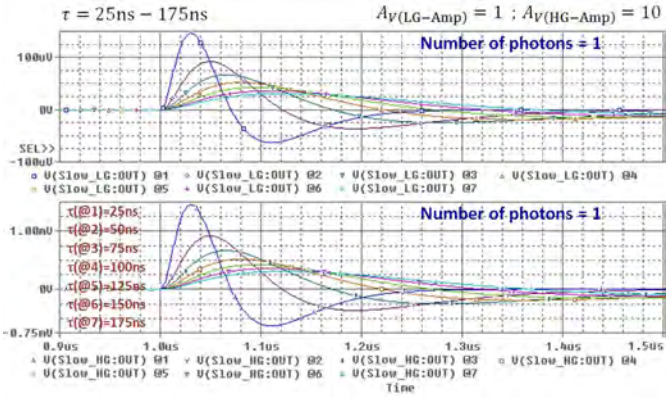

Fig. 11. Parametric time responses of the low-gain and high-gain slow-shaper equivalent models to a single input photon pulse under a minimum pre-amplifier gain, for all available shaping time values.

TABLE I
SIMULATED PEAKING TIMES AND GAIN FACTORS OF THE SLOW-SHAPER MODELS FOR ALL AVAILABLE TIME CONSTANTS

	τ=25ns	τ=50ns	τ=75ns	τ=100ns	τ=125ns	τ=150ns	τ=175ns
slow-shapers peaking times *	30.2ns	49.2ns	65.2ns	80.2ns	95.2ns	109.2ns	124.2ns
slow-shapers peaking gains *	1.457	0.921	0.667	0.520	0.425	0.359	0.309

* for a single input photon

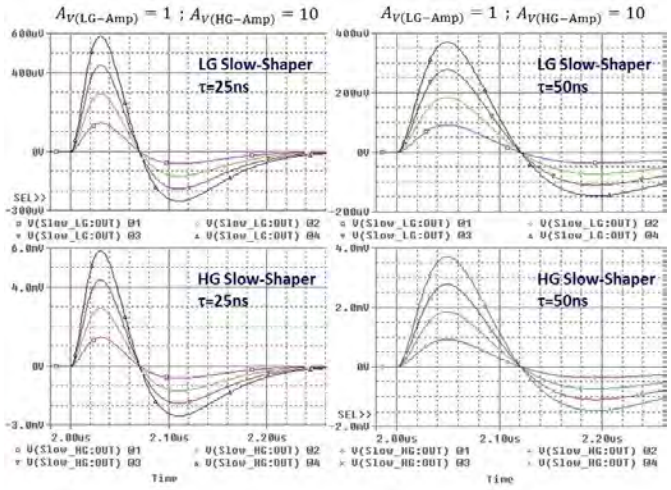

Fig. 12. Parametric time responses of the low-gain and high-gain slow-shaper circuit models to different input pulses under a minimum pre-amplifier gain, for an equal shaping time of 25ns (on the left) and 50ns (on the right).

Also, the output waveforms in Fig. 12 are voltage-inverted compared to the pulse signals at the output of the pre-amplifier sections, due to the circuit phase-inverting topology.

The low-gain and high-gain slow-shaper signals finally get to the analog memory cells sections of the front-end model, which must be capable of sampling the analogue values of the shaped signals when approaching their peak voltage.

C. Trigger Generation Model

A fast noise-shaper section with a fixed shaping time is also integrated in each channel of the CITIROC chip, at the output of the pre-amplifier lines. Its output voltage signal is subsequently compared to a selectable reference threshold by means of a line discriminator, providing the trigger signal.

The user is allowed to select which of the two pre-amplifier outputs has to be connected to the fast-shaper input, depending on specific application targets. This is implemented in the high-level circuit model in Fig. 1 exploiting a pair of opposite-phase voltage-controlled switches acting as a two-input multiplexer. The binary control parameter $\{V_{sel}$-tr$\}$ is thus used to connect the fast-shaper input to the desired pre-amplifier branch.

The simplified schematic circuit of the CITIROC fast-shaper is sketched in Fig. 13, and recalls the conventional active band-pass filter employed in the slow-shaper architecture in Fig. 11.

Assuming an ideal operational amplifier, the circuit transfer function is found to be expressed by

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{sR_FC_S}{(1+sR_SC_S)(1+sR_FC_F)} \qquad (10)$$

Under the following design condition on the passive elements

$$R_SC_S = R_FC_F = \tau \qquad (11)$$

the above transfer function can be expressed as a function of the shaping time constant τ, hence yielding

$$H(s) = -\frac{R_F}{R_S}\frac{s\tau}{(1+s\tau)^2} = -\frac{C_S}{C_F}\frac{s\tau}{(1+s\tau)^2} \qquad (12)$$

The fast-shaper has a second-order transfer function, with a zero at the origin of the complex s-plane generated by the series capacitor C_S. The frequency of the double-multiplicity pole is determined by the reciprocal of the time constant τ, as occurs in the slow-shaper transfer function.

The magnitude of $H(s)$, calculated at the purely-imaginary complex frequency $s = j\Omega$, is

$$|H(j\omega)| = \frac{R_F}{R_S}\frac{\omega\tau}{1+(\omega\tau)^2} = \frac{C_S}{C_F}\frac{\omega\tau}{1+(\omega\tau)^2} \qquad (13)$$

Equating to zero the first derivative in (13) with respect to the angular frequency ω, yields the left half-plane pole frequency, ω_{peak}, at which the magnitude of the above fast-shaper transfer function assumes the highest value

$$\omega_{peak} = \frac{1}{\tau} \qquad (14)$$

Substituting this peak frequency into the original fast-shaper transfer function expression in (12), the amplitude of the maximum gain is obtained

$$|H(j\omega_{peak})| = \frac{1}{2}\frac{R_F}{R_S} = \frac{1}{2}\frac{C_S}{C_F} \qquad (15)$$

Therefore, as for the slow-shaper circuits, a maximum constant gain independent of the shaping time and related to a resistance or capacitance ratio is achieved for the implemented fast-shaper topology. This may cause an additional gain component for the pre-amplified input signals even when processed by the fast-shaping section of the CITIROC front-end, according to the spectral content of the input pulses.

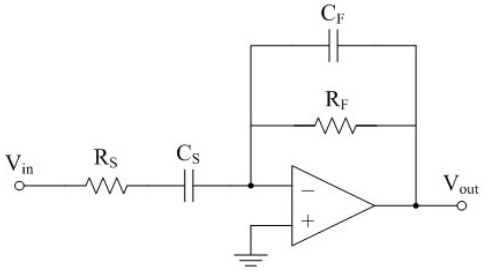

Fig. 13. Schematic of the fast-shaper circuit embedded in the CITIROC chip.

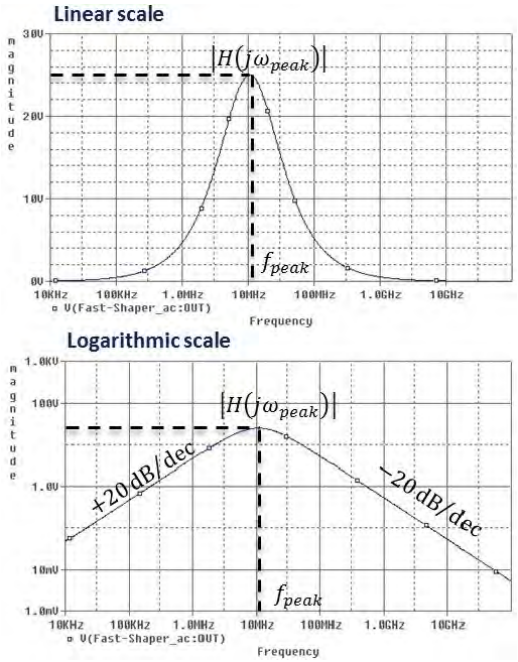

Fig. 14. Simulated frequency responses of the CITIROC fast-shaper circuit in both linear scale (on top) and logarithmic scale (on bottom).

Parametric frequency and transient sweep analyses are performed on the implemented fast-shaper model by varying the number of input photon pulses. To achieve a 15-ns fast-shaping constant, resistances R_S and R_F are selected to be 1.5kΩ and 75kΩ, respectively, while capacitances C_S and C_F are designed to be 10pF and 200fF, respectively.

To evaluate the frequency response of the fast-shaper model and validate the developed analysis, AC magnitude simulations are carried out in both linear and logarithmic scale, as illustrated in the relevant graphs in Fig. 14.

As expected by the theoretical evaluation, the spectral curve linearly increases with a positive +20-dB per decade excursion until the second-order pole frequency, and afterwards decreases by a negative −20-dB per decade linear slope. The system cut-off frequency is found to be 11MHz, in perfect agreement with expression (14). On the other hand, the magnitude at this peak frequency reaches a maximum value of 25, in accordance with relationship (15). Thus, as also highlighted for the slow-shaper model, the fast-shaping section of the CITIROC front-end also accounts for the overall gain factor of the entire channel line. Besides, the incremental gain introduced by the fast-shaper, still related to the spectral content of the pulse signals, is even more consistent compared to that achieved by the slow-shaper circuit. Fig. 15 better remarks the above concept by comparing the AC magnitude diagrams of both shapers transfer functions.

To demonstrate the effectiveness of the adopted model when processing the signals coming from the high-gain pre-amplifier section of the analog front-end, parametric transient sweeps are also carried out. Fig. 16 illustrates the time-domain simulation response of the fast-shaper to different incident photon pulses, for the minimum pre-amplifier high gain.

The amplitude of the fast-shaper output waveforms linearly raise up with increasing peak values of the input pulse voltage.

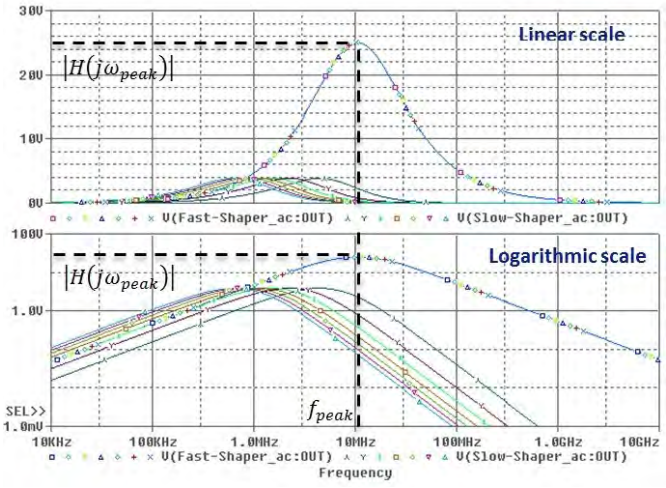

Fig. 15. Fast-shaper versus slow-shaper frequency responses for all available values of the slow-shaping time (25ns-175ns).

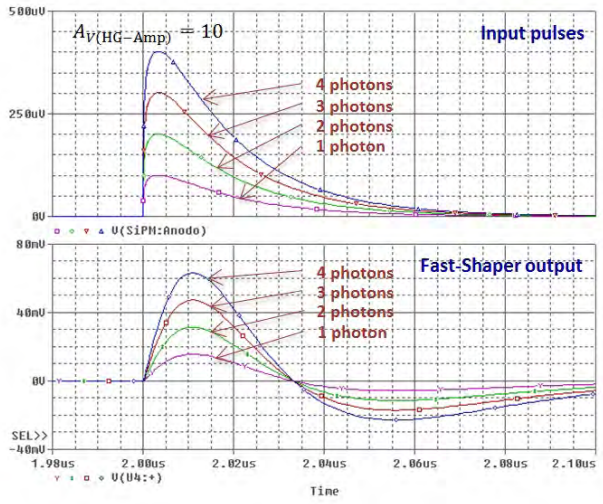

Fig. 16. Parametric time responses of the fast-shaper model to different input photon pulses under a minimum pre-amplifier high gain.

An overall gain factor of about 16 is detected for the realized fast-shaper model with respect to the single input pulse, aside from the gain of the previous pre-amplifier section.

Once again, the correlation between the shaping constant and the peaking time of the fast-shaper time response is evident. An 11.2-ns delay time is found from the raising of the input pulses, regardless of their voltage amplitudes.

The fast-shaper waveforms in Fig. 16 are voltage-inverted, as those at the slow-shaper outputs, compared to the pulse signals at the output of the high-gain pre-amplifier, due to the phase-inverting topology of the fast-shaper.

The simulated transient responses of the high-gain line channel of the front-end to a single incident photon is illustrated in Fig. 17, showing a single pulse waveform and its high-gain pre-amplified output (upon a gain factor of 10), as well as the plot curves at the subsequent high-gain shapers outputs.

The quicker shaping time constant of the fast-shaper section with respect to the slow-shaper counterpart makes it feasible to generate a trigger signal starting from the previously available

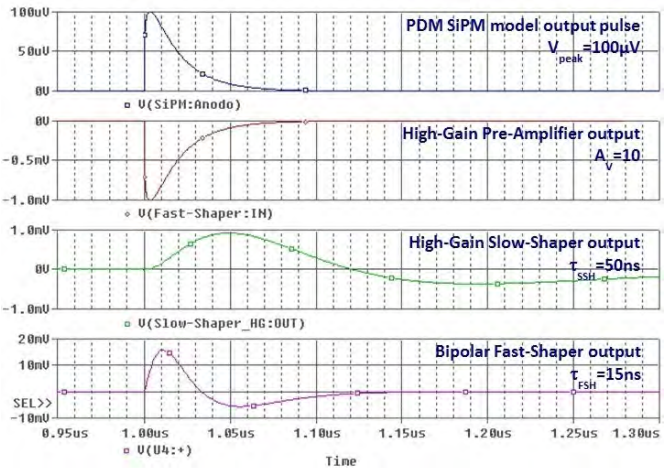

Fig. 17. Simulated time responses of the high-gain line channel of the realized analog front-end model to a single input photon pulse, for a slow-shaping time of 50ns and a high-gain factor of 10.

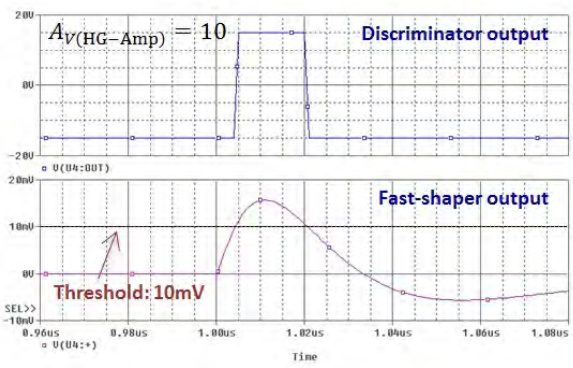

Fig. 18. Simulated discriminator output response with a 10-mV threshold, for an input pulse with a high pre-amplifier gain of 10.

output waveform of the fast-shaper circuit. Thus, the output signal from the fast-shaping channel is compared to an adjustable threshold discriminator cascaded with the fast-shaper circuit, as shown in the full schematic model of Fig. 1.

Fig. 18 depicts the discriminator output time response upon a reference threshold of 10mV, for an input pulse with a high pre-amplified gain of 10. The saturation voltages of the open-loop operational amplifier model are set to $\pm$15V.

The adjustable threshold of the discriminator is modeled by a voltage generator with a tunable DC value, whose label is added to the list of the PSPICE parametric global variables. Therefore, to set a specific reference threshold for the comparator, the user solely has to assign the corresponding static voltage value to the dedicated global parameter $\{V_{th}\}$ directly from the component property window of the voltage source.

D. Analog Memory Cells Section Model

The CITIROC front-end chip is expected to control and save the amplitude of the slow-shaper signals when approaching the peaking values. This can be accomplished either by two analog track-and-hold cells or by two independent peak detectors, both inserted at the end of the dual-line channel of the front-end.

The track-and-hold cells basically capture the analog values of the input waveforms according to an external control signal with a fixed sampling frequency. Conversely, the peak detectors allow to maintain the peak values of the analog inputs as long as an external reset signal is applied. To selectively choose which kind of analog data acquisition has to be performed, depending on the specific application, a double pair of voltage-controlled switches with opposite thresholds is exploited as shown in the front-end model in Fig. 1, where the binary control parameter $\{V_{sel}$-pd$\}$ is used to simultaneously connect both slow-shaper outputs to the desired analog acquisition branches.

The circuit schematic model of the implemented sample-and-hold memory for the digital acquisition of the peak amplitude in both shaping lines of the read-out channel is represented in Fig. 19. A voltage-controlled switch is exploited to regulate the sampling frequency of the memory cells, a storage capacitor C is adopted to supply the dynamic storage of the analogue data, and a unitary-gain amplifier is finally connected to the output of each memory cell to maintain the correct analog information and prevent the stored voltage from decaying.

The value of the storage capacitor must be accurately set, in a design step, to fulfil a suitable trade-off between contradicting design requirements. Actually, an excessively small value of C would entail unavoidable voltage losses of the stored data, due to the finite equivalent impedance of the controlled switches; on the contrary, too high values of C could involve a remarkable exponential rise time delay when sampling the analog voltages coming from the slow-shaper outputs. In the adopted design, an optimum capacitor value of 100pF is determined.

The voltage pulse generator V_{hold} in Fig. 1 is used to sense the controlled switches according to the desired sampling frequency. For the actual design, based on the existing connection between the shaping constant of the slow-shaper circuits and the peaking time of their shaped output waveforms, the sampling clock is chosen to provide a pulse-width (from the input pulse rise) equal to the preceding slow-shaper time constant. To this purpose, the global variable $\{V_{sh}\}$, controlling the shaping time of both low-gain and high-gain shapers, is added to the pulse-width field of the voltage source V_{hold}.

The simulated output waveforms of the track-and-hold cell of the high-gain line, for a few different shaping time values and a single input photon pulse, are reported in Fig. 20. The pulse-width of the source V_{hold}, controlling the switching frequency, is synchronized with the nominal shaping time of the high-gain shaper by means of the same parametric variable definition. As a consequence, the analog voltage value of the shaped signal is held across the storage capacitor C after a time delay which is

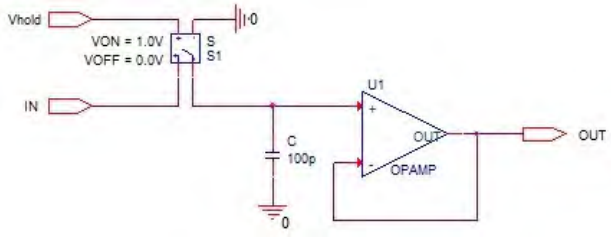

Fig. 19. Circuit schematic model of the dual-line track-and-hold cell.

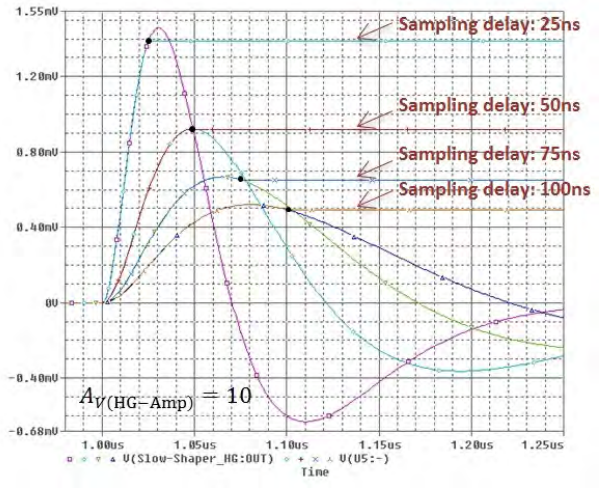

Fig. 20. Transient simulation results of the high-gain track-and-hold outputs for different shaping times.

determined by the time constant of the high-gain slow-shaper. Thereby, the stored information is transferred to the output node for the subsequent digital data processing.

As can be observed, a 50-ns delay time from the pulse rising ensures a stored voltage value that exhibits the closest matching with the peaking value of the shaped signal, thus confirming the obtained results in Table I.

However, depending on the particular application context, to achieve a higher accuracy on the sampled information, a pair of independent peak detectors can be adopted at the outputs of the slow-shaper chains. The circuit schematic models of each peak detector is represented in Fig. 21. The first operational amplifier acts as a unity-gain voltage follower charging capacitor C_1 up to the peak voltage. If the input voltage is larger, the operational amplifier output goes positive until C_1 is charged up to the new peak value; if the input voltage is lower, the diode D_1 prevents data loss from C_1. The second operational amplifier works as a high impedance buffer preventing C_1 from being discharged. The voltage source V_{reset} in Fig. 1 is applied to the voltage-controlled switch S1 to reset the stored information.

Fig. 22 provides the output waveforms of both low-gain and high-gain peak detectors for a few different shaping times and a single input pulse. As observed, the peak analog voltages are saved and kept as long as the reset signal is applied.

The read-out operation of the analog memory sections is performed by the digital control registers of the back-end FPGA.

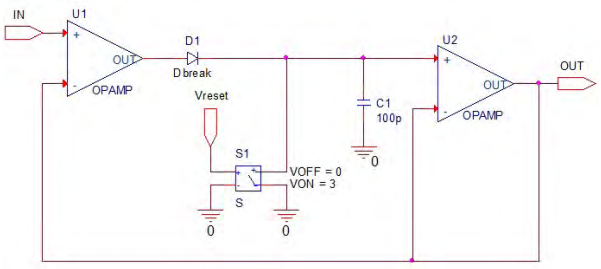

Fig. 21. Circuit schematic model of the dual-line peak detector.

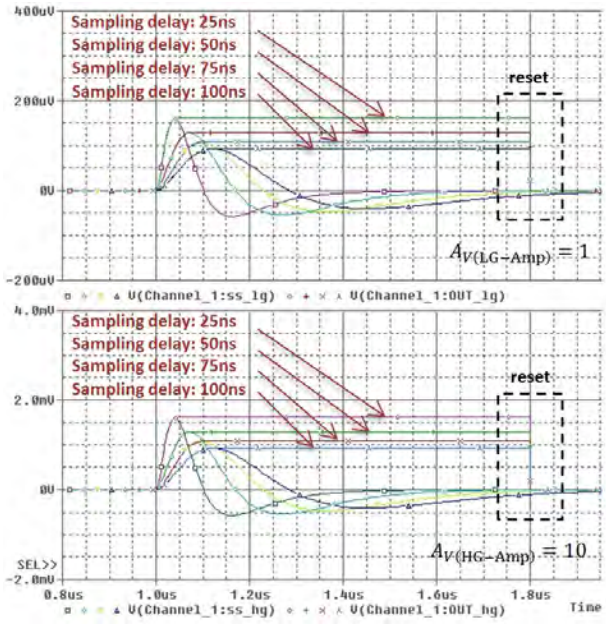

Fig. 22. Simulated low-gain (on top) and high-gain (on bottom) peak detector outputs for different shaping times.

III. Conclusions

The fully-analogue CITIROC front-end model for the SiPM signal read-out is analyzed and developed. Particular emphasis is devoted not only to the purely theoretical aspects, but also to a powerful high-level design approach. Simulations of each single section model are performed to validate the implemented front-end. Time and frequency responses for each circuit block are carried out to show the circuit model behavior and validate the achieved analytical design equations. The proposed front-end model provides a useful and practical simulation tool for analyzing the operating principle and evaluating possible deviations of the operative actual response of the CITIROC signal conditioning electronics from the analytical approach used.

References

[1] The CTA Consortium, *Experimental Astronomy*, vol. 32, issue 3, pp. 193-316, 2011.

[2] R. Canestrari, *et al.*, on behalf of the ASTRI collaboration, "The Italian ASTRI program: an end-to-end dual-mirror telescope prototype for Cherenkov light imaging above few TeV", *32nd International Cosmic Ray Conference*, 2011.

[3] O. Catalano, *et al.*, on behalf of the ASTRI collaboration, "The ASTRI SST-2M Prototype: Camera and Electronics", *33rd International Cosmic Ray Conference*, 2013.

[4] S. Vercellone, *et al.*, on behalf of the ASTRI collaboration, "The ASTRI Mini-Array Science Case", *33rd International Cosmic Ray Conference*, 2013.

[5] D. Marano, *et al.*, "Improved SPICE Electrical Model of Silicon Photomultipliers", *Nuclear Instruments and Methods in Physics Research A*, vol. 726, pp. 1-7, 2013.