A 10 bits three channels 0.35 um SiGe phase shifter

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***Abstract*—**The paper describes an active module for phase control in Active Electronically Scanned Array (AESA) realized in 0.35 µm SiGe BiCMOS technology provided by the AustriaMicroSystem. The system is composed by a digital Phase Control Block (PCB) which generates the three channel square waves with a minimum phase shift of 0.3515° and an output frequency of 1.953MHz, and the PLLs with external VCOs. The system clock is equal to 2GHz. As expected from the simulations, the maximum phase error is less than 0.1° and the rms phase error is less than 0.06°. The complete system has been tested at 2.45 GHz and 3.8 GHz with almost the same maximum phase error and rms from the theory confirming the validity of the architecture.

***Keywords*—**Phase Shifter, Phased Arrays, integrated circuit, PLL, VCO.

I. Introduction

In recent past, the electronically scanned arrays (ESA) are very useful in many applications like automotive, aerospace, military telecommunications, etc… Indeed they allow varying the phase of each element of array electronically. So any mechanical movements are not necessary, reducing costs and sizes of system. The other main advantages of these structures are high directivity, interference rejection, fast scanning response and signal to noise ratio improvement.

The literature reports three main topologies of Electronically Scanned Arrays (ESA) [1]-[7]. Fig. 1a depicts the structure of a Passive ESA (PESA). PESAs use a single Transmit/Receive Module (TRM) and each antenna element requires a separate phase shifter module. The scheme exhibits high insertion losses due to RF operations. On the other hand, PESAs are much common in radar applications due to their low cost and reduced number of components required.

The AESA presents a TRM that directly control the phase of each antenna (Fig. 1b). The system is very flexible and adaptive for many applications and exhibits low insertion losses. Although AESAs present a structure more complex than PESAs, they are very useful for many applications due to their high scalability.

The last topology involves a hybrid scheme, based on a mix between PESA and AESA. Transmitter and Receiver present two different schemes. For the first one, a single transmitter module is present and there is a passive phase module for each antenna.

The receiver scheme instead is similar to an AESA structure (Fig. 1c).

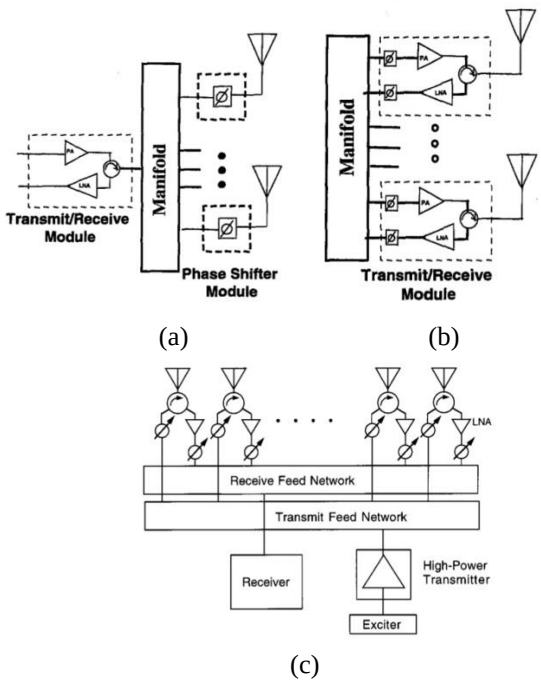


Fig. 1: Electronically Scanned Arrays (a) Passive ESA, (b) Active ESA, (c) Hybrid ESA.

The core of these ESA schemes is the phase shifter, that is, the block that allow generating the phased signal.

The phase shifter related to the ESA scheme can be divided in three different groups. The first one includes the distributed-type phase shifters (DTPSs) [8]. The phase shifters which use a vector sum of two or more orthogonal-phased signals belong to the second group [8]-[10]. Depending on the signal direction this group can be subdivided in forward-type and reflective-type phase shifter (FTPSs, RTPSs). The last group is formed by the phase shifter that uses an all-pass network [7]. The phase shifter can be of digital (discrete phase shift) or analog (continuous phase shift) type.

In this paper an integrated circuit implementation of an evolution of the architecture proposed in [11]-[16] is

presented.

Section II describers the phase shifter basic operation while the section III describes the system architecture. The simulation results are shown in the Section IV while in the Section V the prototype description and experimental results are discussed; finally a conclusion is given in Section VI.

II. Phase Shifter Operation

In Fig. 2it is shown the architecture proposed.

The main system is divided in two macroblocks: the first one is a digital block, named Phase Control Block (PCB), while the second one is a Phase Locked Loop (PLL).

The PCB is composed by a 10-bits counter which drives the *N* 10-bits comparator. An external Digital Signal Processor (DSP) or a microcontroller imposes the phase control word to each digital comparator.

The basic idea is to use the PCB to generate the phased square waves at low frequency, and the PLLs to up-converting the signal without worsening the phase shift imposed by the PCB.

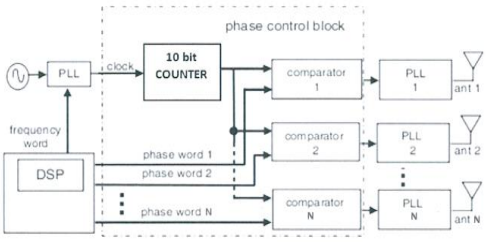


Fig. 2 Phase Shifter Architecture

The system is very similar to the scheme presented in [14], but in this implementation, the accumulator has been replaced with a counter. This lead to an improvement in terms of power consumption, complexity and area occupied.

The output frequency of the PCB is

$$f_{OUT} = \frac{f_{CLK}}{2^{10}} = \frac{2GHz}{2^{10}} = 1.953MHz \quad (1)$$

where f_{CLK} is the system clock frequency, provided by an external reference source, and 10 is the k-bit resolution. Moreover the minimum phase step of PCB is:

$$\Delta\emptyset = \frac{360^\circ}{2^{10}} \cong 0.351^\circ \quad (2)$$

In order to use an M divider in the feedback loop of the PLL instead of a mixer (offset-PLL architecture), without degrading the phase resolution, it is sufficient to bind the choice of the M to the reference frequencies, to the wanted output frequency and the number of bit, k, of the accumulator.

Let $\Delta\varphi_{RES\_IN}$ be the value of the minimum phase shift introduced at the output of the phase control block, which corresponds to a minimum time delay, Δt_{RES}. The relation between $\Delta\varphi_{RES\_IN}$ and Δt_{RES} is expressed in (3)

$$\Delta t_{RES} \rightarrow \Delta\varphi_{RES\_IN} = \frac{\Delta t_{RES}}{T_{IN}} \times 2\pi \quad (3)$$

where T_{IN} is the reference period at the input of the PLL. At the output of the PLL occurs the same time delay, Δt_{RES}, to which corresponds a phase shift, $\Delta\varphi_{RES\_OUT}$, equal to $M \times \Delta\varphi_{RES\_IN}$

$$\Delta t_{RES} \rightarrow \Delta\varphi_{RES\_OUT} = \frac{\Delta t_{RES}}{T_{OUT}} \cdot 2\pi = M \cdot \Delta\varphi_{RES\_IN} \quad (4)$$

where, $T_{IN} = T_{OUT}/M$, is the period at the output of the PLL. Therefore, when a division by a factor M is inserted in the loop, the phase is divided by M considerably decreasing the phase resolution (when an M divider is used, the minimum output phase step becomes $(360/2^k) \times M$ degrees. Actually, considering that

$$\Delta\varphi = \Delta\varphi + m \times 2\pi \quad (5)$$

with m integer and that the relation between Δt_{RES} and k

$$\Delta t_{RES} = \frac{T_{IN}}{2^k} \quad (6)$$

it is possible to choose M in order to have at the output the same resolution achievable at the input

$$\Delta\varphi_{RES\_OUT} = \Delta\varphi_{RES\_IN} + m \times 2\pi \quad (7)$$

The value of M that fulfills (7) is

$$M = m \cdot 2^k + 1 \quad (8)$$

If (8) is respected, it is therefore possible to maintain at the output of the PLLs the same phase resolution imposed at the input by the digital block.

A further important step ahead in using the M divider instead of a mixer in the PLL is possible. The relation stated in (8) allows the use of an M divider but still imposes an important constraint on the choice of M and consequently, places some limitations in dimensioning the reference frequency given a wanted range of output frequencies.

Actually, it is possible to overcome this problem. The basic idea is to use an odd value of M. Making this choice, it is possible to obtain at the output the same number of input phase shifts, that is, the same phase resolution.

As in (3) and considering that $T_{OUT} = T_{IN}/M$, M integer number

$$\Delta\varphi_{RES\_OUT} = M\frac{\Delta t_{RES}}{T_{IN}} \times 2\pi = M\Delta\varphi_{RES\_IN} \quad (9)$$

We could consider that

$$M = m \times 2^k + n \quad (10)$$

with m and n integer number, then

$$\Delta\varphi_{RES\_OUT} = \left(m \times 2^k + n\right)\frac{\Delta t_{RES}}{T_{IN}} = n \times \Delta\varphi_{RES\_IN} \quad (11)$$

where, as just said in different way,

$$n = M \bmod 2^k \quad (12)$$

It's important to underline that it seems to be a coarse output resolution but it's not so. In this case $\Delta\varphi_{RES\_OUT}$ indicates only the output shift obtained related to the input resolution phase shift.

In general if we consider L as the shift position, with $0 < L < 2^k - 1$, we have

$$\Delta\varphi_{OUT} = n \times \Delta\varphi_{IN} = \left(n \times L \times \Delta\varphi_{RES_{IN}}\right)\bmod 2\pi \quad (13)$$

and if we want to know the output position related to the input phase shift position, we have to use (14)

$$L_{OUT} = (L_{IN} \times n) \bmod 2^k \quad (14)$$

where L_{IN} is the input position imposed.

Now it is important to make some fundamental consideration about the choice of the M value and the number of the position obtained.

It's enough to calculate the Maximum Common Divisor (M.C.D.) between the M and 2^k, denoted as $MCD(M, 2^k)$ and the number of the output position N_{OUT} is given by

$$N_{OUT} = \frac{2^k}{MCD(M,2^k)} \quad (15)$$

As a consequence it's clear that if M is an even number, we miss some input position and the most evident are the odd ones; so we have a really coarse phase resolution in relation with the input phase resolution.

On the contrary, if M is an odd number we do not miss any position and maintain the same phase resolution because the M.C.D. between an odd number and a number that is a power of two is always one. Thus in this case, it results $N_{OUT} = 2^k$.

Leaving aside for a moment whether M is an odd or even number, we are not able to control the output phase position yet. At this purpose, we must use a LUT whose dimension is exactly N_{OUT} and populated using the following expression

$$LUT(L) = (L \times n) \bmod 2^k \qquad 0 < L < 2^k - 1 \quad (16)$$

where L is the input phase shift position.

Another more general way is to implement a simple algorithm that has as input the factor used to know the output phase position related to the input phase position, n, the number of bit, k, the desired output resolution related to the input resolution, n', and gives as output the multiplicative number, n'', to use in order to know which input position has to be imposed for obtaining the desired output phase shift position.

The relation that has to be respected is

$$n' = (n'' \times n) \bmod 2^k, \; 0 < n'' < 2^k - 1 \quad (17)$$

and the input position, L, to be imposed is given by the following relation

$$L = (n' \times L') \bmod 2^k \quad 0 < L' < 2^k - 1 \quad (18)$$

where L' represents the output phase position.

In the next chapter there is a detailed description of the architecture for each block of the system.

III. Architecture Overview

An aspect very relevant for this architecture is that it is a frequency independent. In fact as said the PLLs have to up-converter the signal preserving the phase shift imposed by the PCB. So, changing the VCO of PLLs, the frequency changes while maintaining the same phase resolution.

For this reasons the Loop Filters and the VCOs are left off-chip in order to test this topology at different frequency. Thus the PLL design involves the Phase Frequency Detector (PFD), the charge pump and the M-integer Divider.

On contrary the design of digital phase shifter includes one 10-bits counter and three 10-bits comparators, so the system is able to provide the control signals for a phased array composed by three elements.

The Integrated Circuit was realized in 0.35 μm SiGe BiCMOS process provides by AustriaMicroSystem (AMS). This process is cheaper than conventional CMOS processes, but does not exhibit excellent performance for frequencies above approximately 500 MHz. However the design of the elementary cells (inverter , NAND / NOR gates, etc.) in emitter coupled logic, has allowed to realize the system with a maximum clock frequency of 2 GHz.

The core of chip occupies an area of 3.781 x 2.481 mm^2;

the final layout is depicted in Fig. 4 and a picture of the naked chip in Fig. 5.

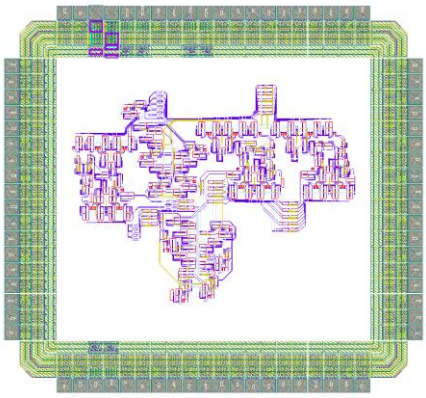


Fig. 4: Phase Shifter – Final Layout

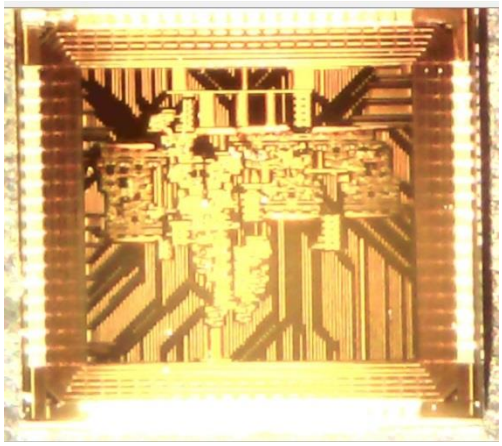


Fig. 5: Phase Shifter – naked chip

The 10-bit counter implements the phase wheel. Each point of this wheel represents one of the possible 2^{10} phase values, coded in a given digital word. Two 5-bit synchronous serial counters constitute the 10-bit counter as in Fig. 6. The first one provides the 5-bit LSB while the second block takes in input the carry of the first module and provides the last 5-bit MSB.

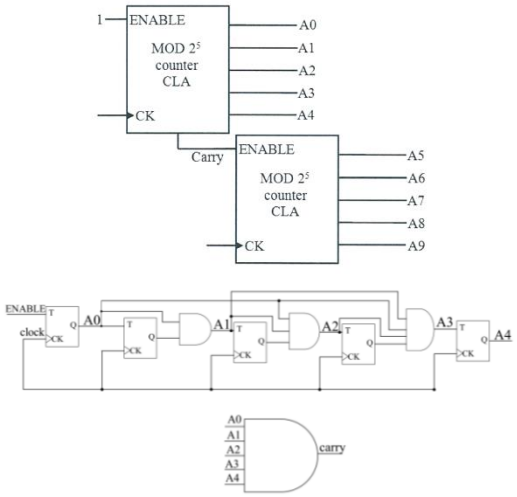
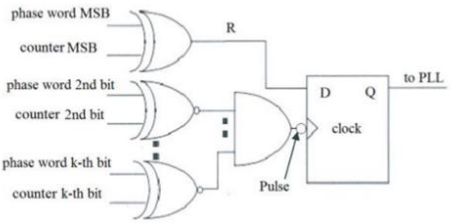


Fig. 6 Simplified 10-bits counter. (a) Parallel/Serial Connection. (b) Simplified schematic of the first 5-bits CLA counter.

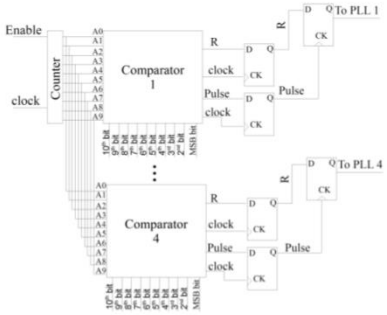
The counter moves around on the phase wheel while the comparator allows selecting the desirable phase value through a digital phase word of k-bit. Therefore, this phase word and the outputs of the counter are the input for this block (Fig. 7a). When the phase word matches bit-to-bit with the output of the counter a pulse is generated. The pulse, in turn, triggers the MSB square wave, whose frequency is equal to:

$$f_{MSB} = \frac{f_{CLK}}{2^k} \tag{19}$$

The main issue of the comparator is the variable delay that depends on the required phase control word. The addition of two D Flip-Flops at the output of each comparator overcomes the problem (Fig. 7.b). Further, these D Flip-Flops eliminate the spurs in the pulse signal generated by the comparator.



(a)



(b)

Fig. 7: 10-bit Comparator (a) Simplified Scheme, (b) Final Scheme.

Fig.8 reports an example of comparator operations. Let us assume for simplicity k=3 and a phase word equal to 001b. The two LSBs of this word are compared with the two LSBs of the counter output by mean of two EX-NOR ports and an AND port. The signal Pulse is high for two clock periods in the MSB period (there are two points in the phase wheel with the LSBs equal to 01b). The MSBs of the phase control word and the counter output are compared by means of an EX-OR port. When these two signals are different, the signal R passes from the low to the high state and vice versa. The following D Flip-Flop outputs R when Pulse is high. In this way, the comparator output is shifted to the desired phase step.

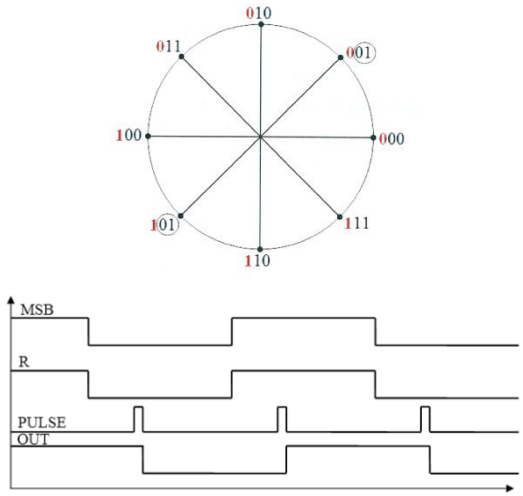


Fig. 8: Principle of comparators operation.

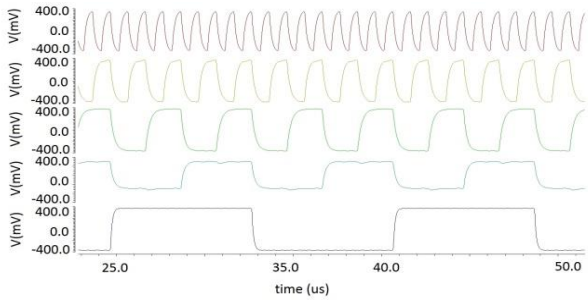
IV. Simulations

The PCB has been simulated by using the layout with parasitic extraction for the chip. The clock frequency has been imposed to 2 GHz so the chip can provides 1024 phased square waves with a minimum phase shift of 0.3515° that correspond to 0.5 ns in time domain. The frequency of these waves is 1.953MHz in accord to equation (1).

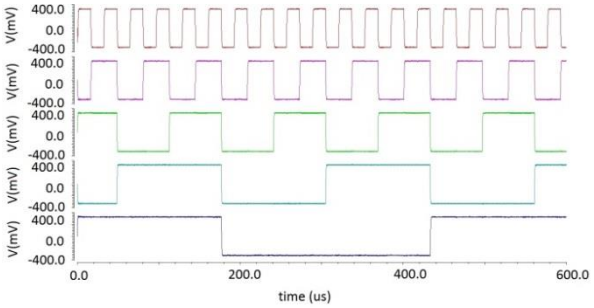
The PCB is designed in Emitter Coupled Logic (ECL), due to the need of speed exceeding the process performances of the CMOS cells.

A top-down approach is utilized, so starting from logic gates (AND, OR, D-Flip Flop…) it was possible to design the counter and comparators.

In Fig. 9a the first 5 bits of counter are reported. Although the output signals are not perfectly squared due to serial architecture chosen and the process utilized, the system was able to generate correctly the phased signals. Indeed the fan-in of the flip-flops limits the number of channels of the structure and suitable level buffers can be introduced in the scheme to solve the problem. Obviously, the number and position of these buffers must be properly chosen, in order to avoid the insertion of unwanted delays. In Fig. 9b the last 5 bits are depicted and it is possible to note the perfectly squared waves being minimal for these bits the fan-in problem.



(a)



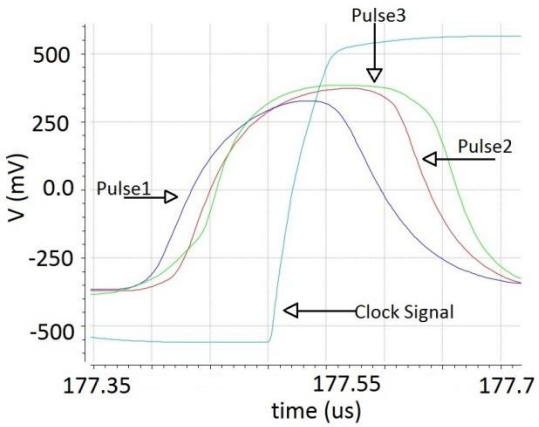
(b)

Fig. 9 10-bit Counter Outputs: (a) LSB bits (b) MSB bits

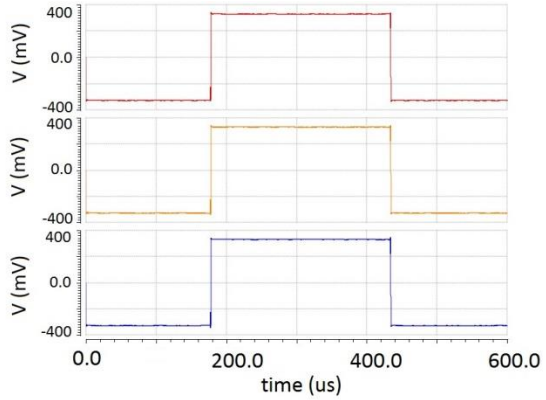
The next test was to verify the synchronism of the channels, that is, when the same phase word is imposed for all the channels. In Fig. 10a phase word equal to 0100000000b has been imposed. Fig 10a shows the output comparator, where blue line is the clock signal used to align the phased square waves depicted in Fig. 10b, where it can be noticed the perfect alignment of the output waves. .

After verifying that the internal propagation delay does not affect the phase shift operation, the first channel has been considered as the reference channel and the 1024 relative phase shifts have been simulated for the other two channels.

A sub-set of the results of these simulations is summarized in Table I, where are listed the MSB period, TMSB, the ideal time delay, TDi, the simulated time delay, TDs, and the phase shift, ΔΦ. The results demonstrate that the PCB can produce phase-shifted square waves with a very high phase-shift precision. Indeed, the worst-case phase error is less than 0.008°.



(a)



(b)

Fig. 10: Output signals of comparators – a) Pulses of phasing . b) Phased Square waves

Finally an example of phased waves is depicted in Fig. 11 where a 90° and 180° phase shift have been imposed for channel two and channel three respectively.

Table I

Phase Word	TMSB [ns]	TDs [ns]	TDi [ns]	Δϕ [deg]
0	512	-	-	0
1	512	0.500	0.500	0.3516
2	512	1	1	0.7031
3	512	1.499	1.500	1.0548
7	512	3.500	3.500	2.4612
17	512	8.490	8.500	5.9772
31	512	15.498	15.500	10.8996
43	512	21.494	21.500	15.1188
401	512	200.500	200.500	140.9916
516	512	258.000	258.000	181.4256
1023	512	511.500	511.500	359.6868

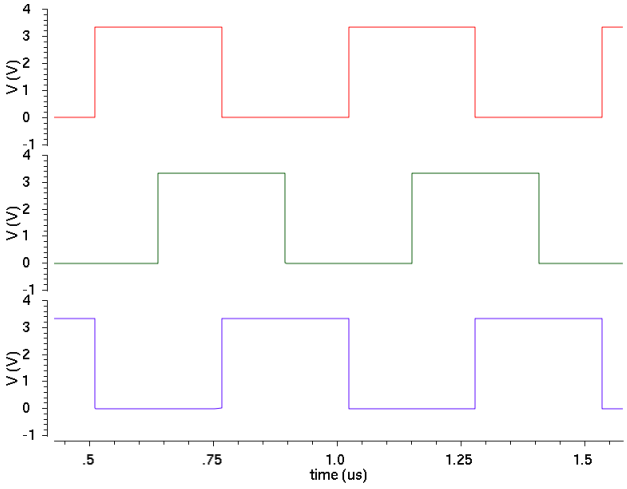


Fig. 11: PCB simulated output squared waves with 90° and 180° phase shift .

Conversely the PLLs were designed in CMOS logic exploiting the AMS standard cell. Indeed the reference frequency is 2 GHz/1024, that is 1.953 MHz. An ECL to CMOS adapter was inserted to translate the voltage levels between the two logics.

The divider was realized with two 11 modulo dividers in series, so the final value is 121. However external modules can be inserted for adapting the scheme to VCO frequency. The overall M divider value is equal to the internal divider multiplied the external divider and must be chosen in accord to [9].

A VCO behavioral block has been inserted into the scheme to verify the complete scheme. The behavioral VCO has allowed verifying the system for different output frequencies. The simulations have demonstrated the independence of system from the output frequency; in fact the output signals present a phase difference equal to the phase difference provided by the Phase Control Block. In Fig. 12 is depicted a zoom of the output signals at 2.4 GHz frequency. For the three channels it was imposed the phase word 0, 1 and 2 respectively.

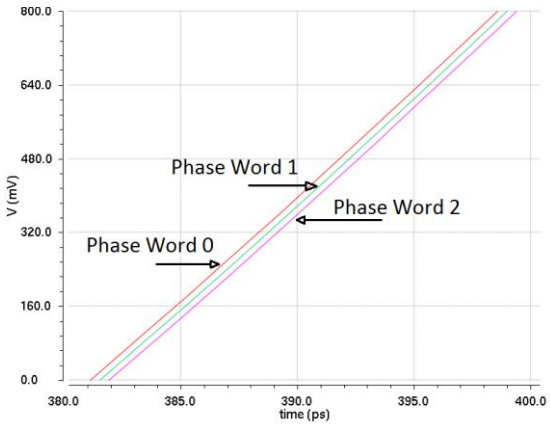


Fig. 12: 2.4 GHz phased output signal

V. Prototype and Measurements

Three different prototypes have been realized. The first one is composed only by the IC fabricated and a microcontroller which imposes the phase words to the three channels. A direct comparison with the simulation results will be presented in the next sub-section.

The second and the third prototypes are composed by the IC fabricated, the microcontroller for the phase words setting and three PLLs with external VCO at different frequencies, in order to test the complete architecture.

A. IC phase shifter and microcontroller

In the first testbench a microcontroller provides the input phase word to the comparators of the phase control block. The external reference imposes the 2GHz clock frequency for the phase control block and it has been used an oscilloscope to

measure the relative phase shifts between the channels.

Also in this case the first step was to verify the channels alignment and then to measure all the relative phase shifts.

In Fig. 13 the same phase word has been imposed for all the channels, while in Fig. 14 the same phase shift imposed as in Fig. 11 is shown.

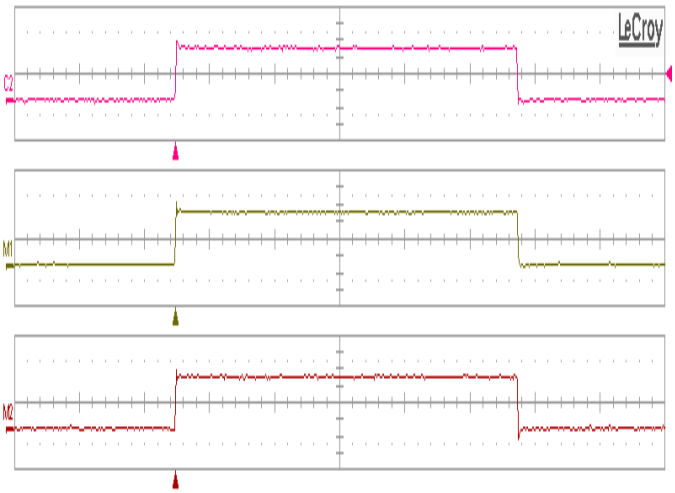


Fig. 13: PCB measured output waveforms with the same phase control word for all the three channel

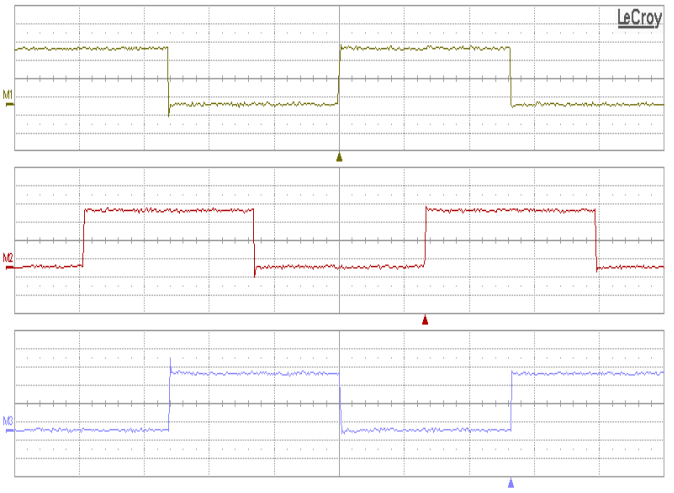


Fig. 14: PCB measured output squared waves with 90° and 180° phase shift.

In general for the relative phase shift measurements, the first channel has been considered as the reference channel and the other two channels as the phased ones. In Fig. 15 there are represented the measured characteristics when a phase word equal to 0000000000b has been imposed for the channel 0.

It can be noticed the almost perfect overlap of the measured characteristics with the ideal one.

In Fig. 16 the phase error of the channel two and channel three is shown. The maximum phase error is about 0.1° for both the channels; the rms error is about 0.0585° for the second channel and 0.0588° for the third channel.

The measures were been repeated imposing the phase word to the reference channel equal to 1111100000b and the results are shown in Fig. 10. Also in this case the maximum error phase shift is about 0.1° and the rms error is about 0.0581° for the second channel and 0.0592 for the third channel.

These tests confirm perfectly the simulations results.

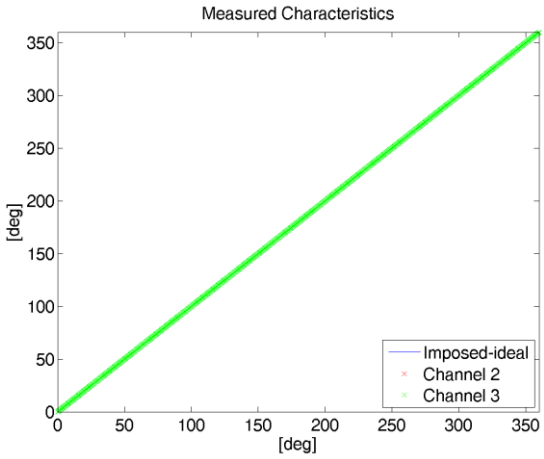
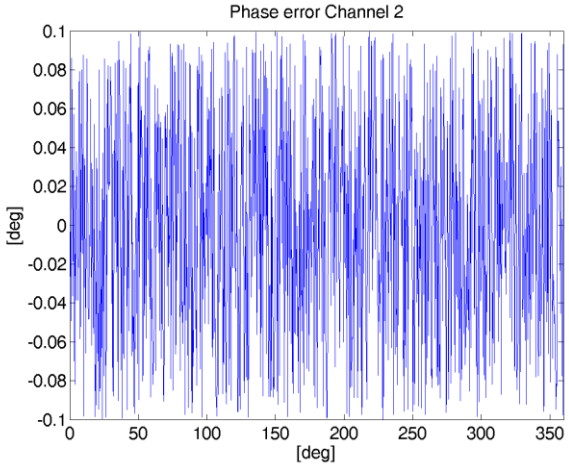
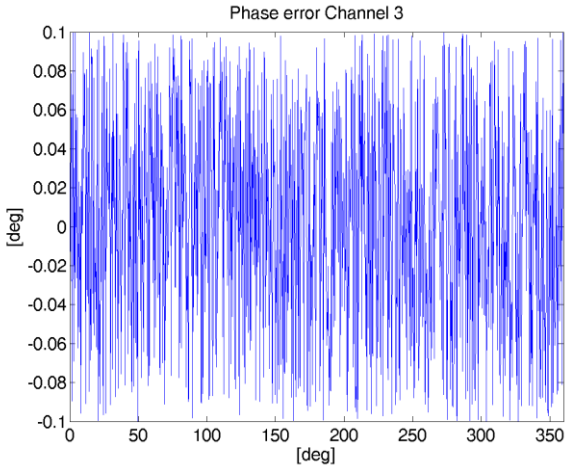


Fig. 15: PCB measured output characteristic.

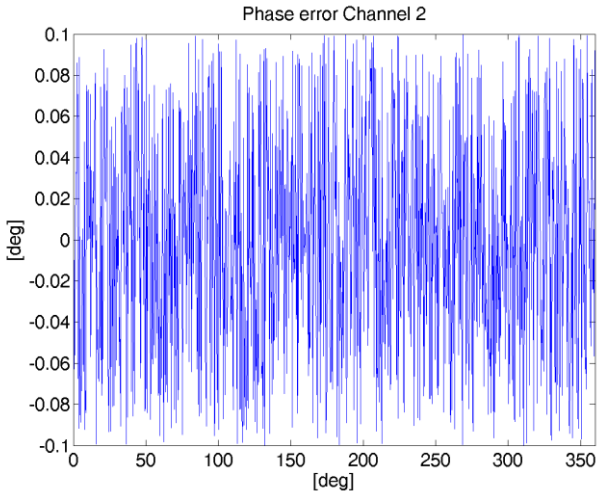


(a)

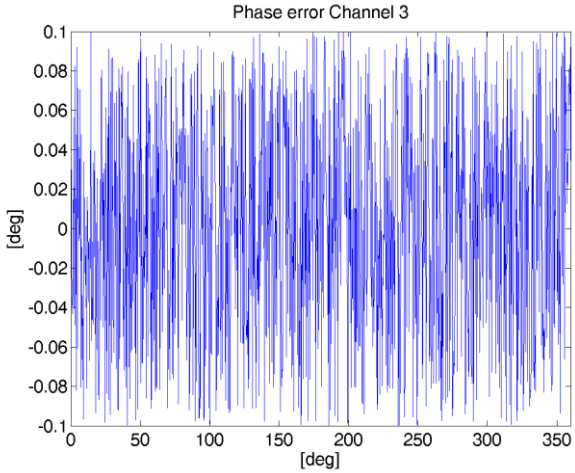


(b)

Fig. 16: PCB phase shift error with phase control word equal to 0000000000b for the channel one. a) Channel two; b) channel three



(a)



(b)

Fig. 17: PCB phase shift error with phase control word equal to 1111100000b for the channel one. a) Channel two; b) channel three

B. *IC phase shifter, microcontroller, PLL and VCO at 2.45GH*

In the second testbench, PLLs synthesize the desired output frequency without deteriorating the achievable good phase resolution. The VCO output frequency was set to 2.45GHz.

For uniformity the same tests previously made are reported. In Fig. 18 there are the output sinewave when the same phase word is imposed for all the three channels.

In Fig. 19 the same phase shifts imposed as in Fig. 5 are shown.

All the 1024 phase shifts have been measured for the center frequency.

As shown in Fig. 20 it can be noticed that the maximum phase error is increased and it is due to the phase noise introduced by the PLL and VCO. The rms phase error is equal to 0.0854° for the channel two and 0.0866° for the channel three.

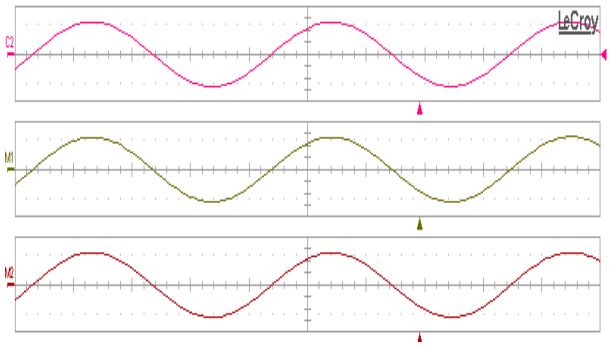


Fig. 18: VCO measured output waveforms with the same phase control word for all the three channels

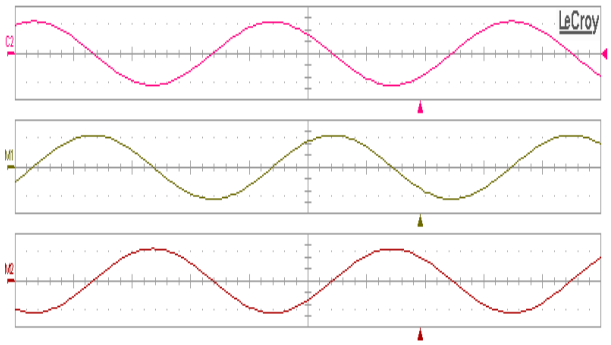
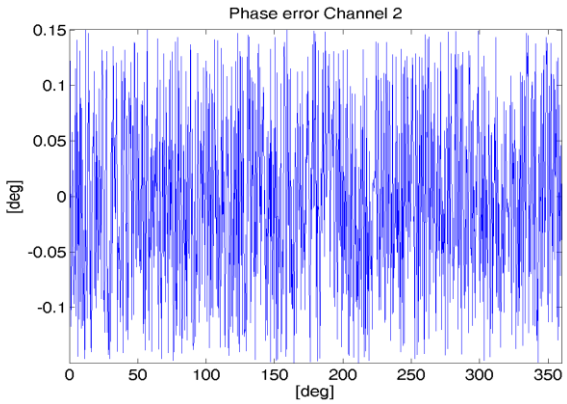
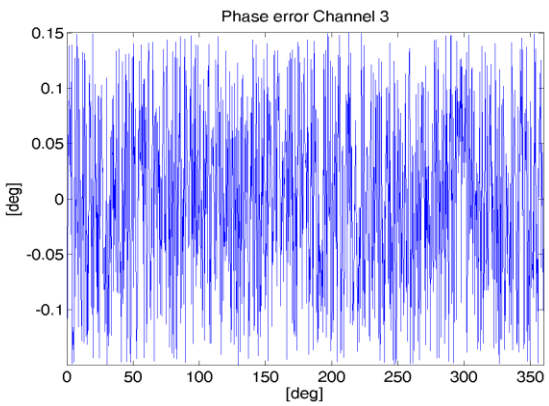


Fig. 19: VCO measured output waveforms with 90° and 180° phase shift



(a)



(b)

Fig. 20: VCO phase shift error with phase control word equal to 0000000000b for the channel one. a) Channel two; b) channel three

C. *IC phase shifter, microcontroller, PLL and VCO at 3.8 GHz*

In the last testbench the VCO with an output frequency equal to 3.8GHz has been chosen.

The same tests previously made are reported. In Fig. 21 there are the output sinewave when the same phase word is imposed for all the three channels.

In Fig. 22 the same phase shifts imposed as in Fig. 5 are shown.

Finally, the Fig. 23 shows that for the center frequency the maximum phase error is decreased compared to the 2.45 GHz prototype and increased compared to the first prototype without the PLL and VCO; it is due to the different phase noise introduced by VCO itself. The rms phase error is equal to 0.0637° for the channel two and 0.0694° for the channel three.

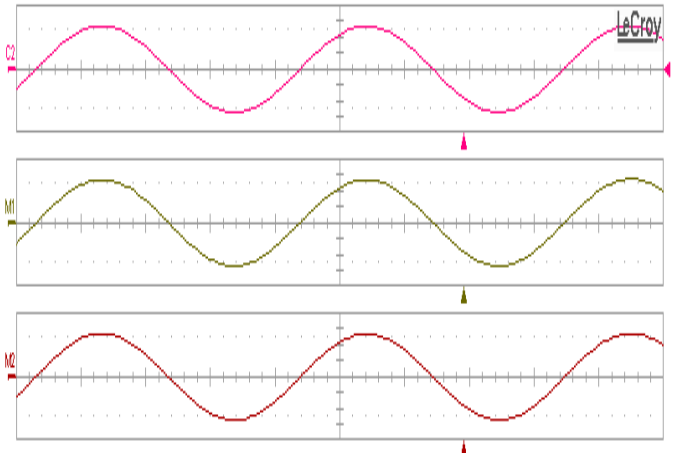


Fig. 21: VCO measured output waveforms with the same phase control word for all the three channels

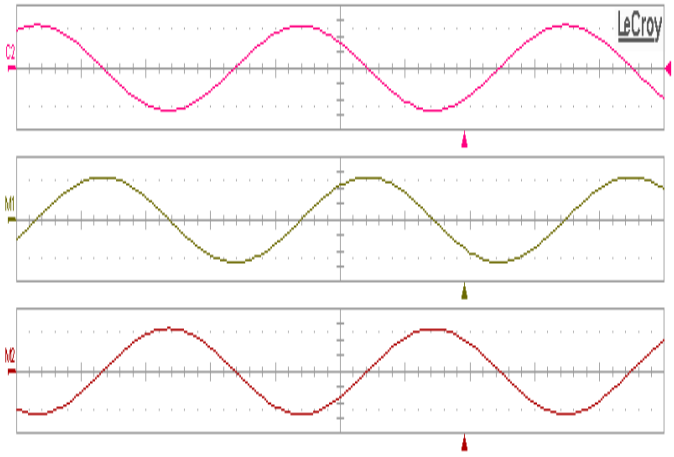
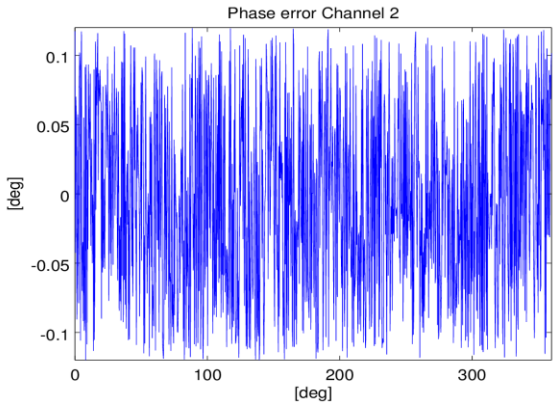
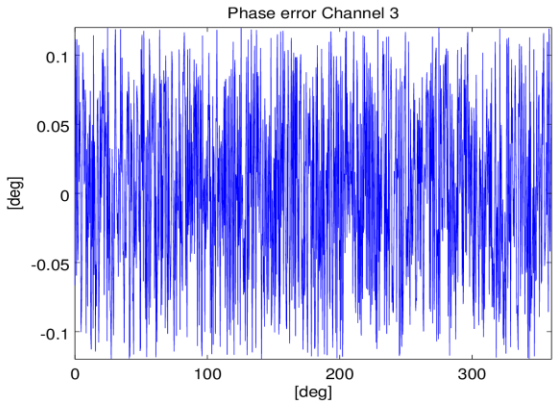


Fig. 22: VCO measured output waveforms with 90° and 180° phase shift

It demonstrates the validity of the proposed approach.



(a)



(b)

Fig. 23: VCO phase shift error with phase control word equal to 0000000000b for the channel one. a) Channel two; b) channel three

VI. Conclusion

In this paper a high precision phase shifter has been presented. The system was realized in 0.35 µm SiGe BiCMOS process and allows generating phased square-waves with a minimum step of 0.3515°. The great flexibility of the proposed architecture is given by its frequency independency and scalability; in fact it is simply demanded at the use of suitable PLLs and VCOs while the phase resolution is demanded to a very simple digital circuit.

The PCB output signals have a maximum phase error of about 0.1° and an rms error equal to 0.0592°. A slight deterioration has been measured at 2.45GHz and 3.8GHz where the overall phase error is due to the VCO phase noise.

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