# Novel Cascaded H-Bridge Multilevel Inverter with Bi-Directional Switches

D. Baimel[1], S. Tapuchi[1], N. Baimel[2]

*Abstract* - The paper presents an analysis of a novel cascaded multilevel inverter, which consists of two cascaded bridges per phase. The upper bridge produces 5-level voltage and consists of only two bi-directional and four standard IGBT switches in each 5-level H-bridge. The lower bridge is standard 3-level H-bridge. The inverter is controlled by Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) PWM methods. The significant advantages of the proposed inverter are simpler control and lower number of components such as switches, diodes and capacitors than in the standard multilevel topologies. Extensive simulation results validate the practicability of the proposed inverter. The proposed topology can be extended to any desired number of levels by cascading additional bridges.

Keywords - Multilevel, inverter, PWM.

## I. INTRODUCTION

The multi-level inverters are suitable for high voltages and high power applications. The output voltage wave is built of several staircases that mitigate the voltage gradient dv/dt stresses on electric machine or transformer windings connected to the multi-level inverters. Furthemore, the output voltage wave has a much lower THD factor than that of their two-level counterparts.

There are several standard configurations for multi-level inverters, [1-4]. One of the configurations is the Neutral Point Clamped (NPC) multi-level inverter [5-8]. The DC voltages are obtained by charging several capacitors from only one DC voltage source. The main advantage is the need for only one DC voltage source. The main disadvantage is the need to control and regulate the capacitor's charging/discharging processes to ensure that their voltage levels remain constant. Another type of multi-level inverters is the Cascaded H-Bridge configuration [9-11]. In this topology, each inverter phase has several H-bridges connected in series, and each H-bridge is supplied by its own DC voltage source. The main advantage is stable voltage levels on the H-bridge switches. Their main disadvantage is the need for several DC voltage sources. Additional standard configuration is Flying Capacitor (FC) multi-level inverter [12]. The main advantage of this topology is the necessity for only one DC voltage source..

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The authors are with: 1.Shamoon College of Engineering, Israel and 2. Sapir Academic College, Hof Ashkelon, Israel

The paper presents extensive simulation results obtained on the proposed 9-level inverter operated by PD, POD and APOD PWM methods [13-16]. Section II presents the proposed The main disadvantage is the requirement to control and regulate the capacitor charging and discharging processes to ensure that their voltage levels remain quasi constant inverter. Section III shows simulation results and their discussion. Section IV presents the conclusions of the paper.

## II. THE PROPOSED INVERTER

The proposed 9-level inverter consists of two series cascaded 5-level and 3-level H-bridges on each inverter phase (see Fig. 1).

The first 5-level H-bridge is fed by VDC voltage source. Additionally to the required five switching states, this bridge has two additional redundancy switching states which simplify the neutral point voltage balancing process. The switching states of the proposed inverter are shown in Table I. The switching states of the upper 5-level H-bridge are the states 1-7. It can be seen that the switching states (4, 5), (6, 7), (8, 9) and (10,11) are redundant. By using these redundant switching states, the switching algorithm exchanges the neutral point capacitors C1 and C2 connection to the load while keeping the same output voltage. By exchanging the capacitors, the switching algorithm balances the neutral point voltage in the 5-level bridge. Without voltage balancing, one of the capacitors would charge to the full VDC voltage and the other one would discharge to the zero voltage [17-20]. The 5-level H-bridge cell has only six IGBT switches and two capacitors when the standard NPC H-bridge cell has eight IGBT switches, two capacitors and six diodes. As a result, the proposed topology has smaller size and weight, and lower price. The second bridge is standard 3-level H-bridge fed by VDC voltage source. This H-bridge provides additional three voltage levels: VDC, - VDC and 0. The cascading of these two H-bridges provides nine voltage levels: 0, VDC/2, -VDC/2, VDC, - VDC, 1.5VDC, - 1.5VDC, 2 VDC, -2 VDC. There are nine possible switching states in this inverter.

The proposed topology can be compared to the standard multilevel topologies including Flying Capacitor (FC), Neutral Point Clamped (NPC) and Cascaded H-BRIDGE topologies (see Fig. 2). The comparison is based on the number of components of each topology and is shown in Table II. It can be seen that the proposed topology has less components than the standard topologies. This results in simple inverter construction, simple production, and maintenance and fault management.

Additional advantages of this topology are the modularity of the H-bridge cells and the relatively low number of the DC voltage sources (only two DC voltage sources per phase for nine voltage levels).

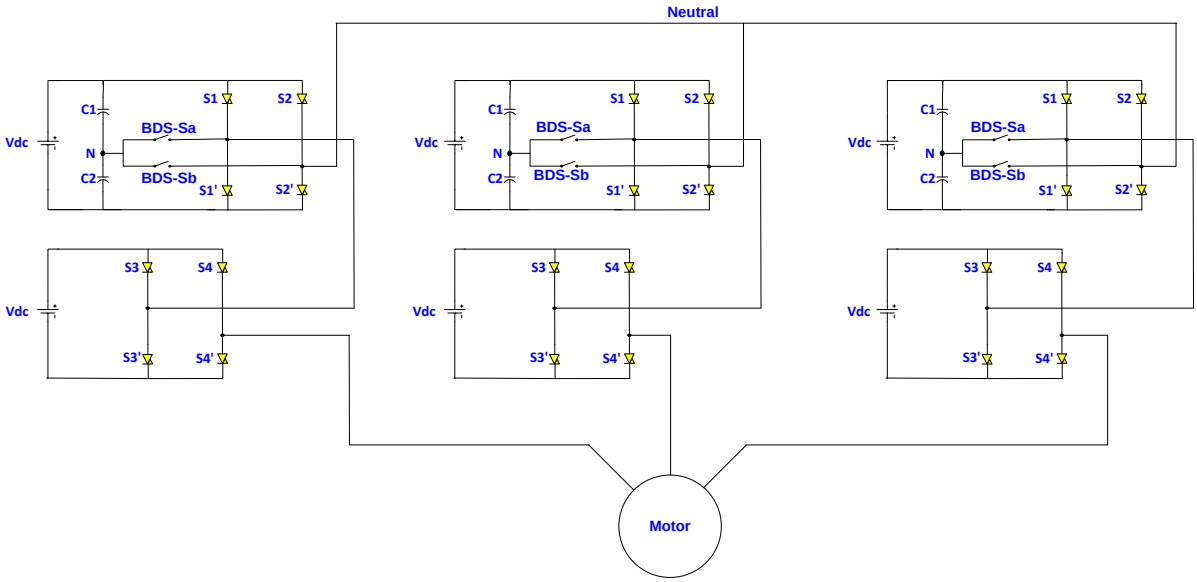
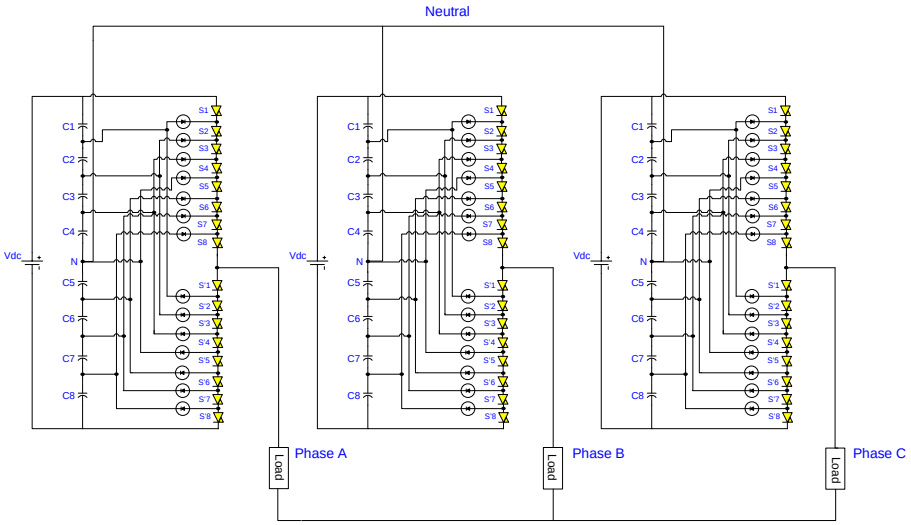



Fig. 1. The proposed 9-level inverter.

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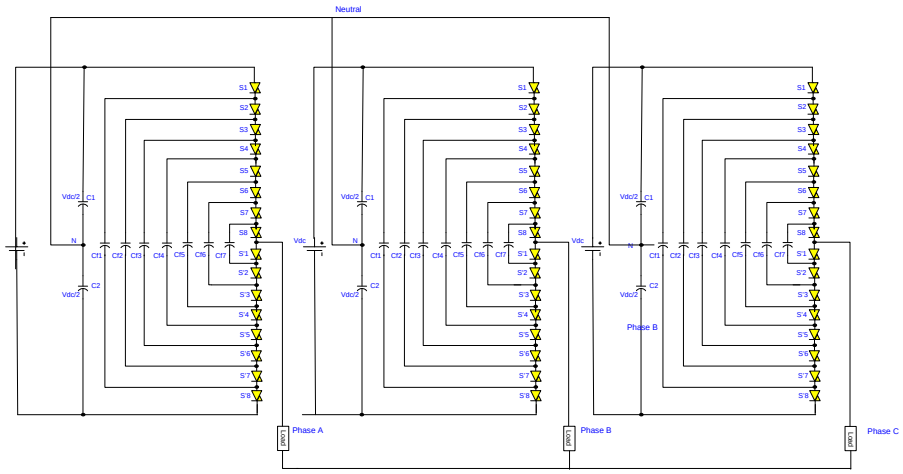


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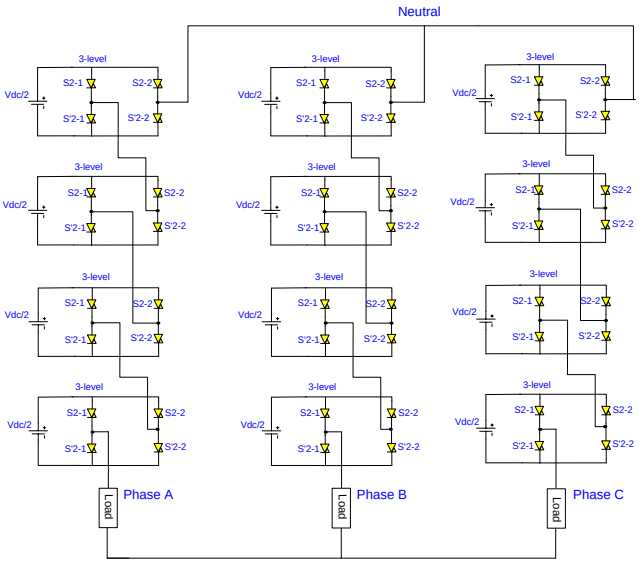


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Fig. 2. Standard multilevel inverter topologies. (a) Standard NPC 9-level inverter; (b) Standard FC 9-level inverter; a) Standard Cascaded H-bridge 9-level inverter.

TABLE I. THE SWITCHING STATES OF THE PROPOSED 9-LEVEL INVERTER.

| State | Capacitor connected to load | Switch/ voltage | Sa | Sb | S1 | S'1 | S2 | S'2 | S3 | S4 | S3' | S4' |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | None | 0 | OFF | OFF | ON | OFF | ON | OFF | ON | ON | OFF | OFF |
| 2 | None | VDC | OFF | OFF | ON | OFF | OFF | ON | ON | ON | OFF | OFF |
| 3 | None | -VDC | OFF | OFF | OFF | ON | ON | OFF | ON | ON | OFF | OFF |
| 4 | C1 | VDC/2 | OFF | ON | ON | OFF | OFF | OFF | ON | ON | OFF | OFF |
| 5 | C2 | VDC/2 | ON | OFF | OFF | OFF | OFF | ON | ON | ON | OFF | OFF |
| 6 | C1 | -VDC/2 | ON | OFF | OFF | OFF | ON | OFF | ON | ON | OFF | OFF |
| 7 | C2 | -VDC/2 | OFF | ON | OFF | ON | OFF | OFF | ON | ON | OFF | OFF |
| 8 | C1 | 1.5VDC | OFF | ON | ON | OFF | OFF | OFF | ON | OFF | OFF | ON |
| 9 | C2 | 1.5VDC | ON | OFF | OFF | OFF | OFF | ON | ON | OFF | OFF | ON |
| 10 | C1 | -1.5VDC | ON | OFF | OFF | OFF | ON | OFF | OFF | ON | ON | OFF |
| 11 | C2 | -1.5VDC | OFF | ON | OFF | ON | OFF | OFF | OFF | ON | ON | OFF |
| 12 | None | 2VDC | OFF | OFF | ON | OFF | OFF | ON | ON | OFF | OFF | ON |
| 13 | None | -2VDC | OFF | OFF | OFF | ON | ON | OFF | OFF | ON | ON | OFF |

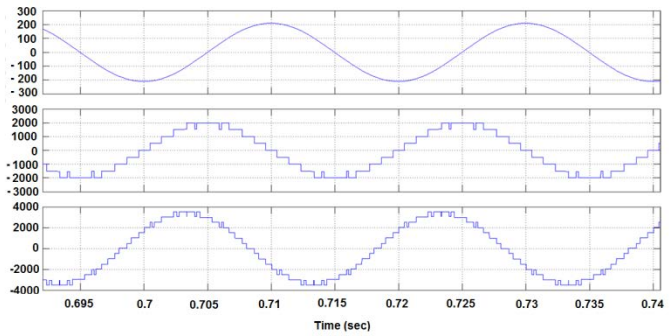
TABLE II. THE COMPARISON BETWEEN THE PROPOSED, STANDARD FC, STANDARD NPC AND CASCADED TOPOLOGIES FOR DIFFERENT NUMBER OF LEVELS.

| Number of voltage levels/ topology | Components | 9-level | 13-level | n-level (n is odd number) |
|---|---|---|---|---|
| Proposed hybrid inverter | Diodes | 0 | 0 | 0 |
| | Switches | 30 | 42 | n*3+3 |
| | Capacitors | 6 | 6 | 6 |
| | dc voltage sources | 6 | 9 | (n/2-0.5)*1.5 |
| Standard FC inverter | Diodes | 0 | 0 | 0 |
| | Switches | 48 | 72 | (N-1)*2*3 |
| | Capacitors | 27 | 39 | N*3 |
| | dc voltage sources | 3 | 3 | 3 |
| Standard NPC inverter | Diodes | 42 | 66 | (N-2)*2*3 |
| | Switches | 48 | 72 | (N-1)*2*3 |
| | Capacitors | 24 | 36 | (N-1)*3 |
| | dc voltage sources | 3 | 3 | 3 |
| Standard cascaded H-bridge inverter | Diodes | 0 | 0 | 0 |
| | Switches | 48 | 72 | (n-1)*2*3 |
| | Capacitors | 0 | 0 | 0 |
| | dc voltage sources | 12 | 18 | (n/2-0.5)*3 |

## III. SIMULATION RESULTS

The purpose of the simulations is to analyze the proposed inverter. The simulations were performed in Simulink (Matlab) program.

The simulation parameters are: VDC=1000V, DC link capacitors C1=C2=10mF; the load of the inverter per phase is R = 0.04 Ω, L=0.03H. Fig. 3 shows simulation results for the PD PWM method, current and voltage waves and their spectra, while the modulation frequency is 50 Hz, the carrier frequency 1050 Hz and the modulation index is 1.

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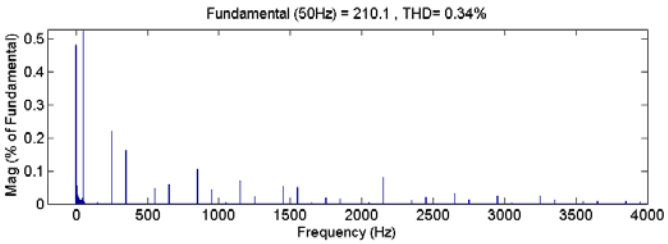


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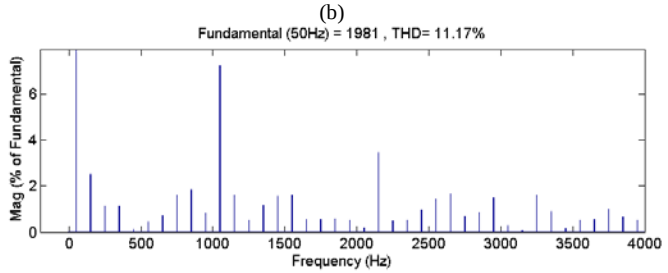


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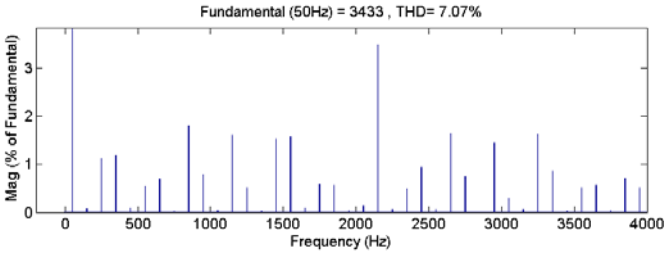
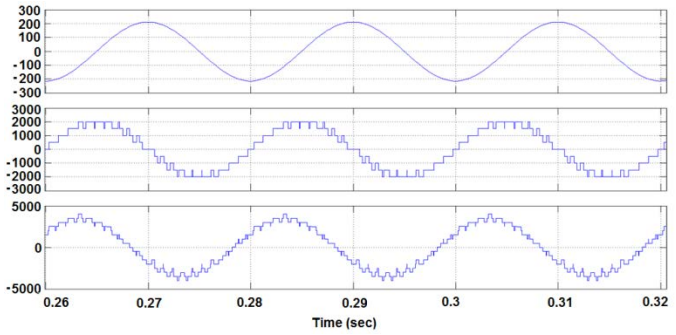



(d)

Fig. 3. Simulation results, current and voltage waves and their spectra, while the modulation frequency is 50 Hz, the carrier frequency 1050 Hz, there are nine voltage levels in the output phase voltage, modulation index is 1, PD PWM method: (a) phase "A" current, phase "A" voltage, and line "AB" voltage; (b) spectrum of the phase current; (c) spectrum of the phase voltage; (d) spectrum of the line voltage.

Fig. 4 shows simulation results for POD PWM method, current and voltage waves and their spectra, while the modulation frequency is 50 Hz, the carrier frequency 1050 Hz and the modulation index is 1.

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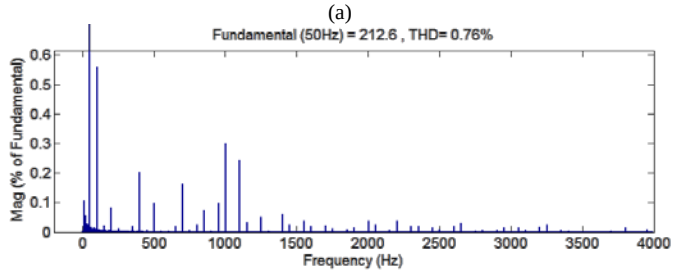


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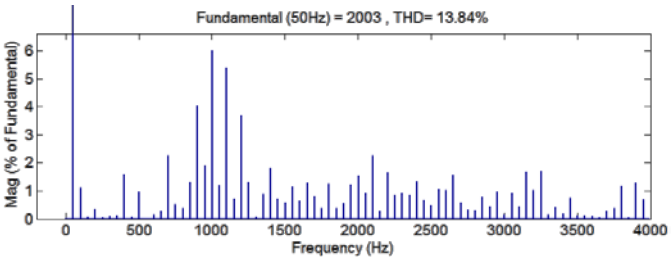


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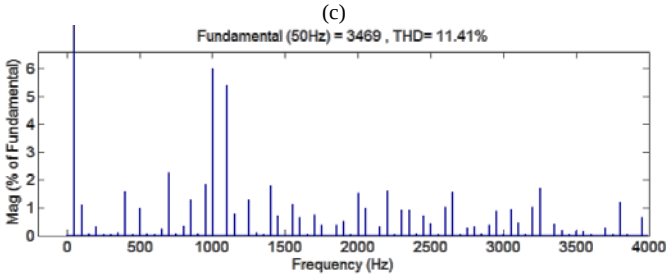


(d)

Fig. 4. Simulation results, current and voltage waves and their spectra, while the modulation frequency is 50 Hz, the carrier frequency 1050 Hz, there are nine voltage levels in the output phase voltage, modulation index is 1, POD PWM method: (a) phase "A" current, phase "A" voltage, and line "AB" voltage; (b) spectrum of the phase current; (c) spectrum of the phase voltage; (d) spectrum of the line voltage.

The proposed inverter was also operated by APOD PWM method. The obtained simulation results for PD, POD and APOD PWM methods, with different modulation and carrier frequencies are shown in Table III.

TABLE III. SIMULATION RESULTS FOR DIFFERENT MODULATION AND CARRIER FREQUENCIES

| Modulation frequency/ PWM method | Carrier frequency (Hz) | Phase current THD (%) | Phase voltage THD (%) | Line voltage THD (%) |
|---|---|---|---|---|
| 50 (PD PWM) | 1050 | 0.34 | 11.17 | 7 |
| 40 (PD PWM) | 840 | 0.37 | 12.58 | 7.94 |
| 30 (PD PWM) | 630 | 0.38 | 11.1 | 7.3 |
| 50 (POD PWM) | 1050 | 0.76 | 13.84 | 11.41 |
| 40 (POD PWM) | 840 | 0.75 | 13.27 | 10.58 |
| 30 (POD PWM) | 630 | 0.75 | 13.5 | 11.2 |
| 50 (APOD PWM) | 1050 | 0.71 | 12.65 | 12 |
| 40 (APOD PWM) | 840 | 0.7 | 12.4 | 11.9 |
| 30 (APOD PWM) | 630 | 0.7 | 12.2 | 11.7 |

The simulation results show that for all simulated carrier frequencies and PWM methods, the obtained phase current THD is lower than 5% as required in IEEE 519 standard. It can be seen that better THD results of phase current and phase voltage are obtained by PD PWM method. The THDs of the currents and voltages in POD and APOD methods are almost similar.

At can be also seen that the phase voltage THD is almost not influenced by the PWM method.

Table III also shows that the THD of the phase currents and phase and line voltages remain almost unchanged (only small variations) during the changes in the modulation and carrier frequencies, as long as the same PWM method is used and as long as the ratio between the modulation and carrier frequencies is kept constant. For example, in Table III the ratio between the modulation frequency and the carrier frequency is 21: between 50 Hz and 1050Hz, between 40Hz and 840 Hz, between 30 Hz and 630Hz.

The obtained phase current is almost sinusoidal and has significantly lower THD than the phase and line voltages due to the inductive load that acts like a filter.

The proposed inverter can be also operated by SVM [21-22] and over-modulation PWM methods [23-25 ].

## IV. CONCLUSIONS

The paper presents a new topology of multilevel cascaded H-bridge inverter. The proposed inverter has two H-bridges per phase while the first H-bridge provides five voltage levels and the second provides three voltage levels. This topology can be extended to any higher number of voltage levels by adding additional three-level H-bridges.

In order to analyze the inverter, it was operated by a PD, POD and APOD carrier-based PWM methods. It can be seen that the obtained phase current THD for all simulated PWM methods and for all cases was lower than 5% as required in IEEE 519 standard. Also better THD results are obtained during the implementation of the PD PWM method.

Extensive simulation results show that the proposed multilevel inverter is practicable and works properly.

The advantages of the proposed inverter are reduced number of components that result in lower size, weight and price. Furthermore, the cascaded H-bridges are modular and can be replaced in case of faults.

In general, the optimal point of operation of the inverter depends on different parameters such as the modulation index and modulation frequency, THD of the output currents and voltages, switching power losses, common mode voltage, and inverter cost and reliability. These parameters would strongly depend on the specific application the inverter would be intended for.

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