Physical phenomena captured in a mathematical model of p-NOI and NOI transistors

Cristian Ravariu, Dan Eduard Mihaiescu

***Abstract*—**The scope of this paper is to establish a mathematical model of the tunneling current between drain and source thru a Nothing On Insulator – NOI transistor and its variants. Using the first, second and third order derivatives of the analytical model, aimed by the Non-linear Electrical Conduction Theorem (NECT), new rigorously extraction methods of the threshold drain voltage is presented. Finally, some validations of the exponential analytical model by simulations are presented. Two distinct work regimes for the NOI and p-NOI devices are established: strong and weak tunneling.

***Keywords*—**Electron devices; Mathematical model; Non linear conduction; Simulations; Tunneling.

I. INTRODUCTION

THE vacuum electronic devices are usually operated at high voltages, more than 40V to control a non-linear current of few micro- or nano- Amperes [1]. The paid price is an un-null gate current that is specific to a triode, [1-4].

The Nothing On Insulator (NOI) devices are expected to provide an almost null gate current, due to the bottom oxide isolation, besides to an exponential source-drain characteristics, as previous work reveals, [5-8]. Working with electrons in vacuum, the NOI device takes the advantage to avoid the recombination processes from pin or MOS. So, it is expected to get a fast switching property due to strong non-linear current-voltage dependence. From this point, some applications were previously presented, [6]. A related variant is the planar-NOI or p-NOI, based on tunneling thru ultra thin oxide regions instead vacuum, [9, 10]. Both vacuum NOI and p-NOI possess strong non-linear drain-source conduction by the Fowler-Nordheim (FNORD) tunneling law, [10]. The exponential law of the Fowler-Nordheim model was always used in simulations, activating the FNORD parameter inside the Atlas models. But an analytical model is missing or is drafted, [11-13]. Therefore, the aim if this paper is to develop a mathematical model of the drain characteristics, ID-VD, which must demonstrate this beneficial strong non-linear conduction. In this scope, the final analytical model has to obey to the Non-linear Electrical Conduction Theorem (NECT), [14]. Using NECT mathematical tool, some knee points of the ID-VD characteristics are rigorously defined in this paper.

II. PHYSICAL PHENOMENA

A. *The NOI and p-NOI structures*

A NOI predecessor was a device with a thinner p-film connecting both Si, n^+ films, [7]. This prior device possesses two conduction mechanisms: (i) by electrons confinement thru thin p-type film and by a tunneling thru "Nothing" region, [8]. Then the p-type film was thinned down up to one atomic layer and extremely up to "nothing" region between Si, n^+ films. This "Nothing" zone with extremely low size becomes the main device body, fig.1.a. It is a nano-space of 1 - 10nm distance, d, which allows a single conduction way from source to drain - by the vacuum tunneling.

A NOI completely differs from a SOI-MOSFET or SON [15] with inversion channels thru a solid-state material and is closer to a Tunnel-FET (TFET), [16]. The TFET conduction is based on the Band-to-band tunneling thru the successive regions Si-p / Si-i / Si-n of a pin diode on insulator, [17]. The NOI tunneling is based on the Fowler-Nordheim (FNORD) tunneling thru a triangular potential barrier created by a nano-space into an insulator, as tunneling thru the typical succession Si-n^+ / Nothing / Si-n^+ on insulator, [18].

The horizontal implementation for a NOI transistor with vacuum isn't still possible at the nowadays technological resolution. Therefore we propose here the vertical p-NOI variant. If Oxide (O) replaces Vacuum (V) and the metal of drain replace the semiconductor drain island, a mOn succession (metal/Oxide/n-Si) or p-NOI device results, based on the oxide tunneling on vertical direction. The oxide insulator can be deposited in Si-technology as ultra-thin film of 2...10nm oxide. Therefore, the p-NOI variant is a vertical

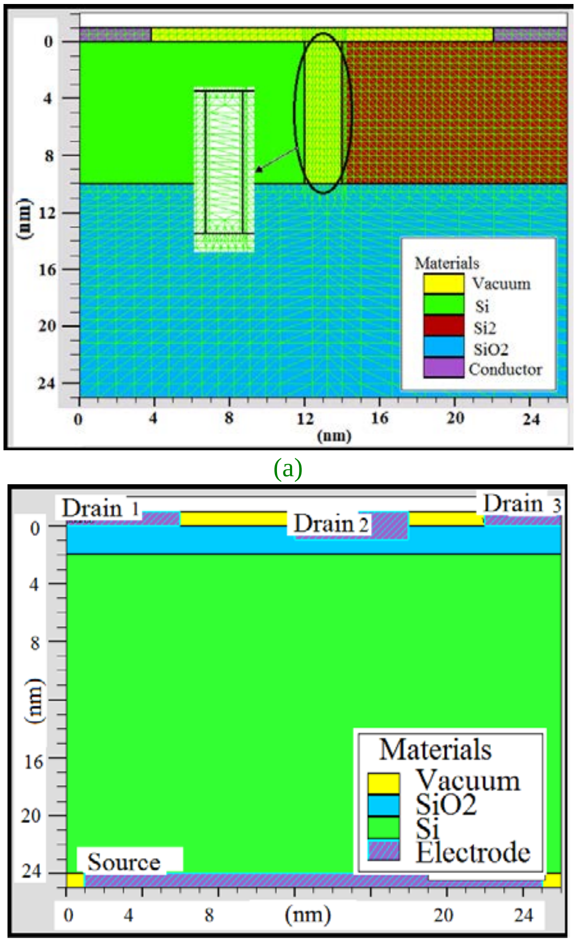
---

This work was partially supported by a grant of the Romanian National Authority for Scientific Research and Innovation, CNCS/CCCDI UEFISCDI, project number PN-III-P2-2.1-PED-2016-0427 as 205PED /2017 (DEMOTUN), partially supported by a grant of CNCS - UEFISCDI, project number PN-III-P4-ID-PCE-2016-0480 as project 4/2017 (TFTNANOEL) and partially funded by the Research Projects PN-III-P2-2.1-PTE-2016-0160, 49-PTE 2016 (PROZECHIMED).

C. Ravariu is with the Electronic Devices Circuits and Architectures Department, Polytechnic University of Bucharest, Faculty of Electronics, Bucharest, 060042, Romania, Splaiul Independentei 313, phone: +40214024840; fax: +40214024886; e-mail: cristian.ravariu@upb.ro.

D.E. Mihaiescu is with the Organic Chemistry Department, Polytechnic University of Bucharest, Faculty of Applied Chemistry, Bucharest, 060042, Romania (e-mail: dan.mihaiescu@upb.ro).

simplified NOI variant, with the advantage of simpler Si integration and suitable for the same mathematical model.



(a)

(b)

Fig.1. The NOI nanostructure with vacuum; (b) the planar vertical variant of p-NOI with oxide.

The validation of the FNORD model is suggested by the simulated energetic diagram from fig. 2 for NOI with vacuum or p-NOI with oxide and the same size. For V_{DS} higher than 3V the source-drain energetic barrier gets a triangular shape both for NOI and p-NOI variants. The barrier width is $x_c/10$, where x_c is the cavity width, at V_{DS}=7V, allowing a strong Fowler-Nordheim tunneling.

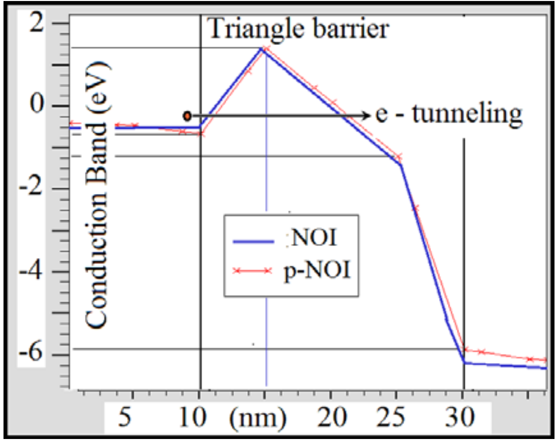


Fig. 2. The conduction band energy at V_S=0V, V_D=4V and V_G=-4V for NOI and p-NOI structures.

B. Any insulator cavity and p-NOI variant

Obviously, any insulator instead vacuum allows the same FNORD tunneling, keeping similar sizes. A recent analysis proved the FNORD tunneling thru the NOI with oxide that means the succession: Si-n$^+$ / Oxide / Si-n$^+$, as NOI(a) variant with all similar features. This empowers us to extend the theory to a related variant - the planar NOI, with the succession: Metal / Oxide / Si-n$^+$, as p-NOI(a) variant. This is in agreement with the well-known theory of the MOSFET gate tunneling by FNORD mechanism.

In conclusion, the next developed models obey to the FNORD law, as the main conduction phenomenon in NOI devices.

III. MATHEMATICAL MODEL

A. Fundamental model - FNORD

For small vacuum or oxide width x_c, the source-drain tunneling probability is described by the Fowler-Nordheim model, [11]:

$$P_t \approx exp\left[-\frac{4\sqrt{2m_n^*}\cdot\chi_S^{3/2}\cdot d}{3q\hbar V_{DS}}\right] \qquad (1)$$

where m_n^* is the electron effective mass, χ_S is the semiconductor affinity for electrons in respect with the vacuum, $\hbar=h/2\pi$ (h is the Planck's constant), q is the elementary electric charge.

Figure 3 presents the tunneling probability versus the V_{DS} voltage for different x_c values: 2, 3, 4, 7nm. For d=7nm, the probability is negligible under 30V, because the triangle barrier approximation is no longer true, until V_{DS} voltage reaches 30V.

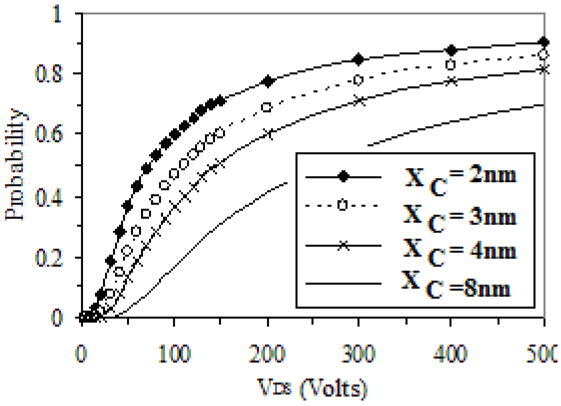


Fig. 3. Probability of tunneling thru a nano-cavity of x_c.

Considering a potential barrier from semiconductor to vacuum with a triangle shape for $V_S=V_G=0$ and $V_D>0$, and assuming the applied electric field in vacuum, $E=-gradV \approx V_{DS}/x_C$, the tunnel current density for electrons, J_{FN}, is given by, [11, 19]:

$$J_{FN1}=F.AE\cdot E^2\exp\left(-\frac{F.BE}{E}\right) \tag{2}$$

In Atlas, this model is activated by FNORD parameter. The F.AE, F.BE expressions are depending on the Semiconductor-Insulator potential barrier height, φ_S:

$$F.AE=A\cdot\varphi_S^{-1} \text{ and } F.BE=B\cdot\varphi_S^{3/2} \tag{3}$$

where A and respectively B are the first and second Fowler-Nordheim constants:

$$A=\frac{q^3}{8\pi h}=1.54\cdot 10^{-6}AV^{-2}eV \tag{4}$$

$$B=\frac{4\cdot\sqrt{2m_n^*}}{3q\hbar}=6.83\cdot 10^{+7}cm^{-1}V(eV)^{-3/2} \tag{5}$$

where q, h, ħ, π are usual constants and m_n^* is the electron effective mass in semiconductor.

After previous considerations, the tunneling current It, can be directly expressed versus the drain-source voltage:

$$I_t=\alpha\cdot\frac{V_{DS}^2}{d}\cdot exp\left(-\frac{\beta\cdot d}{V_{DS}}\right) \tag{6}$$

where the notations of more constants are

$$\alpha=y_{n+}\cdot z_{n+}\cdot\frac{q^3}{h^2}\cdot\sqrt{\frac{2m_n^*}{\chi_S}} \tag{7}$$

$$\beta=\frac{8\pi\cdot\sqrt{2m_n^*}\cdot\chi_S^{3/2}}{3qh} \tag{8}$$

In our case, the drain current is: $I_D=yz.J_{FN}$, where y and z corresponds to the device size, [20]. For Si-n^+ material with $y_{n+}=10nm$, $z_{n+}=10nm$, results: $\alpha=3.44\cdot 10^{-13}A/mV^2$, $\beta=22\cdot 10^9 V/m$.

Considering x_c as constant parameter, the variation of the tunnel current I_t, versus the drain-source voltage V_{DS} is analytically studied. The tunnel current monotonically increases with the drain-source voltage, accordingly with the first order derivative study. But the tunnel current decreases with the cavity width x_c, accordingly with its derivative:

$$I_t'(d)=-\alpha\cdot\frac{V_{DS}^2}{d}\cdot exp\left(-\frac{\beta\cdot d}{V_{DS}}\right)\cdot\left(\frac{1}{d}+\frac{\beta}{V_{DS}}\right) \tag{9}$$

In this case $x_c>0$ and $V_{DS}>0$ ensures a tunnel current decreasing with the distance d, fig. 4.

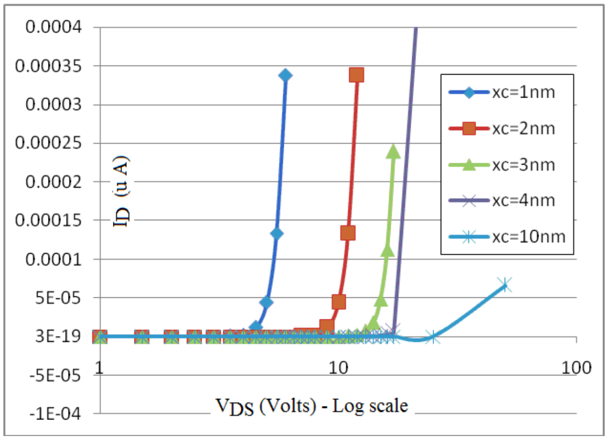


Fig. 4. Checking the ID-VDS increasing with VDS and ID decreasing with x_c.

Conclusion here: Analytical study reveals an exponential drain current increasing with VDS. It is an ON/OFF switch commanded by the VDS voltage. Also the VDST increases with the xc value.

B. *A specific model suitable for NECT applying*

Due to the electrons tunneling through a triangle potential barrier, the drain current is modeled with:

$$I_D(V_{DS})=A\cdot V_{dsT}V_{DS}\cdot exp\left(-\frac{B}{V_{DS}}\right) \tag{10}$$

where A, B are constants depending on χ_s and geometrical sizes of NOI, V_{DS} is the drain-source voltage and V_{dsT} is a constant model parameter, named threshold drain-source voltage. The proposed model (10) is an approximation of a physical model expressed by A, B constants:

$$I_D(V_{DS})=A\cdot V_{DS}V_{DS}\cdot exp\left(-\frac{B}{V_{DS}}\right) \tag{11}$$

The new model (10) is suitable to the V_{dsT} vicinity. The target of the approximated model (10) is to offer a function with oblique asymptotes:

$$I_D=A\cdot V_{dsT}\cdot(V_{DS}-B) \tag{12}$$

The simulated output characteristics, I_D-V_{DS}, at $V_{GS}=0.6V$ and $V_{GS}=1V$, seam to present a sub-threshold conduction for $V_{DS}<4V$, fig. 5, black curves. Here, the NOI transistor seems to present a drain-source threshold voltage.

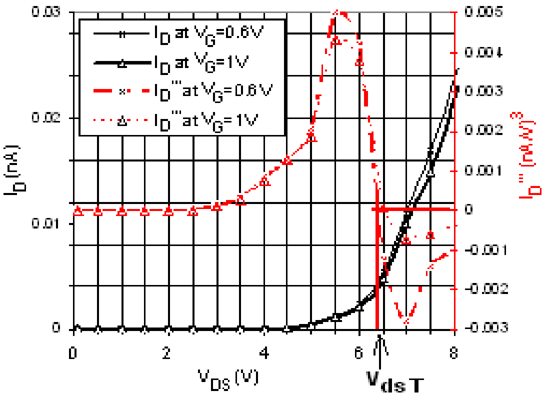


Fig. 5. The ID-VDS characteristics for the NOI device biased at V_G = 0.6V and 1V in black lines at the left side and the third order derivative values in the right side.

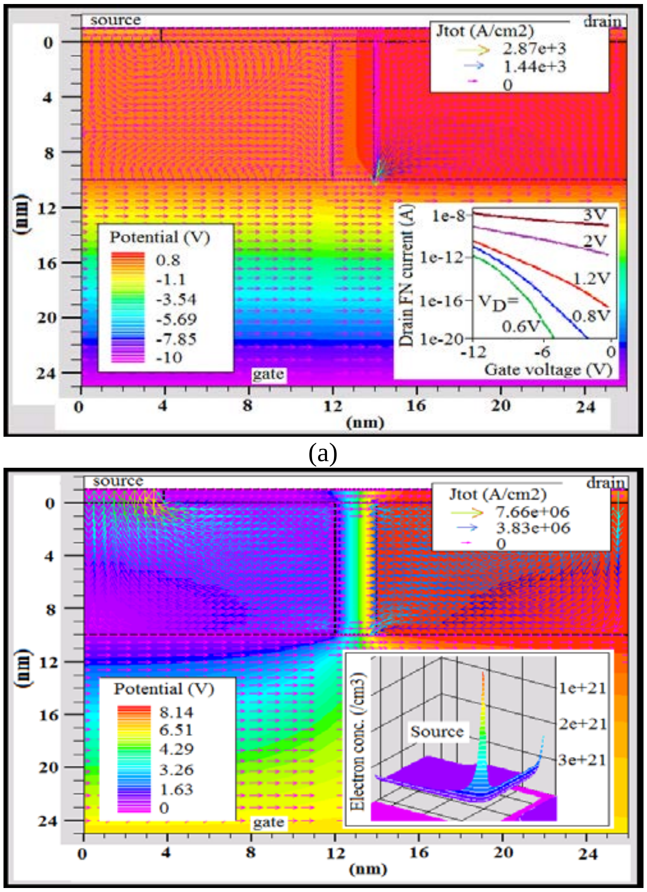
A valuable tool in order to characterize a non-linear conduction and to extract an accurate threshold point is the *Non-Linear Electrical Conduction Theorem NECT*, [14]. Accordingly with this theorem: for any nonlinear electrical conduction function with asymptotic behaviors at ±∞, there is at least, a point where the third order derivative gets zero value. The zeroing values have a “threshold” value meaning.

The threshold voltage V_{dsT} can be extracted now by numerical derivative of the simulated I_D-V_{DS} curves by Origin, fig. 5, red lines. The value $V_{dsT} \approx 6.4V$ results from the I_D''' interception with the horizontal axis. This parameter stands for a certain boundary between a weak and strong conduction for the I_D-V_{DS} characteristics.

IV. VALIDATIONS BY SIMULATIONS

Using a drain voltage, $V_D \geq 2V$ or higher (e.g. V_{D1}=3V,..., V_{D4}=6V), the simulations provides I_D-V_{GS} curves corresponding to a strong tunneling. When $V_D < 2V$ (e.g. V_{D1}=1V,..., V_{D4}=0.6V), the device enter in a so called weak tunneling regime, offering two firm states, [18].

The explanation is searched in the physical structure now. The contour of potentials indicates the device bias in each case: weak tunneling (fig. 6.a) or strong tunneling (fig. 6.b). A negative gate voltage induces an inversion regime in the n-type semiconductor islands, at the films bottom. But the gate action is stronger in the weak tunneling regime, concentrating the current density at the film bottom, fig. 6.a. In strong tunneling, the current vectors are quite uniform distributed, fig. 6.b. The electrons have high concentrations along the vacuum cavity. The pure Fowler Nordheim current from fig. 6.a inset, which is a horizontal source-drain tunneling current, show a much more sensitive dependence on the transversal electric field produced by V_{GS}, in weak tunneling at V_{DS} ~ 0.8V than in strong tunneling at V_{DS} = 3V.



(a)

(b)

Fig. 6. Contours of potential and vectors of total current density thru the device at: (a) V_{DS}=0.8V, V_{GS}=-10V; in inset - the pure Fowler Nordheim current; (b) V_{DS}=8V, V_{GS}=5V; in inset - the electron concentration in the source region.

The Energy Balance Transport Model adds continuity equations for the carrier temperatures, activated by parameters KSN=KSP=-1. The electron and hole temperatures are set equal to the lattice temperature. The Lattice Temperature distribution across the NOI structure maximum biased at V_{GS}=-8V and V_{DS}=12V assumes the substrate as thermal contact at 290K, but no special temperature gradients occur, [20]. It is important to check the electric field distribution at these higher voltage values, fig. 7.

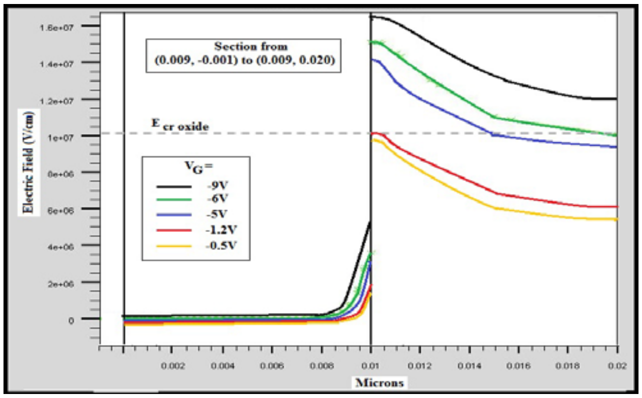


Fig. 7. The electric field distribution for the NOI device at V_S=0V,

V_D=+5V and different V_G.

The critical electric field is reached at the oxide surface from VG < 1.2V and is extended till the oxide bottom for VG < -6V, when the leakage current thru the gate terminal starts to increase.

V. CONCLUSION

This paper presented an analytical model of the output characteristics of a Nothing On Insulator transistor and its planar p-NOI variant. An exponential dependence was emphasized. Using the NECT theorem a threshold drain voltage was rigorously established, separating the strong and weak tunneling regimes. The Atlas simulations validated the mathematical model.

REFERENCES

[1] K. Subramanian, W.P. Kang, and J.L. Davidson, “A Monolithic Nanodiamond Lateral Field Emission Vacuum Transistor,” *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1259-1261, Nov. 2008.

[2] M. Suzuki, M. Sagawa, T. Kusunoki, E. Nishimura, M. Ikeda, and K. Tsuji, “Enhancing Electron-Emission Efficiency of MIM Tunneling Cathodes by Reducing Insulator Trap Density,” *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2256–2262, Aug. 2012

[3] Ernest G. Zaidman, “Simulation of Field Emission Microtriodes”, *IEEE Transactions on Electron Devices*, vol. 40, pp.1009-1015, 1993.

[4] S-S. Park, D-Il Park, S-H. Hahm, J-H. Lee, H-C. Choi, and J.-H. Lee, Fabrication of a lateral field emission triode with a high current density and high transconductance using the local oxidation of the polysilicon layer,” *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1283-1289, Jun 1999.

[5] C. Ravariu, “The implementation methodology of the real effects in a NOI nanostructure aided by simulation and modelling,” *Elsevier Journal of Simulation Modeling Practice and Theory*, vol. 18, no. 9, pp. 1274-1285, Oct. 2010.

[6] C. Ravariu, “ Semiconductor Materials Optimization for A TFET Device with Nothing Region On Insulator,” *IEEE Trans. on Semiconductor Manufacturing*, vol. 26, no. 3, pp. 406-413, Aug. 2013.

[7] C. Ravariu, A. Rusu, M. Profirescu, and F. Ravariu, “A Nano-Transistor with a Cavity,” *in Proc. IEEE 8-th International Conference Nanotech-MSM*, Anaheim, USA, vol.1, chapter 4, pp.111-114, 2005

[8] C. Ravariu, and F. Babarada, “Modeling and simulation of special shaped SOI materials for the nanodevices implementation,” *Hindawi Journal of Nanomaterials*, ID 792759, pp. 1-11, July 2011.

[9] C. Ravariu, D. Mihaiescu, F. Babarada, E. Manea, M. Idu, L. Vladoianu, Vertical Variants of PIN and p-NOI Tunnel Electronic Devices and Potential Applications, 5th International IEEE Symposium On Electrical and Electronics Engineering, Galați, Romania, Oct. 20-22, 2017, pp.36.1-36.6.

[10] Cristian Ravariu, Florin Babarada; Resizing and reshaping of the Nothing On Insulator NOI Transistor; Advanced Nano-Bio-Materials and Devices; 2017, vol.1, issue 1, pp. 18-23.

[11] Richard G. Forbes, “Description of field emission current/voltage characteristics in terms of scaled barrier field values (f-values), ” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 26, no. 209, 2008.

[12] C. Ravariu, “A Compact NOI Nano-Device Simulation,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 8, pp. 1841 - 1844, Aug 2014.

[13] C. Ravariu, Deeper Insights of the Conduction Mechanisms in a Vacuum SOI Nanotransistor, IEEE Transactions on Electron Devices, vol. 63, no. 8, 2016, pp. 3278 – 3283.

[14] Adrian Rusu. A Theorem of the Non-Linear Electrical Conduction, Proceedings Int. IEEE Conf. of Semic. CAS'1993, Sinaia, Romania, pp. 31-34, 1993.

[15] J. Pretet, S. Monfray, S. Cristoloveanu, and T. Skotnicki, “Silicon-On-Nothing MOSFETs: performance, short channels effects and back gate coupling,” *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 240-245, Feb. 2004.

[16] S.O. Koswatta, M.S. Lundstrom, and D.E. Nikonov, “Performance Comparison Between p-i-n Tunneling Transistors and Conventional MOSFETs,” *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 456-465, March 2009.

[17] V. Nagavarapu, R. Jhaveri, and J.C.S. Woo, “The tunnel source (PNPN) n-MOSFET: A novel high performance transistor,” *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013–1019, Apr. 2008.

[18] J.-W. Han, J. S. Oh, and M. Meyyappan, Vacuum nanoelectronics: Back to the future?—Gate insulated nanoscale vacuum channel transistor, Applied Physics Letters 100, 213505, pp. 1-4, 2012.

[19] SILVACO Inc., *ATLAS User’s Manual*, Jan., 2012, pp. 96-129.

[20] Cristian Ravariu, Dan Mihaiescu, Static and dynamic aspects of different tunneling NOI nanotransistors with oxide and vacuum, in Proceedings of European Conference on Electrical Engineering and Computer Science, Berna, Switzerland, 17-19 Nov. 2017, pp.1-4.

Cristian Ravariu became IEEE Member in 2008. He received the B.S.('93), Ph.D ('01), PostDoc ('12) degrees at the Polytechnic University of Bucharest, Romania in the Electron Devices domain and Bioelectronics with specialization stages and/or visiting positions at EPFL - Federal Institute of Technology from Lausanne, Switzerland, LAAS-CNRS Laboratory for Analysis and Architecture of Systems, Toulouse, France and Faculty of Bioengineering from Patras, Greece. Between '93-'99 he activated as researcher at the Institute of Microtechnology Bucharest, in the field of Electronic Devices Simulation and Silicon technology. Now, he is Professor at Polytechnic University of Bucharest, Electronic Device and Circuits Department, being interested in the electronics devices development. He has published more than 100 articles.

Since 2014 Dr. Ravariu helps to revitalize the Electron Device Romanian Chapter, serving in the lasts two years as the Chairman of this ED15 Chapter.

Dan Mihaiescu (Ph.D.-chemistry), now is Professor of Instrumental Analysis and Organic Chemistry, of the Organic Chemistry “Costin Nenitescu” Department, Faculty of Applied Chemistry and Material Science, Polytechnic University Bucharest, Romania. His main areas of interest are related to Organic Chemistry, Instrumental Analysis, Nanotechnology, Plasma Chemistry, Natural Products, Forensic Chemistry, Oceanography, GIS integration of analytical data. Currently Dr. Dan Mihaiescu' researches focus on the advanced nanocomposite / hybrid materials synthesis (magnetic nanocarriers, core-shell nanoparticles, electronic devices and materials, characterization and applications.