Design of 24GHz Frequency Source based on Phase Noise Analysis

Bo Yin, Shuai Zhang, Shiwei Zhao, Wei Luo, Wen Huang

***Abstract*—**A 24 GHz Phase-Locked Loop (PLL) frequency source based on the analysis of the phase noise of the system is presented. Instead of using Direct Digital Synthesizer (DDS) and the combination of DDS and PLL, the design method of a single PLL circuit is adopted in this paper. Based on the phase noise model of the PLL system, it is concluded that the selection of loop bandwidth determines the phase noise performance of the frequency source by analyzing the characteristics of the phase noise transfer function of each noise source. ADIsimPLL4.10 software is used to adjust the bandwidth of the Loop Filter, so that the designed Loop Filter meets the design requirements of the 24GHz microwave frequency source. The test results show that output frequency of the frequency source is at 24.17GHz, and its phase noise is -102.48dBc/Hz@10kHz. Compared with the frequency source designed by other methods, this design has the advantage of low phase noise.

***Keywords*—**PLL; frequency source; loop bandwidth; low phase noise

I. Introduction

THE frequency source is the core device of the electronic system such as navigation, radar and other electronic systems, which is called the heart of the electronic system. With the development of modern communication technology, the electronic system also puts forward higher performance requirements for the frequency source. According to different application requirements of microwave frequency source, different technical methods are adopted to complete the design. In [1], the parameters (frequency, amplitude, mean value) of high frequency drive current are digitalized and dynamically programmed by DDS technology, which presents a Giant Magneto-Impedance (GMI) magnetic sensor with DDS as a high stable frequency source. In [2], a high speed 2.502GHz DDS in 0.1802μm CMOS is achieved by time interleaved structure. Frequency Modulated Continuous Wave (FMCW) signal is generated in [3] by using the DDS, and the measurement of this kind of signal is realized on the module DDS. A 40 GHz PLL frequency synthesizer for 60 GHz wireless communication applications is presented in [4]. A 60-GHz fundamental frequency PLL is introduced in [5] as part of a highly integrated system of on-chip memory and antenna. A monolithic K-band PLL for microwave radar applications is implemented, the phase noise of the system is reduced by eliminating the tail transistor and using optimized high-Q LC-tank in [6]. The combination of DDS and PLL is adopted in [7] so that the final output frequency of the entire system is C-band microwave for Doppler weather radar. It is not difficult to find that the current technologies for realizing frequency source is DDS, PLL, and the combination of DDS and PLL. However, the upper limit frequency of output signal of the frequency source is not high by using the DDS. The combination of DDS and PLL can overcome this problem, and the frequency conversion speed is fast, the frequency resolution is high in [8,9], but its drawback is that the circuit structure is complex and the debugging is not convenient [10].

In this paper, a single PLL circuit is used to design a 24GHz frequency source. The circuit is relatively simple, with low phase noise, low power, high spectral purity, the output frequency is easy to program control and so on.

II. PLL Frequency Source Principle

The PLL circuit is a phase negative feedback control circuit, which is characterized by the use of external input reference signal to control the frequency and phase of the internal oscillation signal of the loop. Because PLL can be used to realize the same frequency of the output signal as the input signal, PLL is always used in closed-loop tracking circuits.

The basic structure of a PLL is shown in Fig.1, which is composed of a Phase Detector, a Loop Filter and a Voltage Controlled Oscillator (VCO). Among them, the Phase Detector is used to compare the phase of the input signal with that of the VCO, and its output voltage is filtered and applied to the VCO whose output frequency moves in the direction so as to reduce the phase difference of both input and output signals. The Loop Filter is also called Low-Pass Filter, which is used to provide pure Direct-Current (DC) control voltage for VCO and to provide stable phase margin for the system. The VCO is used to generate oscillatory signals with variable frequency and its output frequency is controlled by the DC voltage. And, the output frequency of most VCO increases with the increase of control voltage and has a positive slope. The Frequency Divider between the VCO and the Phase Detector is used to divide the output frequency of VCO to match the frequency of the reference signal. In general, the Frequency Divider uses the

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Bo Yin, Shuai Zhang, Shiwei Zhao, Wei Luo, Wen Huang are all with the College of Electronic Engineering, Chongqing University of Posts and Telecommunications, Chongqing, 400065, China (phone: 86-23-62460184; e-mail: yinbo@cqupt.edu.cn, 1149116420 @qq.com).

Digital N Divider for digital switching to change the output frequency of the PLL circuit. The PLL input reference signal is provided by a Temperature Compensated Crystal Oscillator that generates high precision frequency signals. In this way, after the output signal of VCO switches the frequency through the Frequency Divider, the output signal of VCO is obtained with the same precision as the input frequency. This is how the PLL frequency source works, as shown in Fig.1.

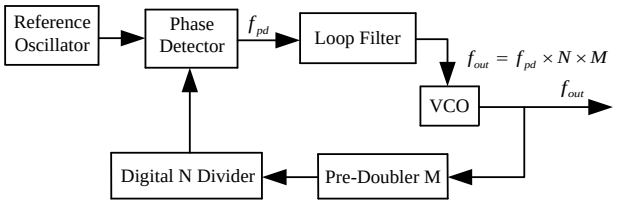

Fig.1 Basic structure of PLL frequency source

In addition, in order to increase output frequency of the PLL microwave frequency source, it is common to adopt a method of connecting the Pre-Doubler M between the VCO and the Digital N Divider.

III. Phase Noise Analysis of Each Noise Source in PLL System

Phase noise is the random change of the phase of the system output signal caused by various noises. It is an important parameter for the PLL system to measure the purity quality of its spectrum. The magnitude of phase noise can reflect the performance of microwave frequency source. The phase noise of microwave frequency source is lower, its performance is better. The noise of PLL system mainly comes from four parts, which are reference signal source, Phase Detector, VCO and Digital N Divider. Fig.2 shows the phase noise model of PLL system. Where K_d is phase detector gain, K_v is voltage control sensitivity of the VCO, θ_{nr}, θ_{nd}, θ_{nv}, θ_{nn} and θ_{no} are the phase noise of reference signal source, Phase Detector, VCO, Digital N Divider and output signal of the PLL frequency source, respectively.

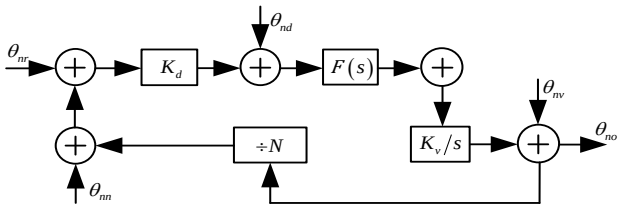

Fig.2 The phase noise model of PLL system

According to the classical closed-loop system control theory, the phase transfer function of each noise source is calculated and analyzed by using the system linear analysis method. The phase noise model of PLL system, as shown in Fig.2. Assuming that the phase noise in the system is only input from the reference signal source, and all other noise sources are zero input, the following formulas can be deduced from the system phase noise model block diagram.

$$\left[\theta_{nr}(s)-\frac{\theta_{no}(s)}{N}\right]\cdot K_d\cdot F(s)\cdot\frac{K_v}{s}=\theta_{no}(s) \tag{1}$$

$$\frac{\theta_{no}(s)}{\theta_{nr}(s)}=\frac{K_d\cdot F(s)\cdot\frac{K_v}{s}}{1+\frac{1}{N}\left[K_d\cdot F(s)\cdot\frac{K_v}{s}\right]} \tag{2}$$

Suppose $G(s)=K_d\cdot F(s)\cdot\frac{K_v}{s}$, $H=\frac{1}{N}$, then

The transfer function of the phase noise introduced by the reference signal source is written as

$$H_{\theta_{nr}}(s)=\frac{G(s)}{1+H\cdot G(s)} \tag{3}$$

In the same way, the transfer function of phase noise introduced by Phase Detector is written as

$$H_{\theta_{nd}}(s)=\frac{G(s)}{1+H\cdot G(s)}\cdot\frac{1}{K_d} \tag{4}$$

The transfer function of the phase noise introduced by the Digital N Divider is written as

$$H_{\theta_{nn}}(s)=\frac{G(s)}{1+H\cdot G(s)} \tag{5}$$

The transfer function of phase noise introduced by VCO is written as

$$H_{\theta_{nv}}(s)=\frac{1}{1+H\cdot G(s)} \tag{6}$$

Where:

F(s) is the transfer function of Loop Filter.

G(s) is the open-loop transfer function of PLL system.

G(s)/[1+*H* · *G(s)*] is the closed-loop transfer function of PLL system.

In PLL circuit, because *F(s)*, *G(s)* and *G(s)*/[1+*H* · *G(s)*] are low pass characteristic, the phase noise transfer function introduced by reference signal source, Phase Detector and N Frequency Divider is low pass characteristic, while the phase noise transfer function introduced by VCO is high pass characteristic. In other words, the in-band phase noise of the frequency source loop is determined by the reference signal source, the Phase Detector and the N Frequency Divider, while the out-of-band phase noise of the frequency source loop is determined by the VCO. Therefore, in order to optimize the phase noise performance of the frequency source, the proper selection of the loop bandwidth is very important.

IV. Loop Filter Design and Phase Noise Simulation of 24GHz Frequency Source

A. Loop Filter design of 24GHz frequency source

The target parameters of the frequency source in this design is that the output frequency is 24.17GHz, and its phase noise is better than -100dBc/Hz@10kHz.

According to the analysis of the third part, the selection of loop bandwidth plays an important role in maintaining the stability of the loop and controlling the internal and external noise of the loop. With the help of ADIsimPLL4.10 software, the loop bandwidth can be adjusted to complete the design of Loop Filter and make it meet the requirement of 24GHz frequency source phase noise. Fig.3 shows the circuit diagram of Active Loop Filter designed by ADIsimPLL4.10 software.

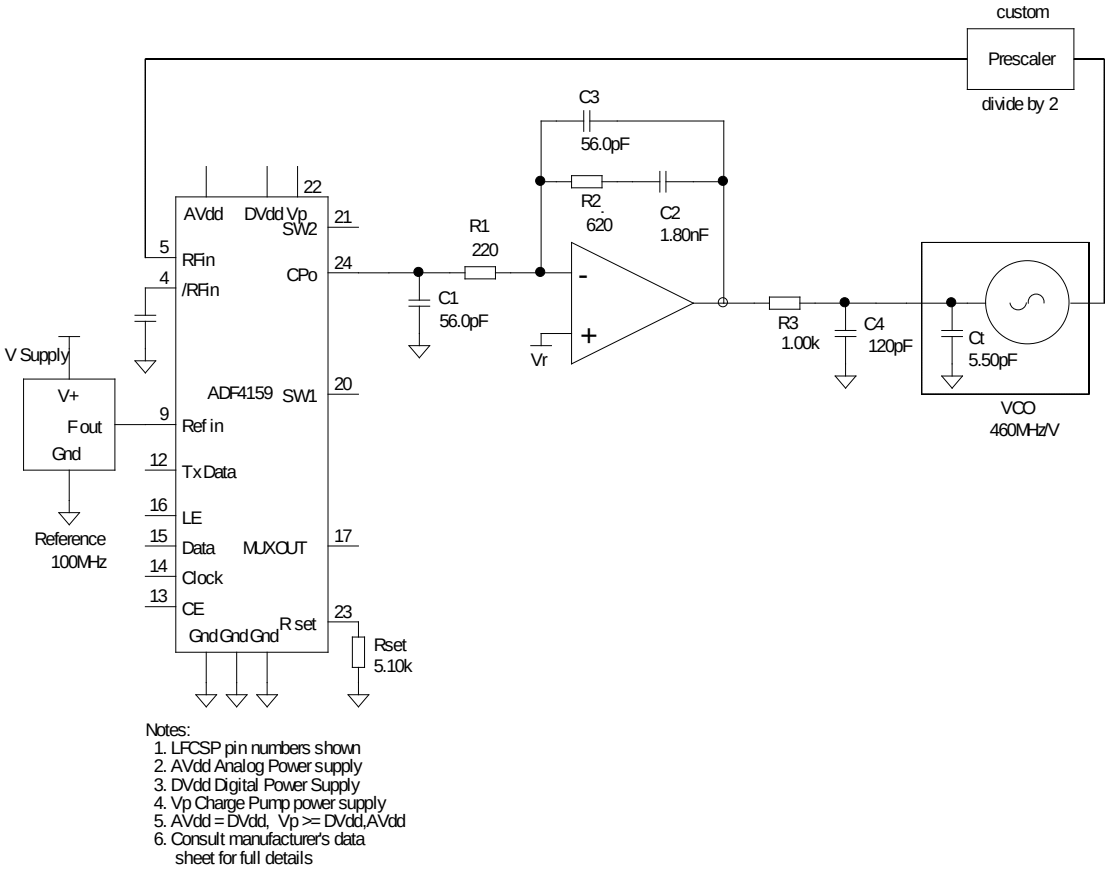

Fig.3 Circuit design diagram of Active Loop Filter

The loop bandwidth is proportional to the phase noise of the reference signal source, Phase Detector and Loop Filter, while it is inversely proportional to the locking time of the system and the phase noise of the VCO. According to the above, through the simulation of Active Loop Filter with different order, it is concluded that the higher the order of filter, the better the filtering effect and the faster the locking time. The phase noise of the system will be further reduced by adding a further Low-Pass Filter stage composed of resistors and capacitors at the output, so the topology of the Loop Filter is chosen in Fig.3.

B. Simulation and analysis of 24GHz frequency source

By adjusting the loop bandwidth and phase margin several times, the simulation results show the amplitude and phase frequency curves of the open-loop system, as shown in Fig.4.

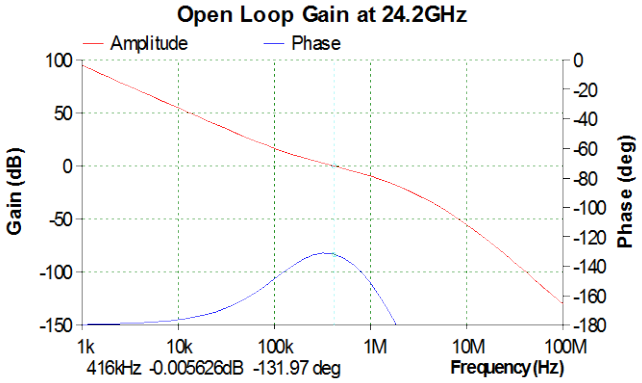

Fig.4 Open-loop system response of the PLL frequency source

From Fig.4, it can be clearly found that when the open-loop gain is 0dB, the frequency source system is stable, and the loop bandwidth is 416 kHz and the phase margin is 48° . The locking time when the system is stable is 6 us, as shown in Fig.5.

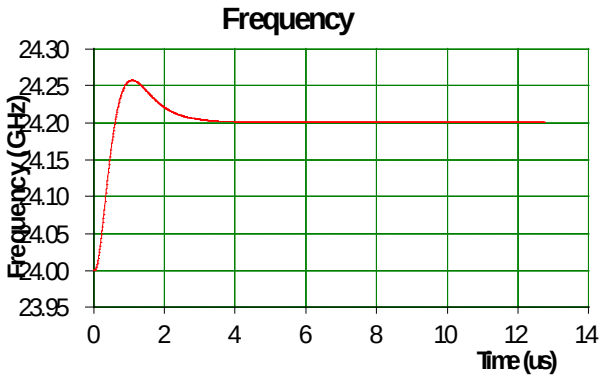

Fig.5 Locking time Curve of the PLL Frequency Source

The phase noise of the PLL Frequency Source system at frequency offset 10kHz is -104dBc/Hz, as shown in Fig.6. Where PN_{Total} is the total output phase noise of frequency source, $PN_{Loop\ Filter}$, PN_{Chip}, PN_{Ref} and PN_{Vco} are only the phase noise introduced by Loop Filter, Phase Detector chip, reference signal and VCO, respectively. From the simulation results of phase noise of the PLL frequency source, it can be seen that in the range of 1 kHz offset carrier frequency, the PN_{Total} is limited by the Reference Oscillator noise. The PN_{Ref} becomes the limiting factor of the in-band phase noise after the deterioration of 20lgN. When the frequency offset is close to the loop bandwidth, the PN_{Chip} becomes the main factor that affects the total phase noise of the frequency source system. The PN_{Total} coincides with the PN_{Vco} when the cutoff frequency of the frequency source system is far away from the loop bandwidth. From the above analysis, it can be seen that the simulation results of the system phase noise are consistent with the theoretical analysis results.

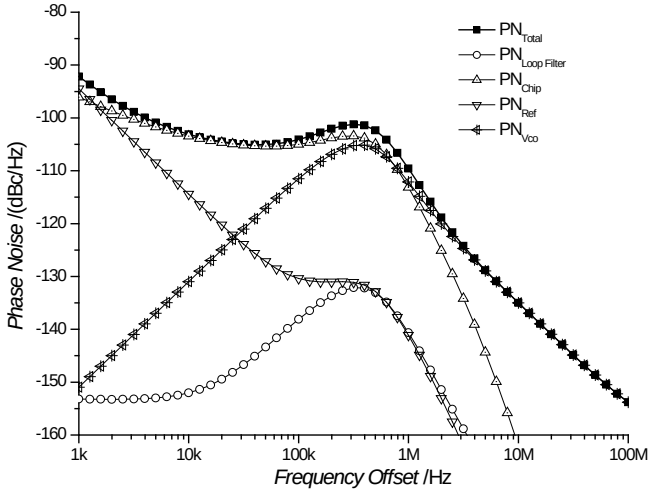

Fig.6 Simulation results of the phase noise of PLL frequency source

V. Design of PCB and Phase Noise Measurement of 24GHz Frequency Source

A. Design of PCB Board for 24GHz Frequency Source

The design and manufacture of PCB board plays a decisive role in the performance of the product. The 24GHz frequency source circuit board in this paper belongs to the high frequency circuit board. The highest output frequency of the circuit board is up to 24GHz or more, and the core devices such as Active Temperature Compensation Crystal Oscillator and VCO are used. Therefore, the whole system has very high requirements for anti-interference, anti-noise and electromagnetic compatibility.

Finished processing of the frequency source physical, as shown in Fig.7.

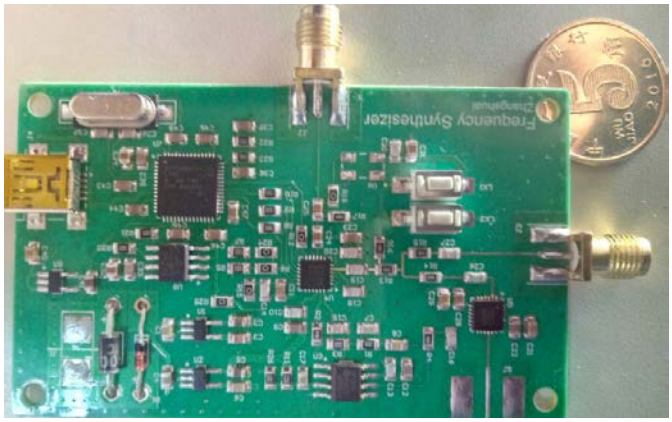

Fig.7 Physical map of the 24GHz frequency source

During design, in order to get a purer RF output signal, many problems such as circuit board stack structure, device layout and signal wiring must be carefully considered in the design of hardware circuit. The following is a brief description of the design of the 24GHz frequency source. Firstly, in order to obtain better EMC, the circuit board adopts four layers, the top layer and the bottom layer are both signal layers, the RO4350 is used as the material of the circuit board, and the FR4 board is used between the middle ground and the power layer. Because there are analog ground level, digital ground level and various supply voltage signals in the frequency source, the ground and power layer should be partitioned. Secondly, in order to reduce the interference between the power ripple and the device, the power pin of the device should be decoupled and filtered with the capacitor. The stable power supply in the frequency source should also be separated from the Crystal Oscillator and the VCO, and the Crystal Oscillator should be far away from the VCO. Thirdly, the signal alignment should be calculated by impedance matching. The difference line width of the frequency source is 6.7mil, the line distance is 5.8mil, the RF signal width is 8.1mil, but the ground and power lines should be widened as far as possible to reduce the impedance. In addition, to avoid electromagnetic radiation, wiring should be as short as possible, preferably straight or 45-degree broken lines. Especially, the distance between loop filter and feedback loop should be as small as possible to prevent the PLL circuit from losing lock due to too long running line.

B. Measurement and analysis of phase noise of 24GHz frequency source

After completing frequency source PCB processing, the frequency source is tested, as shown in Fig.8.

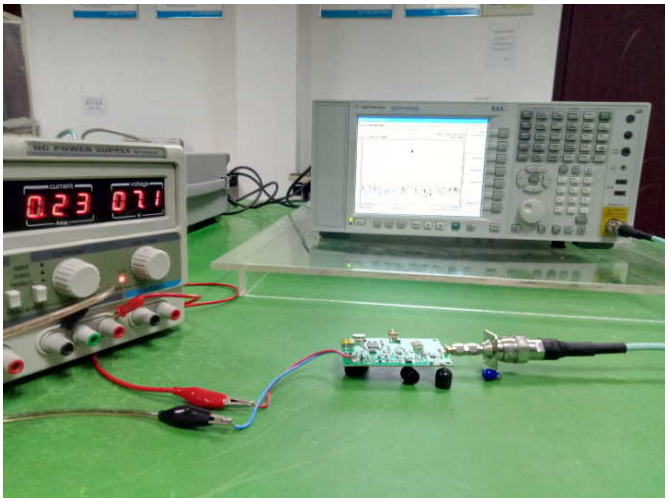

Fig.8 Physical test chart of frequency synthesizer

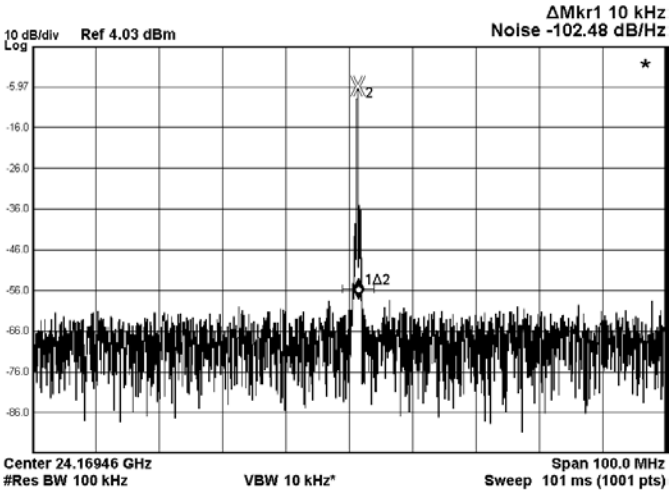

Fig.9 Phase noise of output frequency at 24.17GHz

When testing, first prepare the test equipment, and check whether the welding PCB soldering, leakage and so on. Then provide the frequency source power supply, and check the output voltage and current of the power supply is normal. After confirming that there are no errors, configure the programming sequence. According to the data sheet of ADF4159, the following equation governs how the synthesizer must be programmed.

$$RF_{out} = \left[INT + \left(FRAC / 2^{25} \right) \right] \times f_{PFD} \tag{7}$$

Where：

RF_{out} is the RF frequency output.

INT is the integer division factor.

FRAC is the fractionality.

The PFD frequency (f_{PFD}) equation is

$$f_{PFD} = REF_{IN} \times \left[(1+D) / (R \times (1+T)) \right] \tag{8}$$

Where:

REF_{IN} is the reference frequency input.

D is the RF REF_{IN} doubler bit, Bit DB20 in Register R2 (0 or 1).

R is the RF reference division factor (1 to 32).

T is the reference divide-by-2 bit, Bit DB21 in Register R2 (0 or 1).

The reference frequency and phase detection frequency of this 24GHz frequency source are both 100 MHz and its output frequency rate is 24.17 GHz. According to the formula (7) and (8), the register value inside the chip is configured, and each register inside the phase-locked chip is controlled by Microcontroller Unit, so that the PLL circuit can be locked. After the above operation, the signal to be tested is connected to the Agilent N9010A spectrum analyzer for phase noise testing. After several debugging and optimization, the test results show that the phase noise is up to -102.48dBc/Hz@10kHz when the output frequency of the PLL frequency source is 24.17GHz, as shown in Fig.9.

Because of the influence of the Phase Detector flicker noise, the test results of phase noise at offset carrier 10kHz are slightly different from the estimated results and simulation results, but above the design requirement -100 Bc/Hz@10kHz, as shown in Table 1. Therefore, it is feasible and effective to design the 24GHz PLL frequency source based on the phase noise analysis.

Table 1 Phase noise of 24GHz frequency synthesizer in this paper

Phase noise	Required value	Simulation value	measured value
dBc/Hz@10kHz	better than -100	-104	-102.48

This paper is compared with the phase noise of other frequency bands of frequency sources, such as table 2. The phase noise of the frequency source designed in this paper can reach -102.48dBc/Hz@10kHz, which is 7 dB better than that of the frequency source in [11]. Compared with the phase noise of the K-band frequency source in [12], the phase noise is improved by 3 dB.

Table 2 Phase noise comparison between this paper and other frequency band documents

Parameter	Paper[11]	Paper[12]	This paper
Output frequency	Ku-band	K-band	24.17GHz
Phase noise (dBc/Hz@10kHz)	-95	-99	-102.48

VI. Conclusion

Based on the phase noise model of PLL system, the phase transfer function characteristics of each noise source are calculated and analyzed, and the phase noise of 24GHz PLL frequency source is simulated. The results show that when the output frequency of the PLL frequency source is 24.17GHz, its phase noise is -102.48dBc/Hz@10kHz, which meets the design requirements. Compared with the frequency source designed by other methods, the 24GHz PLL frequency source designed by single PLL circuit has the advantage of low phase noise, which provides a reference for the design of 24GHz frequency source.

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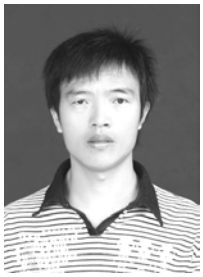

Bo Yin received the master's degree from the Chongqing University of Posts and Telecommunications, Chongqing, China, in 2007, and the Ph.D. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2014. He is currently an associate professor with Chongqing University of Posts and Telecommunications, Chongqing. His research interests include MIMO technology in radio communication, and design of radio frequency microwave circuit.

Shuai Zhang received the B.S. degree in electronic engineering from Chongqing University of Posts and Telecommunications, China, in 2015, and is working towards the M.S. degree. His research interest includes design of radio frequency microwave circuit

Shiwei Zhao received the M.S. and Ph.D. degrees in electromagnetics and microwave technology, from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2003 and 2011, respectively. He has worked in San Jose American ISSI (Integrated Silicon Solution, Inc.) Company and Shanghai radio equipment research institute since from 2004 to 2016. He is currently working in Chongqing University of Posts and Telecommunications, Chongqing, China. He has over 15 years of experience in the RF/Microwave-circuits field and has successfully designed two Microwave-circuits chips and several commercial RF receivers. His current research interests include RF/MW circuits and systems, frequency synthesis, wireless communication and non-linear dynamic systems.

Wei Luo received the Ph.D. degree in Radio physics from XiDian University, Xi'an, China in 2011. He has worked for HUAWEI TECHNOLOGIES CO., LTD. as an antenna system engineer from 2011 to 2015. He is currently an associate professor in Chongqing University of Posts and Telecommunications, Chongqing, China. His current research interests include antenna design for mobile communication and electromagnetic scattering modeling for microwave remote sensing.

Wen Huang received the B.S. and Ph.D. degrees in electronic engineering, both from Sichuan University, Chengdu, China, in 2008 and 2013, respectively. She is currently an associate professor in Chongqing University of Posts and Telecommunications, Chongqing, China. Her current research interests include RF components and metamaterial.