A monolithic high-voltage driver circuit based on a Dickson charge pump for MEMS actuator applications

Hui Peng, Herbert De Pauw, Pieter Bauwens, and Jan Doutreloigne

***Abstract*—**A monolithic high-voltage driver circuit is proposed for use in MEMS applications. To improve the efficiency of the driver circuit, an advanced charge recycling strategy and finger capacitor structure are implemented in the Dickson charge pump which acts as the high-voltage generator and can boost the output voltage to 100.9 V from a 3 V power supply. The proposed driver circuit offers an output voltage which can linearly sweep from 0 V to 100.9 V under zero-load conditions. By means of the feedback circuit, the driver circuit also can self-adjust the clock frequency to minimize the voltage variation caused by changes in the load conditions.

***Keywords*—** Charge recycling, Dickson charge pump, High-voltage generator, MEMS driver circuit.

I. Introduction

MANY applications need on-chip high-voltage generators, such as MEMS actuators [1], [2], [3], energy harvesters [4], reconfigurable antennas [5], the automotive industry [6], etc. High-voltage signals are also used to improve the performance and reliability of electronic systems in low-voltage designs [7], [8].

In this paper, we present a high-voltage driver circuit which is used on a MEMS-based interferometer. Fig. 1 shows the overall system. The interferometer is a movable lamellar MEMS grating which is controlled by an electrostatic actuator (simplified as a capacitive load in Fig. 1). It can be used in lots of domains such as telecommunication, medical diagnosis, food industry and process control.

The high-voltage driver has three parts: a charge pump (CP), a frequency regulator and a feedback loop. To make sure the interferometer has sufficient resolution, the lamellar grating needs to have enough displacement range. In this project, the proposed high-voltage driver's maximum output voltage can reach 100.9 V with a 3 V supply voltage, which is slightly higher than the required 100 V driving capability for the electrostatic actuator so that the lamellar grating achieves the necessary displacement range. With the frequency regulator and feedback loop, the driver's output voltage can sweep from 0 V to 100.9 V. The main part of the driver is the high-voltage CP. A modified Dickson CP is used as high-voltage generator, which not only can be easily integrated on a chip to save space but also can apparently improve the system's power efficiency.

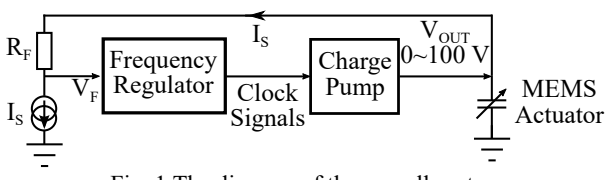

Fig. 1 The diagram of the overall system

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II. Proposed Driver Architecture

A. Charge Pump Circuit

In this design, we use the widely used Dickson CP as the high-voltage generator. To overcome the relatively low power efficiency problem of the Dickson CP, the charge recycling strategy is implemented in a 16-phase 8-branch CP, yielding improved power efficiency as reported in [9]. Fig. 2 shows one stage of the proposed 16-phase 8-branch CP, where the bottom plates of the boost capacitors C_1-C_8 are connected by a transmission gate matrix to implement the charge recycling strategy. Fig. 3 shows the waveform of the boost capacitor's bottom plate C_1 in one stage and the charge recycling procedure. The principle of charge recycling in this 16-phase 8-branch CP is that instead of charging the bottom plate of boost capacitor C_1 directly from GND to VDD, it will first be

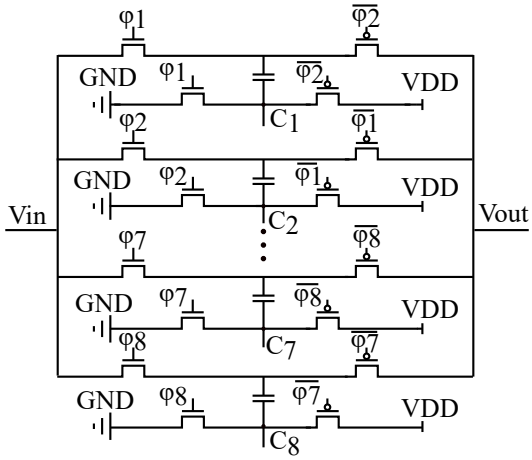

Fig. 2 One stage of the 16-phase 8-branch CP structure

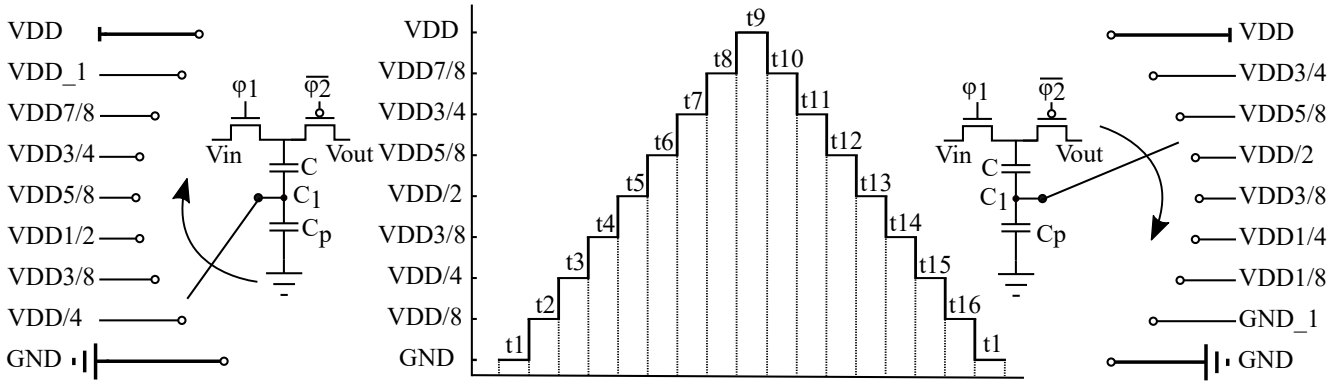

Fig. 3 16-phase 8-branch CP boost capacitor's bottom plate waveform

properly shorted by the transmission gate matrix to the bottom plate of other boost capacitors, in such a way that a 9-level triangular waveform is obtained. This strategy can significantly decrease the power dissipation due to parasitic capacitance and hence increase the power efficiency, as well as decrease the voltage ripple. The required maximum output voltage of this driver circuit is 100 V. For the Dickson CP, the boost capacitor must be able to withstand high voltages, especially for the last stage's boost capacitor which needs to have a breakdown voltage higher than 100 V. However, in current CMOS technology the high-voltage capacitor normally has significant parasitic capacitance [10]. As an example of a typical high-voltage CMOS technology, the 0.35 μm H35 CMOS IC technology of Austria MicroSystems (AMS) can provide a maximum operating voltage up to 120 V. In this technology there is only one type of high-voltage capacitor, the so-called CPM capacitor (Poly 1 – Metal 1 – Metal 2 – Metal 3 sandwich capacitor) which has a breakdown voltage higher than 100 V, but a parasitic capacitance as high as 94% of the nominal capacitance value, as shown in Table 1. Even though the charge recycling strategy can apparently decrease the power dissipation due to parasitic capacitance, the 94% parasitic to nominal capacitance ratio is still too high to design a high-performance driver circuit. To minimize the boost capacitor's parasitic capacitance, we designed a metal finger capacitor which not only has enough high-voltage handling capability but also significantly reduces the parasitic capacitance. Fig. 4 shows the cross section and top view of the finger capacitor. In this technology, there are four metal layers. The Metal 4 is the top thick metal layer, with a required minimum width of 2.5 μm and minimum spacing of 2 μm. For the Metal 3 the minimum width and spacing are both 0.6 μm. To make sure the finger capacitor has a high nominal capacitance, we use the minimum spacing between fingers and minimum width for every finger. Even though the Metal 2 and Metal 1 have slightly smaller spacing and width requirements, we set their spacing and width also to 0.6 μm in order to avoid a mismatch with the Metal 3 layer.

For the finger capacitor, apart from the spacing and width of the fingers, the nominal capacitance is also determined by the number of metal layers. The finger capacitor obviously has the maximum nominal capacitance if we use all the metal layers. But because the bottom metal layer Metal 1 is close to the substrate, the parasitic capacitance of the finger capacitor with all the metal layers also must be higher. To find the best trade-off between nominal and parasitic capacitance for this finger capacitor, we simulated capacitors with different number of metal layers. Capacitor CM1-4 has all the metal layers, CM2-4 uses Metal 2 to Metal 4 and CM3-4 only has Metal 3 and Metal 4. The simulation results are shown in Table 1 and the parasitic capacitance is extracted between one plate of the finger capacitor and the silicon substrate. Apparently capacitor

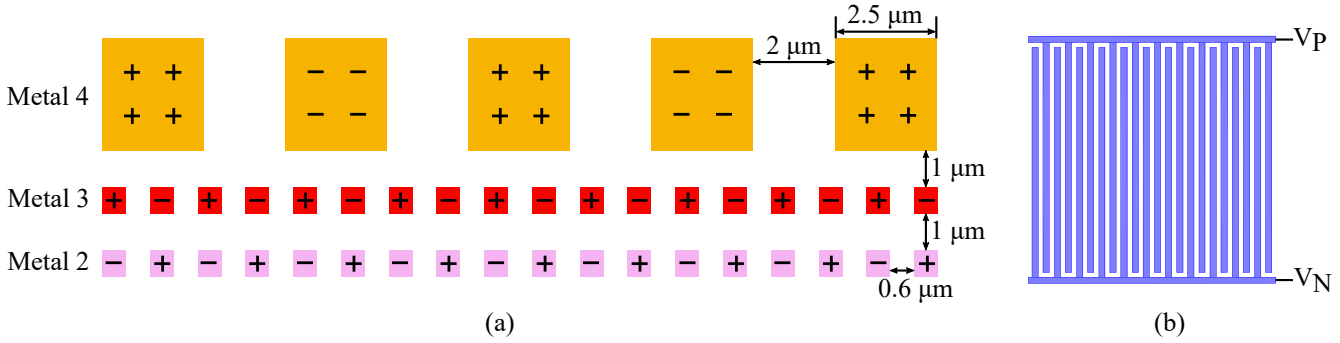

Fig. 4 (a) Cross section view of finger capacitor (b) Top view of one metal layer in finger capacitor

Table 1. The capacitance of different capacitor types (72 µm * 72 µm)

Capacitor	Nominal Capacitance [pF]	Parasitic Capacitance [pF]	Ratio of Parasitic to Nominal Capacitance [%]
CPM	0.672	0.632	94
CM1-4	1.106	0.082	7.4
CM2-4	0.771	0.039	5.1
CM3-4	0.426	0.027	6.2

CM2-4 has a reasonable nominal capacitance and the lowest ratio of parasitic to nominal capacitance. In this design, all the boost capacitors will use the finger capacitor CM2-4 with a capacitance of 0.771 pF.

B. Frequency Regulator and Feedback Circuit

To control this 16-phase 8-branch CP, a precise and stable clock signal is necessary. Fig. 5 shows the schematic of the on-chip frequency regulator. The frequency of this regulator is determined by the feedback voltage (V_F) which is connected to the gate of p-type MOSFET P_1. V_F controls the drain current of P_1, which drives the unity-gain current mirror $N_1 + N_2$, resulting in a ring oscillator bias current equal to the current through P_1. The ring oscillator's frequency (f) is determined by:

$$f = \frac{1}{2\tau n} \quad (1)$$

In which τ is the average inverter delay and n is the number of inverters. In this work the number of inverters is 17. When the current through the oscillator increases, the charge and discharge time for one inverter is becoming shorter, which means that inverter delay τ is decreased. By (1), the regulator's frequency will increase. It is therefore clear that the feedback voltage V_F and the oscillator's frequency exhibit a negative correlation, which is essential for obtaining stable behavior of the overall system. In this design, the oscillator's frequency can sweep from 0 to 9.32 MHz. The signal from the oscillator then passes through the waveform shaping and clock buffer circuits to become the expected clock signals φ_1, $\overline{\varphi_1}$, φ_2, $\overline{\varphi_2}$ .... φ_8, $\overline{\varphi_8}$ to control the CP.

The feedback circuit consists of a feedback resistor (R_F) and a current source as shown in Fig. 1. The current I_S of the current source can be digitally set with 8-bit resolution and is sunk from the CP's output node through the feedback resistor R_F. As a consequence, the feedback voltage V_F is given by:

$$V_F = V_{OUT} - R_F \times I_S \quad (2)$$

This equation provides the required negative feedback for stable operation. When the CP's output voltage V_{OUT} has a drop, V_F will also decrease, resulting in an increase of the clock frequency, which makes V_{OUT} rise again to compensate the initial drop. This keeps the output voltage at a fixed level that can be digitally programmed with 8-bit resolution.

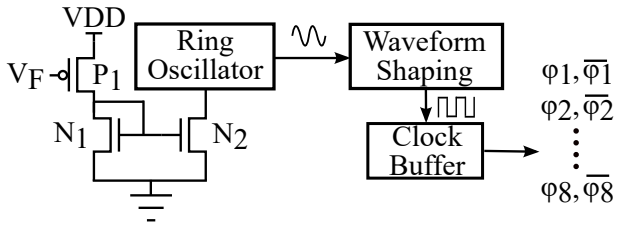

Fig. 5 The schematic of the frequency regulator

III. Simulation Results and Discussion

In this section we present the simulation results of the proposed driver circuit by using the 0.35 µm H35 technology of AMS. To achieve the required output voltage, this proposed 16-phase 8-branch CP includes 40 concatenated stages. A 20 pF capacitor is connected at the output of the last stage to stabilize the voltage.

Fig. 6 shows the output voltage of the driver circuit at different programming input values. The programming bits are ramped up starting from 0Fh to FFh at a constant rate and the corresponding output voltage sweeps from 8 V to 100.9 V which reveals a good linearity. Applying a linear fitting of the output voltage versus the programming input word $\sum B_i 2^i$, yields the equation:

$$V_{OUT} = 0.38996V \sum B_i 2^i + 2.3669V \quad (3)$$

The transient simulation waveform of the output voltage at different current load conditions is shown in Fig. 7. The programming value is fixed at FAh for the 8-bit resolution digital input. At the beginning, under zero - load condition, the driver circuit is working at its maximum clock frequency of approximately 9.32 MHz to minimize the difference between the actual and programmed output voltage as fast as possible. After about 0.25 ms the output voltage of the driver circuit has been boosted to the desired output voltage of 100 V and is then kept in a stable state. In this stable state the clock frequency drops gradually to 2.5 MHz which keeps the output voltage stabilized at 100 V. Starting from t=0.5ms, a current load of 5 µA is applied at the output of the driver circuit. Due to the increased current load, the output voltage starts to drop. But thanks to the feedback circuit and frequency regulator, the negative feedback causes the clock frequency to increase to 4.7 MHz, thereby preventing the output voltage from dropping any further. The current load is further increased to 10 µA at t=1ms. Based on the same principle, the clock frequency is increased to

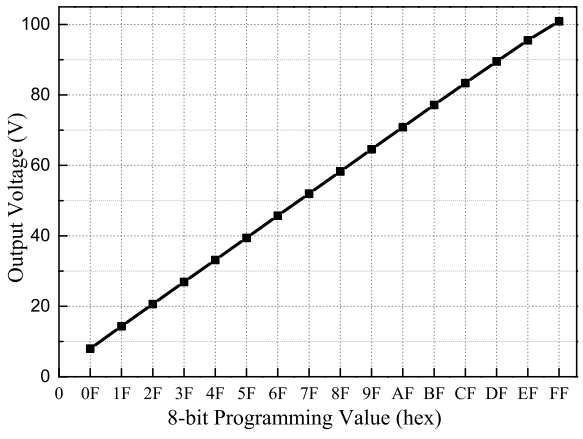

Fig. 6 Output voltage at different programming input values

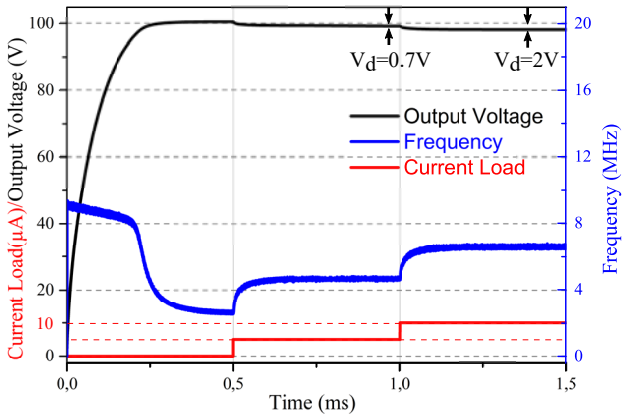

Fig. 7 Output voltage at different current load

6.5 MHz to supply enough power for the output current load. The output voltage drops at the different current loads of 5 μA and 10 μA are 0.7 V and 2 V respectively as shown in Fig. 7.

The power efficiency and output voltage of the driver circuit at different current loads are plotted in Fig. 8. An efficiency of about 40% is achieved at load currents of 40 to 50 μA. In the light load condition, the output voltage can be kept at a relatively stable level due to the negative feedback which adjusts the frequency so that enough power is supplied to the output. When the current load is higher than 20 μA, the oscillator is almost working at its maximum frequency, and hence, the output voltage drop can't be compensated anymore by a frequency increase. As a result, the decreasing tendency of the output voltage becomes more pronounced. In this MEMS interferometer application, the driver circuit only needs to drive the capacitive actuator which means the driver circuit is working under zero-load condition. At this condition, the overall power consumption of this driver circuit is 1.78 mW.

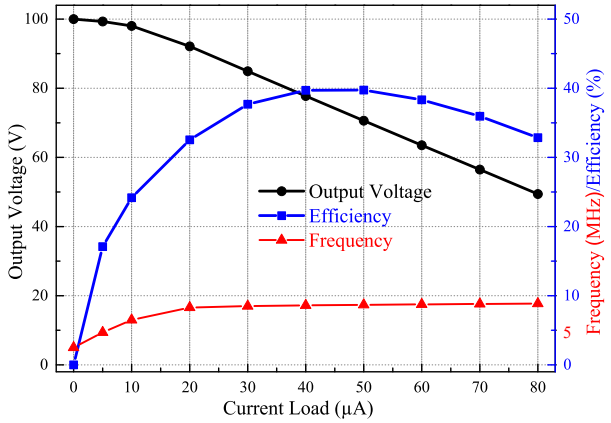

Fig. 8 Efficiency and output voltage at different current load

IV. Conclusion

This paper has presented a highly integrated monolithic driver circuit which is used in a MEMS-based interferometer. To improve the system's power efficiency, an advanced charge recycling strategy and finger capacitor structure are used to minimize the power dissipation caused by the parasitic capacitance in the high-voltage generator. The maximum efficiency of this driver circuit is 40%. Thanks to a frequency regulator and feedback circuit, the driver circuit offers an 8-bit resolution for programming the output voltage which can linearly sweep from 0 V to 100.9 V from a 3 V power supply under zero-load conditions. The driver circuit also can self-adjust the clock frequency to minimize the voltage variation caused by changes in the load conditions.

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